SONY®

Semiconductor IC

Data Book 1987

TVs

SONY®

Semiconductor Integrated Circuit Data Book 1987

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Semiconductor Integrated Circuit Data Book
1987

SONY®

PREFACE

This is the 1987 version of the Sony semiconductor IC databook. This book covers all the semiconductor products manufactured and marketed by Sony.

In preparation of this databook, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write; we welcome suggestions and comments.

The Sony semiconductor IC databook has been edited to include only accurate and reliable data. However, because of technical improvements and other modifications the contents are subject to change without notice.

The circuit examples used in this book are for illustration of typical applications only; we are not responsible for any problems that may occur in the circuitry and patents of any third party if these examples are put in practice.

Package abbreviations

DIP : Dual Inline Package
MFP : Mini Flat Package (=Flat DIP)
QIP : Quad Inline Package (=Flat QUIP)
PGA : Pin Grid Array
SRK : Shrink Dual Inline Package
SIP : Single Inline Package

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1. List of Model Names

Type	Page	Type	Page	Type	Page
CX-099	23	CX20159	283	CXK1005P	144
CX-7925B/-1	75	CX20183	63	CXK1006L	155
CX-7948	191	CX23055/-1	97	CXK1007P	161
CX-7958	201	CXA1011P/M	290	CXK1008L	172
CX-7961A/-1	86	CXA1024S	306	CXK1009P	178
CX20014A CX20015A	36	CXA1044P	328	CXK1201P	364
CX20100	219	CXD1053S	340	※BX-1330 BX-1396	376
CX20106A	248	CXD1054S	353	※BX-1387 BX-1407	382
CX20112	255	CXK1001P	108	※BX-1393 BX-1408	389
CX20125	276	CXK1002P	118	※BX-1398 BX-1409	395
CX20139	45	CXK1003P	128	※BX-1435	402
CX20155	53	CXK1004L	138	※BX-1436	410

※Hybrid ICs

2. Index by Usage

1) Signal System

Type	Function	Page
CX-099	Monolithic Tuner IC	23
CX20014A CX20015A	VIF/SIF Amplifier	36
CX20139	PLL Video Synchronous Detection	45
CX20155	CATV and VHF TV Tuner	53
CX20183	Television Picture Signal Processor IC	63

2) Tuning System

Type	Function	Page
CX-7925B/-1	Frequency Synthesizer PLL	75
CX-7961A/-1	Frequency Synthesizer PLL	86
CX23055/-1	Frequency Synthesizer PLL	97
CXK1001P	640-bit (40 word×16 bit) Non-volatile Memory	108
CXK1002P	560-bit (40 word×14 bit) Non-volatile Memory	118
CXK1003P	320-bit (20 word×16 bit) Non-volatile Memory	128
CXK1004L	512-bit (32 word×16 bit) Non-volatile Memory	138
CXK1005P	512-bit (32 word×16 bit) Non-volatile Memory	144
CXK1006L	1024-bit (64 word×16 bit) Non-volatile Memory (P)	155
CXK1007P	1024-bit (64 word×16 bit) Non-volatile Memory	161
CXK1008L	2048-bit (128 word×16 bit) Non-volatile Memory (P)	172
CXK1009P	2048-bit (128 word×16 bit) Non-volatile Memory	178

(P) : Preliminary

3) Supplementary Function

Type	Function	Page
CX-7948	Hatch Signal Generator for TV	191
CX-7958	TV Screen Display (CRT Display)	201
CX20100	RGB Interface for CTV	219
CX20106A	Preamplifier for Remote Control Use	248
CX20112	US Audio Multiplexing Decoder	255
CX20125	Dynamic Picture	276
CX20159	Power Supply IC for TV	283
CXA1011P/M	dbx-TV Noise Reduction IC	290
CXA1024S	RGB Interface Automatic White Balance	306
CXA1044P	RGB Interface for Ultra-High Resolution Display	328
CXD1053S	Picture-in-Picture Memory Control IC for TV	340
CXD1054S	Picture-in-Picture Data Control IC for TV	353
CXK1201P	Double Scan Converter (P)	364
※BX-1330 BX-1396	Infrared Ray Remote Control Receiver	376
※BX-1387 BX-1407	Infrared Remote Control Receiver	382
※BX-1393 BX-1408	Infrared Remote Control Receiver	389
※BX-1398 BX-1409	Infrared Remote Control Receiver	395
※BX-1435	US Multiplexing Sound Decoder Module	402
※BX-1436	US Multiplexing Sound Decoder Module	410

※ Hybrid ICs (P) : Preliminary

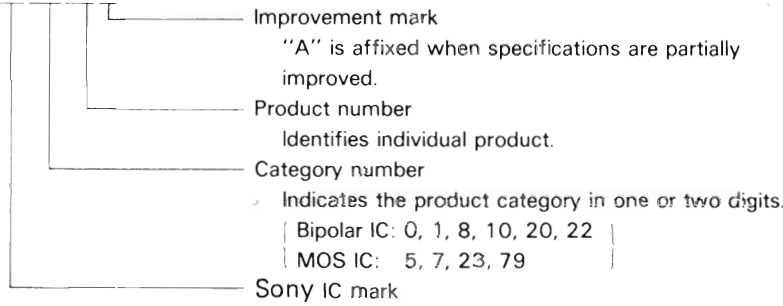
3. IC Nomenclature

1) Nomenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

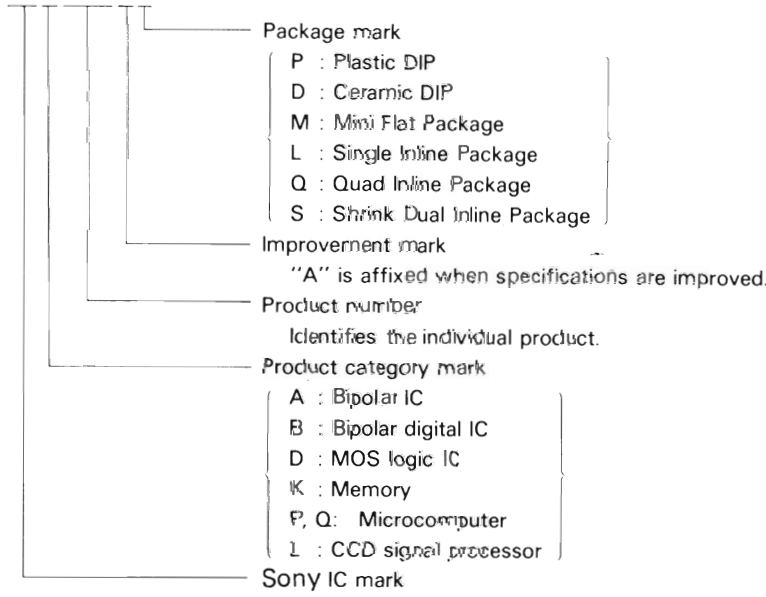
(1) Conventional nomenclature system

[Example] CX20011A


Improvement mark
"A" is affixed when specifications are partially improved.
Product number
Identifies individual product.
Category number
Indicates the product category in one or two digits.
Bipolar IC: 0, 1, 8, 10, 20, 22
MOS IC: 5, 7, 23, 79
Sony IC mark

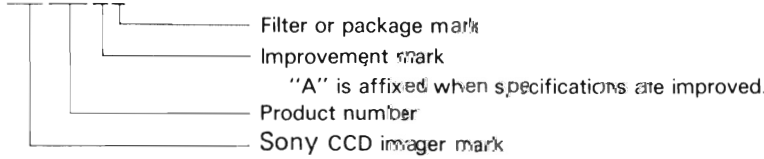
(2) New nomenclature

[Example] CXA1001AP


Package mark
P : Plastic DIP
D : Ceramic DIP
M : Mini Flat Package
L : Single Inline Package
Q : Quad Inline Package
S : Shrink Dual Inline Package
Improvement mark
"A" is affixed when specifications are improved.
Product number
Identifies the individual product.
Product category mark
A : Bipolar IC
B : Bipolar digital IC
D : MOS logic IC
K : Memory
P, Q: Microcomputer
L : CCD signal processor
Sony IC mark

2) Nomenclature for CCD image product name

[Example] ICX016AK



4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even in a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably short.

Maximum rating must never be reached for two items at the same time.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage Vcc (V_{DD})

The maximum voltage that can be applied between the power supply terminal and ground terminal.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit; the transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation PD

The maximum power consumption allowed in IC

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following:

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with the amount of IC integration in package types.

(3) Operating ambient temperature Topr

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at Ta=25°C are not guaranteed even in this temperature range.

(4) Storage temperature Tstg

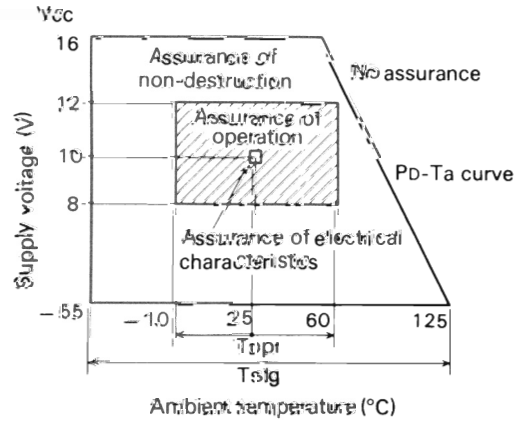
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage Vin, output voltage Vout, input current Iin, output current Iout and other values may be specified in some IC's.

The relationship among these maximum ratings for IC is shown below.



2) Protection against electrostatic breakdown

There have been problems of electrostatic destruction of electronic devices since the 2nd World War. Their history is closely related to the advancement in the semiconductor devices; that is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

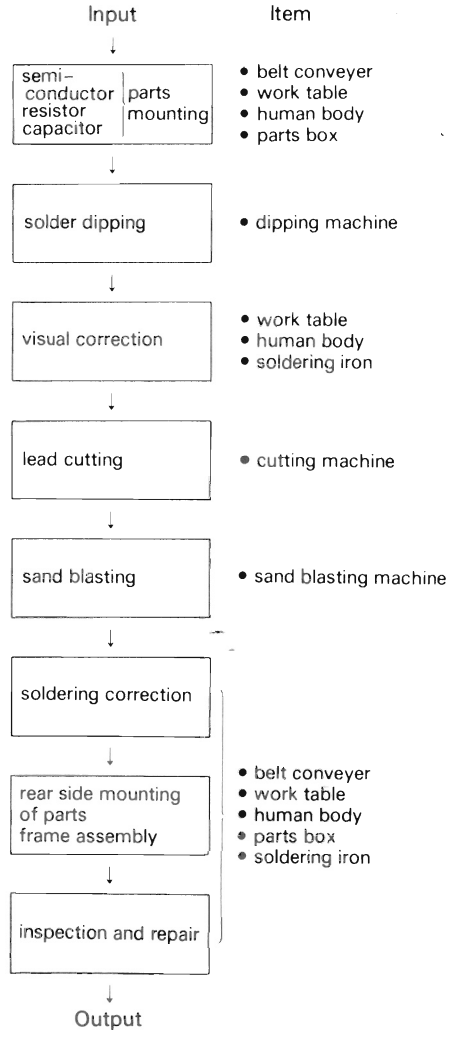
Today, the problem of electrostatic destruction is again drawing people's attention as we are entering the era of LSI and VLSI. Here are our suggestions for preventing electrostatic destruction in the device fabrication process.

Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:

Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for preventing electrostatic destruction

Explained below are procedures that must be taken in fabrication for preventing the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

① Equalize potentials of terminals when transporting or storing.

② Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.

③ Prepare an environment that does not generate static electricity.
One method is keeping relative humidity in the work room about 50%.

Operator

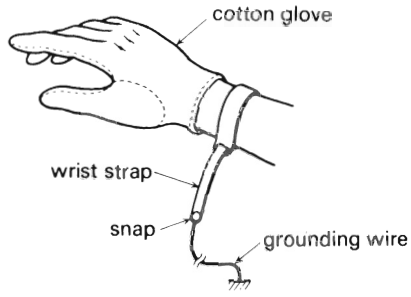
(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If wrist strap cannot be used, then the operator should touch the grounding point with his hand, before handling any semiconductor device.

example of grounding band



When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device

DIP type can type

Equipment and tools

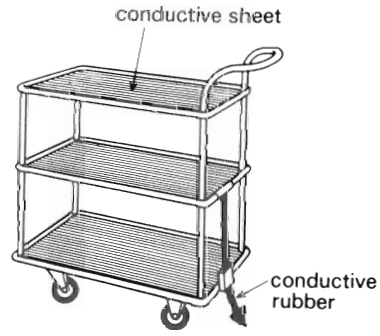
(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

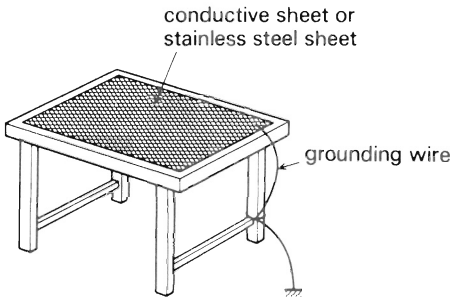
grounding of carrier



(2) Grounding of work table

Ground the work table as illustrated. Do not put anything which can easily generate static electricity, such as foam styrol, on the work table.

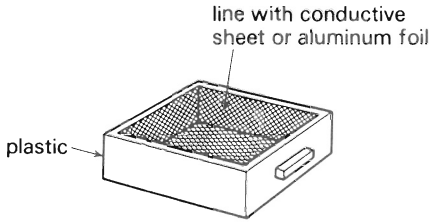
grounding of work table



(3) Semiconductor device case

Use the metal case, or the antistatic plastic case (lined with conductive sheet or aluminum foil).

plastic case for semiconductor devices



(4) Insertion of semiconductor device

Insert the semiconductor device in mounting process or on the belt conveyer. The insertion should be done on a conductive sheet, or a wood or metal carrier.

(5) Operation in energized state

When the substrate is checked while energizing the substrate where the delicate semiconductor device is mounted, be sure to place the substrate on corrugated cardboard, wood, or on a metal carrier.

(6) Other points of caution

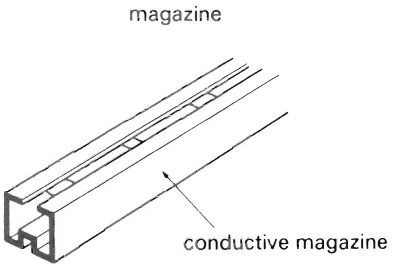
Take note of the kind of the brush material used for removing lead chips. Use metal or antistatic-treated plastic brushes.

Transporting, storing and packaging methods

(1) Magazine

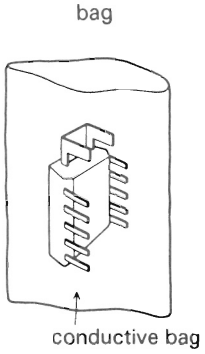
Use the metal, or antistatic-treated plastic IC magazines.

The plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.



(2) Bag

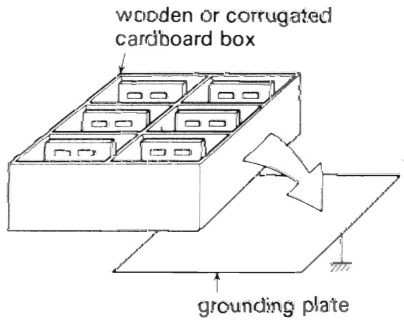
Use a conductive bag for keeping ICs. If use of a vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of wood or corrugated cardboard. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



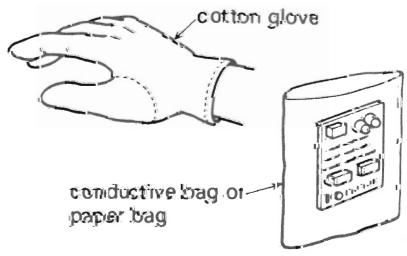
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table, or concrete floor for discharging. Do not pull the delivery box for more than 1 meter except on a concrete or a wooden floor.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive or paper bag. Do not use a polyethylene bag.

handling of mounted substrate



Soldering operation

(1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron whose insulation resistance after five minutes from energizing is greater than 10 MΩ (DC 500V).

(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by car.

(3) Correction

When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

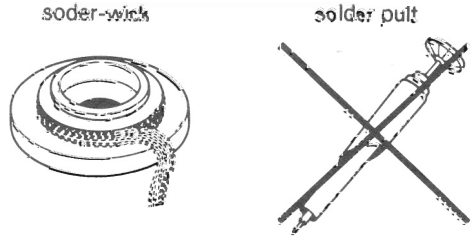
(4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to time during operation.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Soder-wick or equivalent.

solder remover



(6) Soldering work table

Use a grounded work table, corrugated cardboard, or wooden work table for soldering. Do not solder on foam styrol, vinyl, or decorative board.

3) Mounting method

Soldering and solderability

(1) Solderability guaranteed by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2". An abstract of this standard follows:

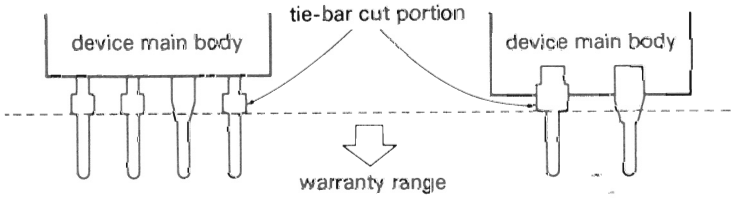
- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which has been heated to 230°C±5°C for 5±1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.

warranty area for soldering



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10±1 seconds in a solder bath of 260°C±5°C, or for $3^{+0.5}_{-0}$ seconds in a solder bath of 350°C ±10°C, for a distance of up to 1 to 1.5 mm from the main body.

The temperature of 260°C ±5°C assumes the soldering with solder flow system, and the temperature 350°C ±10°C assumes soldering by soldering iron.

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited for 10 seconds at 260°C ±5°C. The distance between the device main body and solder bath is assumed as 1.6 mm.

5. Quality Assurance and Reliability

Sony's Policy of Quality Assurance

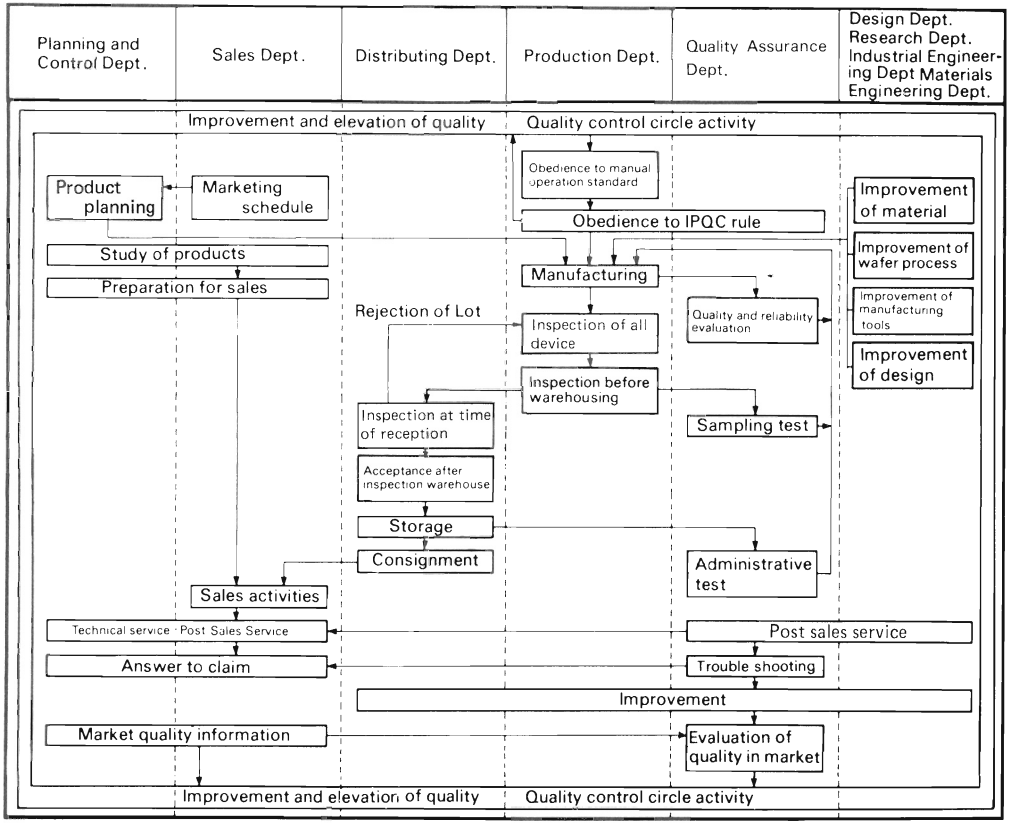
The Sony semiconductor embodies two fundamental ideas: "highest quality" and "lowest cost". There are the two key points for realizing these ideas.

One is the "quality" of men fabricating the semiconductor devices. The reliability of these people is reflected in the Sony products. Accordingly, Sony is making a continuous effort to raise the "quality" of people capable of manufacturing and fabricating Sony semiconductor devices.

The other point is a source management system combined with the concept of thorough quality design. With this system, higher quality products can be steadily manufactured through automation of device design, process design, and the fabrication process.

Sony is making constant efforts to supply the most economical and most useful products of very high quality for users.

Quality assurance system of semiconductor products



Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "total-inspected" at the final fabrication stage, thus ensuring no detective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodical reliability test

Type of Test		Test Hour	LTPD (%)
Electrical characteristic test		In order to know the quality level, some types are selected and tested again.	
LIFE TEST	High temperature operation	Up to 1000 hr	10%
	High temperature storage	Up to 1000 hr	10%
	Low temperature storage	Up to 1000 hr	10%
	High temperature and high humidity storage	Up to 1000 hr	10%
	High humidity bias test	Up to 1000 hr	10%
	High temperature and high humidity with bias	Up to 500 hr	10%
	Pressure cooker	Up to 200 hr	10%
ENVIRONMENT TEST	Soldering heat resistance heat cycle	10 s	15%
	Heat cycle	10 cycle	15%
MECHANICAL TEST	Solderability	Japan Industrial Standard (JIS)	15%
	Lead strength		15%
OTHER TESTS	if necessary test, are selected accordingly to JIS C7021, C7022, EIAJ SD121, IC121.		

• These tests are selected by sampling standard.

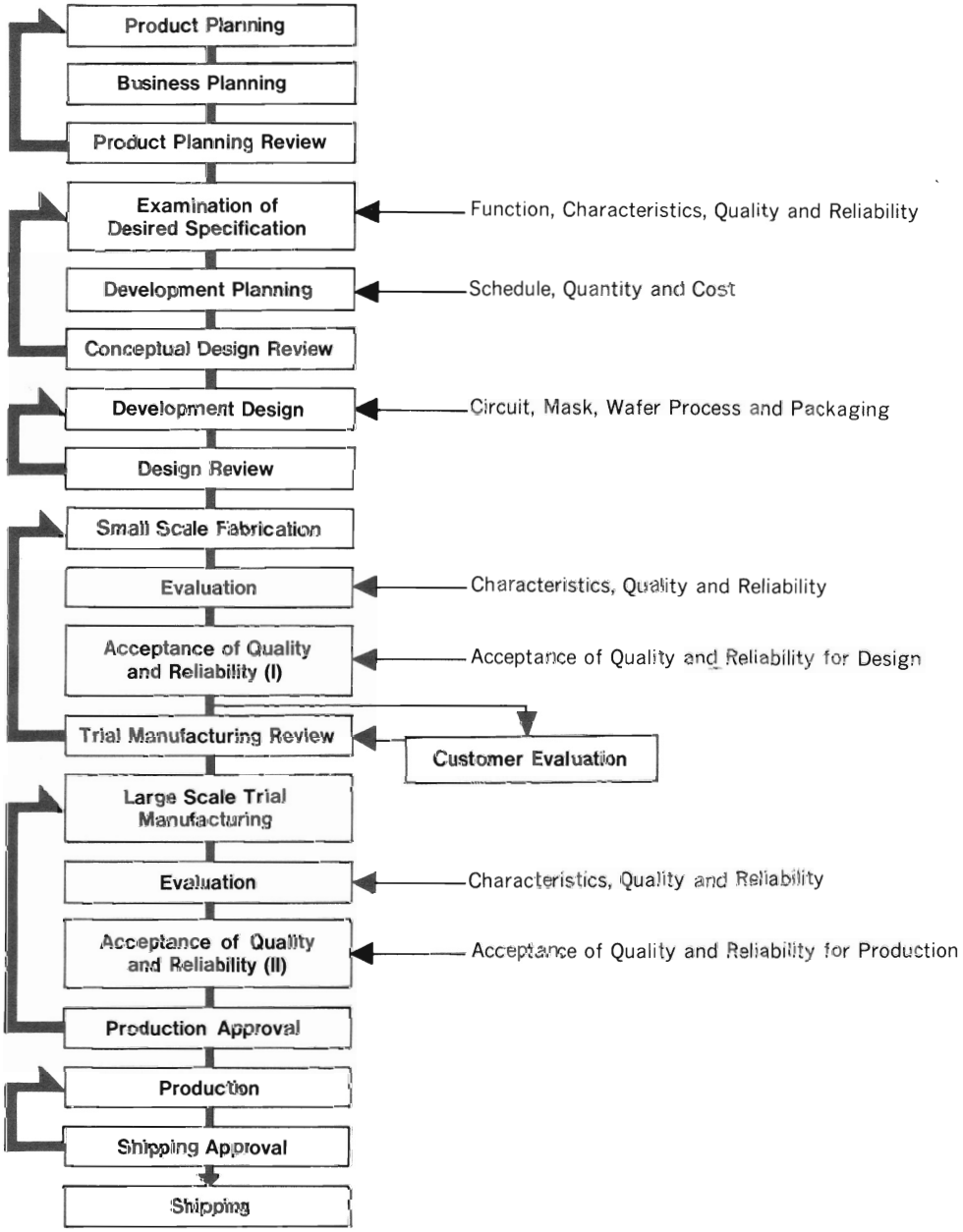
These tests and inspection data are useful not only to estimate quality in the market place but also as data to improve design and wafer processes.

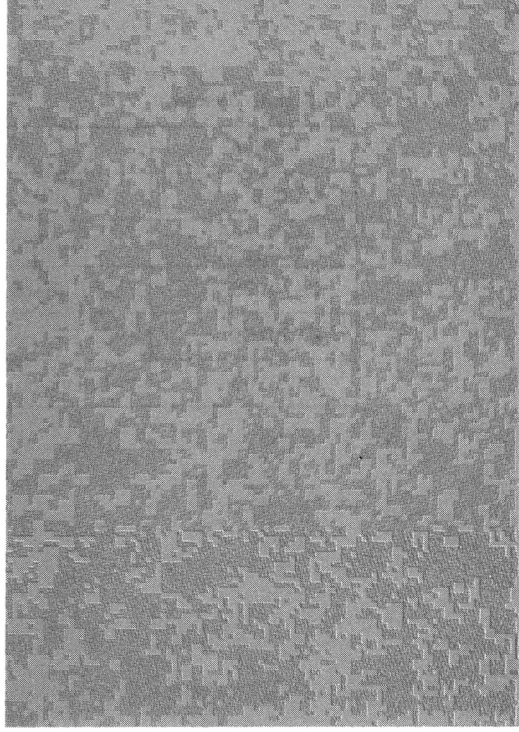
Reliability test standard for acceptance of products

Type of Test	Condition	Supply voltage	Testing time	LTPD(%)
High temperature operation	Ta = 125°C, 150°C	Typ	1000 hr	5%
High temperature with bias	Ta = 125°C, 150°C	Typ	1000 hr	5%
High temperature storage	Ta = 150°C		1000 hr	5%
Low temperature storage	Ta = −65°C		1000 hr	5%
High temperature and humidity storage	Ta = 85°C, 85%RH		1000 hr	5%
High temperature and High humidity with bias	Ta = 85°C, 85%RH	Typ (1 hr on/3 hr off)	1000 hr	5%
Pressure cooker	Ta = 121°C, 100%RH, 30 pounds per square inch		1000 hr	5%
Temperature cycle	Ta = −65°C to +150°C		100 C	10%
Heat shock	Ta = 0°C to +100°C		5 C	10%
Soldering heat resistance	Tsolder = 260°C		10 S	10S
Solderability	Tsolder = 230°C (Rosin type flux)		5 S	10%
Mechanical shock	X, Y, Z 1500G 0.5 ms half sine wave		3 times for each direction	10%
Vibration	X, Y, Z 20G 10 to 2000 to 10 Hz (4 min) sine wave vibration		16 minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000 G centrifugal acceleration		1 minute for each direction	10%
Fall by gravity	Falling from the height of 75cm to maple plate by gravity		3 times	10%
Lead strength (Bend) (Pull)	Japan Industrial Standard (JIS)			10%
Electrostatics strength	Device must be designed again, when electrostatic strength is below standard supplying surge voltage To each pin under the conditions of C = 200PF and Rs = 0Ω.			

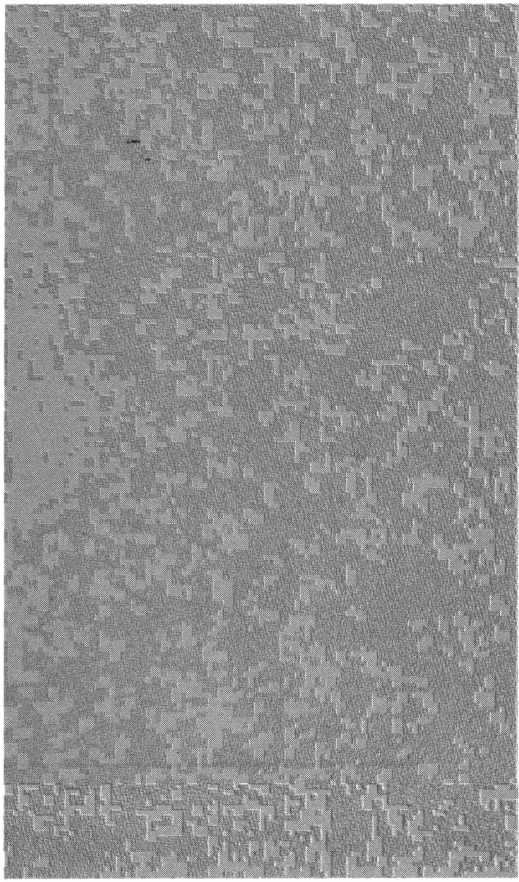
Flow Chart from Development to Manufacturing

Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.





Signal System



1) Signal System

Type	Function	Page
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Monolithic Tuner IC

Description

The CX-099 is a bipolar IC designed for VHF tuner of color TV and is composed of local oscillator, mixer, IF amplifier and constant resistance output circuit.

Features

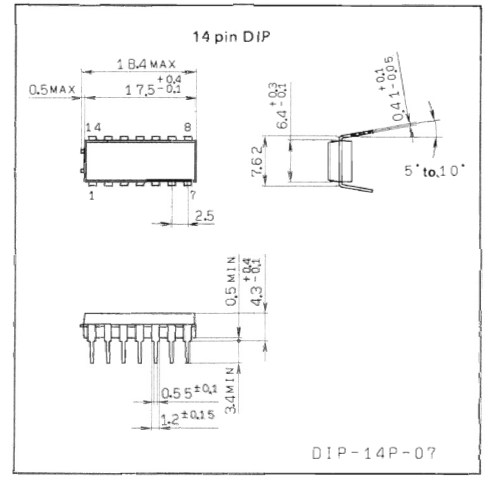
- Local oscillator has stable oscillation characteristics since it includes self-compensation circuit against the variations of temperature and power supply voltage.
- Mixer can provide stable conversion gain and IF stage is completely adjustment-free by wide band system.
- Constant resistance output circuit can produce good standing wave ratio characteristics and has the advantages of making it adjustment-free when connecting with VIF circuit.

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



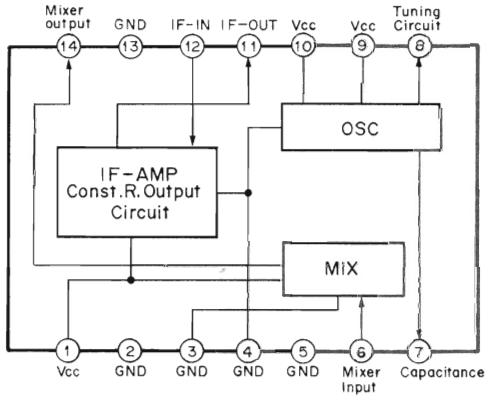
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	17	V
• Mixer input voltage	$V_{I(MIX)}$	12	Vp-p
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−50 to +150	°C
• Allowable power dissipation	P_D	1.7	W

Recommended Operating Condition

• Supply voltage	V_{CC}	11 to 13	V

Block Diagram



Electrical Characteristics

[AC Characteristics-1]

(Ta=25°C, Vcc=12V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
UIF Power Gain	UIF.PG	$f_{(IF)}$=43.5 MHz, V_I=67 dBμ 75Ω Open	31.0	33.5	38.0	dB	Fig. 2
RF Noise Figure	RF.NF	$f_{(RF)}$=200 MHz	8.0	11.0	14.5	dB	Fig. 8
UIF Noise Figure	UIF.NF	f=43.5 MHz	2.5	3.9	5.0	dB	Fig. 9
Local OSC Input Voltage-1	V_{inj1}	$f_{(OSC)}$=276 MHz, Vcc2=10V	200	280	370	mVr.m.s.	Fig. 11 Fig. 17
Local OSC Input Voltage-2	V_{inj2}	$f_{(OSC)}$=101 MHz, Vcc2=0.5V	400	500	600	mVr.m.s.	Fig. 11 Fig. 17
Local OSC Voltage Drift	$f_{V\text{-}drift}$	Vcc1±10% Change, $f_{(OSC)}$=276 MHz		±60	+150 −180	kHz	Fig. 11 Fig. 14
Local OSC Drift	OSC-S11	f=90 MHz, V_I=115 dBμ 75Ω Open	0.40	0.85	1.5	dB	Fig. 10
Conversion Gain-1	C.G1	$f_{(RF)}$=200 MHz, V_I=75 dBμ 75Ω Open, f_{IF}=43.5 MHz	21.0	25.0	29.0	dB	Fig. 3
Conversion Gain-2	C.G2	$f_{(RF)}$=57.5 MHz, V_I=75 dBμ 75Ω Open, f_{IF}=43.5 MHz	22.0	26.0	30.0	dB	Fig. 3
IF Band	ΔPG	$f_{(IF)}$=41.25−45.75 MHz, V_I=67 dBμ 75Ω Open	0.1	0.50	0.90	dB	Fig. 2
IF Gain Maximum Frequency	$f_{PG\text{-}MAX}$	V_I=67 dBμ 75Ω Open	41.0	44.0	47.5	MHz	Fig. 2

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Mixer Input Impedance	r_{ip}	f=200 MHz, P_I=−40 dBm 75Ω Open	170	240	310	Ω	Fig. 4
	C_{ip}		4.6	5.6	6.6	pF	Fig. 16
Constant Resistance Output Circuit SWR	V.S.W.R	f=43.5 MHz, V_I=100 dBμ 75Ω Open	1.1	1.5	2.5		Fig. 5 Fig. 12
Signal Level 1% Class Modulation	C.M *	f_D=200 MHz, $V_{I(fD)}$=74 dBμ, f_U=212 MHz 1kHz 40% AM 75Ω Open	85	90	100	dBμ	Fig. 6
Mixer Maximum Output	$V_{O\ MAX}$ *	$f_{(P)}$=200 MHz, $f_{(S)}$=204.5 MHz, $f_{(C)}$=203.58 MHz	110	117	125	dBμ	Fig. 7
Local OSC Leakage at Mixer Output	$V_{(OSC)\ Leak}$ *	$f_{(OSC)}$=276 MHz		103	108	dBμ	Fig. 11
Local OSC Starting Stability	$f_{S\ drift}$	$f_{(OSC)}$=276 MHz, t=3sec to 3min	±1	±60	±150	kHz	Fig. 11
Local OSC Frequency Temp. Stability	$f_{T\ drift}$	$f_{(OSC)}$=276 MHz, Ta=25±25°C	+3 −2	+70 −100	+150 −200	kHz	Fig. 11 Fig. 15

* CM, V_{OMAX}, $V_{(OSC)Leak}$ Value shows 75Ω open Value.

Electrical Characteristics

[DC Characteristics-2]

(Ta=25°C, V_{CC}=12V) Test circuit see Fig. 1.

Item	Symbol	SW Position		Min.	Typ.	Max.	Unit	Remark
		SW-1	SW-2					
Circuit Current	I_D	ON	OFF	23.0	30.5	38.0	mA	
Constant Resistance Output Circuit Different Voltage	ΔV_{CR}	ON	ON/OFF	300	335	370	mV	Note 1

Note 1) $\Delta V_{CR}=V_{CR(1)}-V_{CR(2)}$ $V_{CR(1)}$ .... V_{11} Voltage at SW-2 OFF.
$V_{CR(2)}$ .... V_{11} Voltage at SW-2 ON.

DC Characteristics

Test Circuit See Fig. 1

Item		Typ.	Unit
Pin Voltage	Pin No. 6	0.83	V
	Pin No. 7	7.40	V
	Pin No. 8	8.20	V
	Pin No.11	6.60	V
	Pin No.12	2.50	V
	Pin No.14	7.20	V
Pin Current	Pin No. 1 (A_2)	23.30	mA
	Pin No. 9 (A_3)	7.20	mA

Electrical Characteristics-2

[DC Characteristics-2] Test Circuit

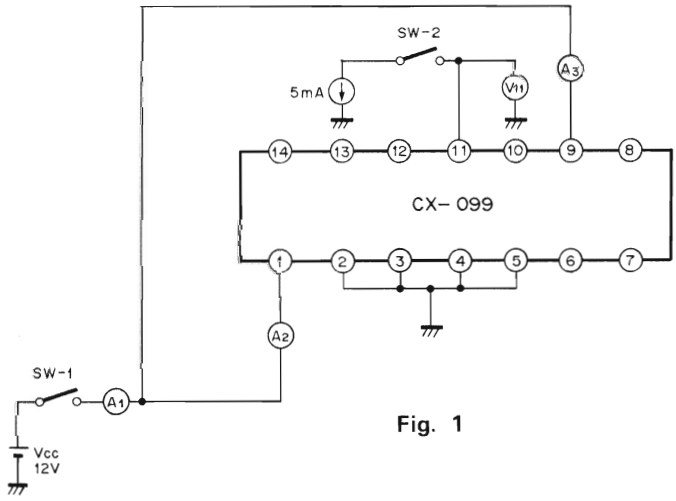


Fig. 1

Item	Symbol	Test Point
Circuit Current	I_D	A_1
Pin Input Current	I_{A2}	A_2
	I_{A9}	A_3
Constant Resistance Output Circuit Difference Voltage	ΔV_{CR}	V_{11}

UIF Voltage Gain, IF Band Characteristics, IF Gain Maximum Frequency Test Circuit

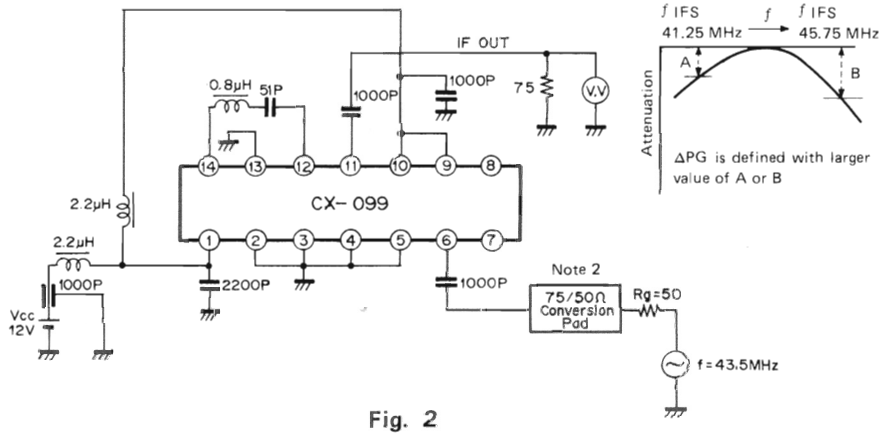


Fig. 2

Note 2) Use the transformed pad as the impedance conversion pad unless otherwise specified.

Conversion Gain 1, 2 Test Circuit

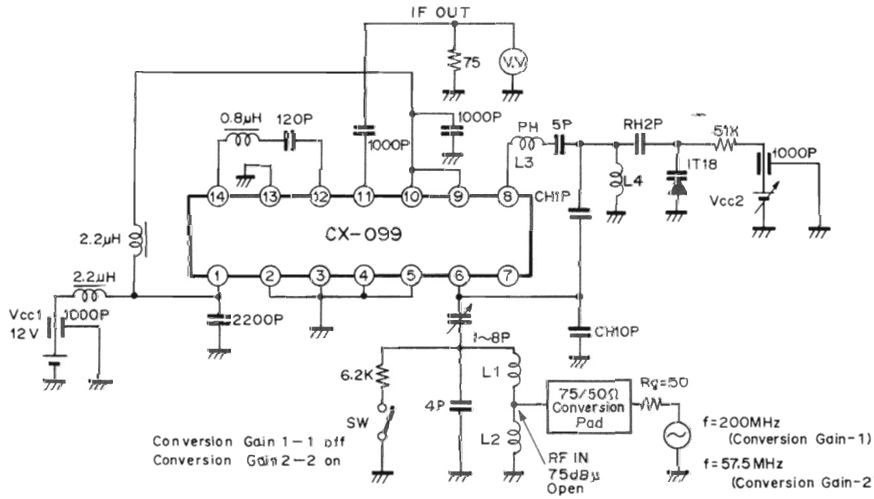


Fig. 3

Note 3) The constant of the input matching inductance (L1 and L2) and the constant of the inductance (L3 and L4) of the oscillator resonance circuit in the conversion gain-1 (f=200 MHz) measuring circuit and those in the conversion gain-2 (f=57.5 MHz) measuring circuit are different.

Mixer Input Impedance Test Circuit

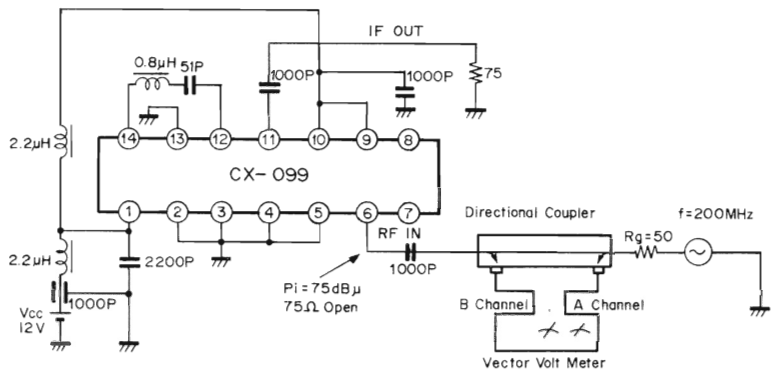


Fig. 4

Constant Resistance Output Circuit VSWR Test Circuit

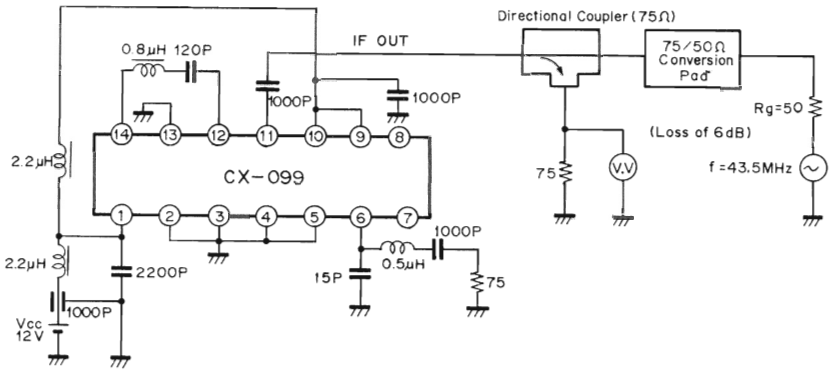


Fig. 5

Signal Level 1% Closs Modulation Test Circuit

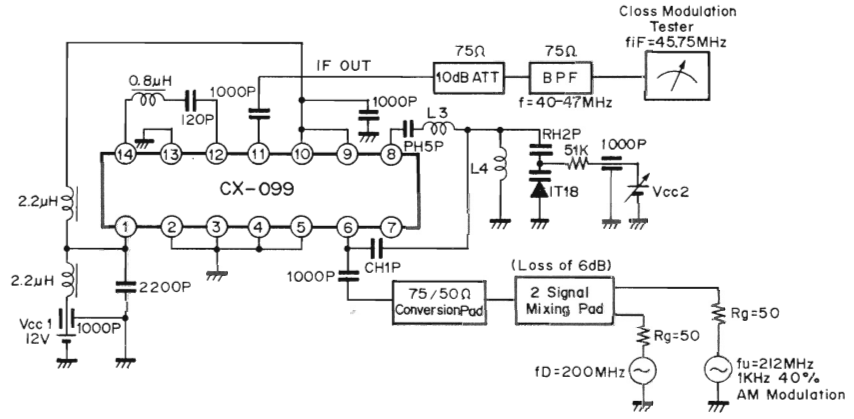


Fig. 6

Mixer Maximum Output Test Circuit

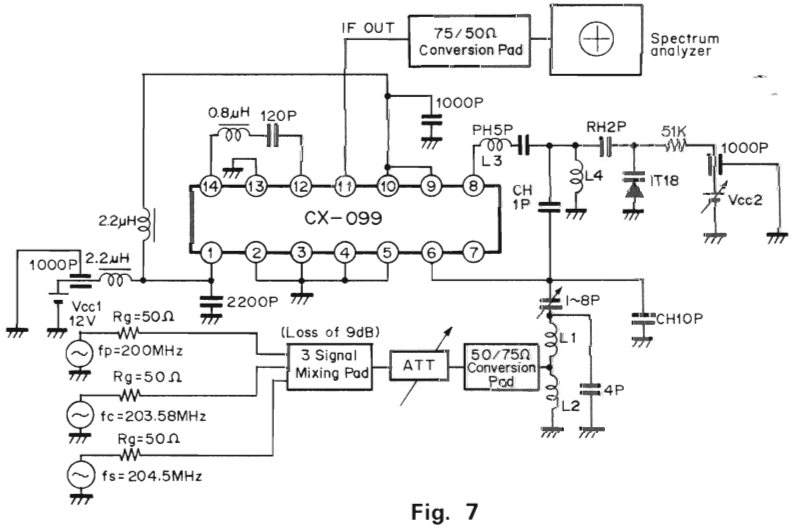


Fig. 7

Note 4) Input Condition

$$20 \log \frac{Vfc}{Vfp} = -12 \text{ dB}$$

$$20 \log \frac{Vfs}{Vfp} = -1.7 \text{ dB Mixer Maximum output} = \frac{\text{Beat Level (fs}-\text{fc)}}{\text{fp Level}} = 40 \text{ dB}$$

RF Noise Fig. 1 Test Circuit

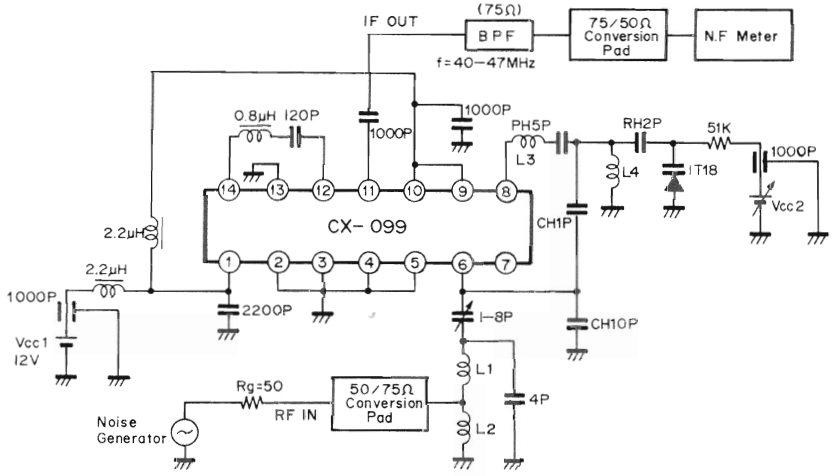


Fig. 8

UIF Noise Fig. 2 Test Circuit

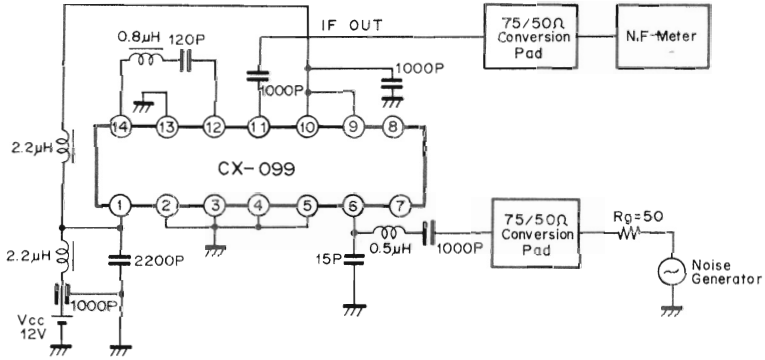


Fig. 9

Local OSC Stability Test Circuit

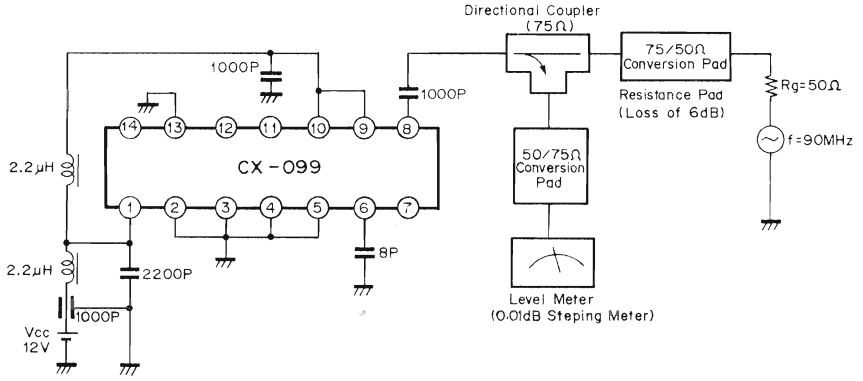
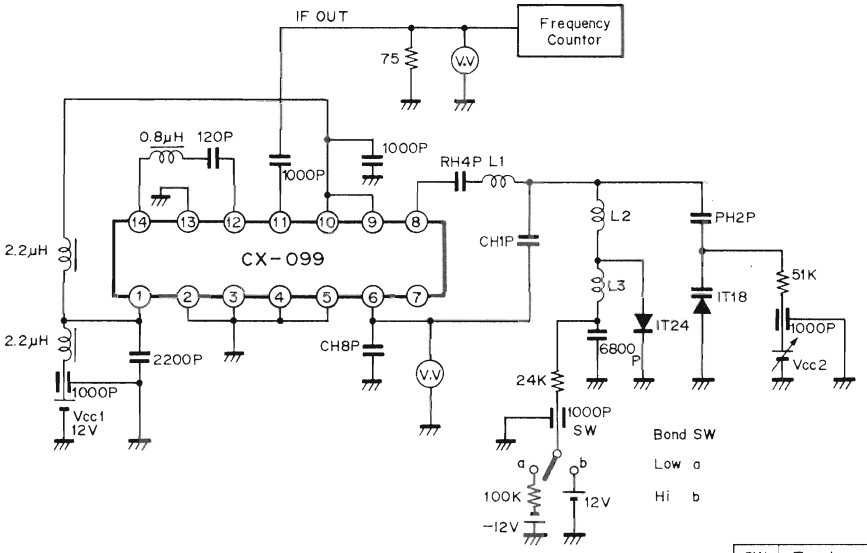


Fig. 10

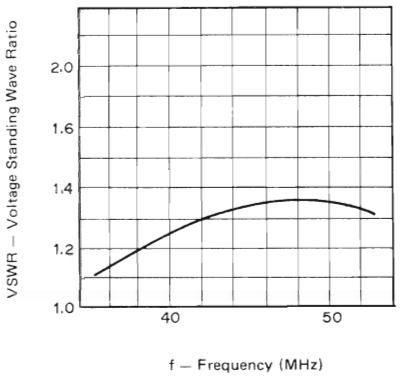
Local OSC Stability, Injection Voltage 1, 2, IF Local OSC Leakage Voltage Test Circuit



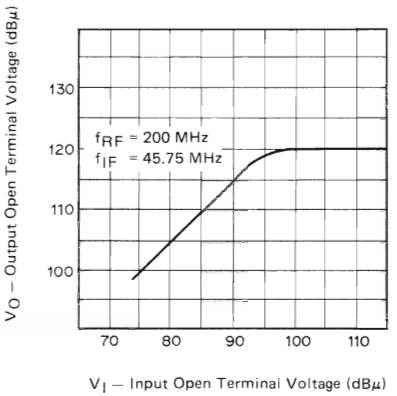
SW	Test Items
a	Vinj2
b	Vinj1 ∫ V-drift V osc Leak ∫ S-drift ∫ T-drift

Fig. 11

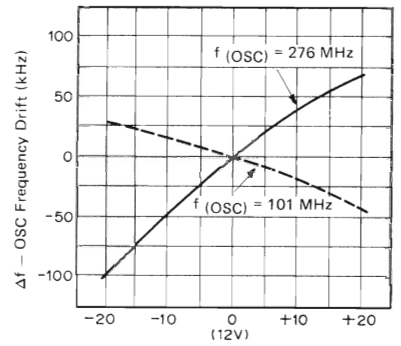
Constant Resistance Output Circuit VSWR



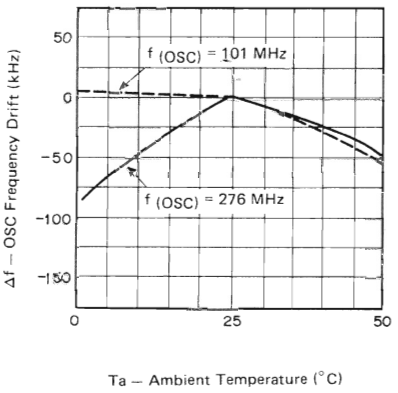
Mixer Input/Output Characteristics



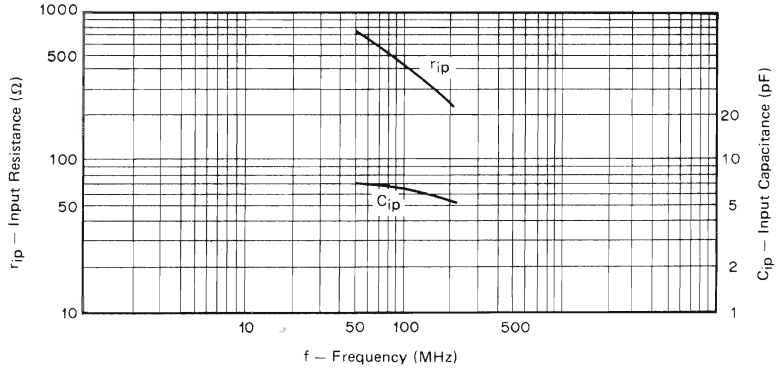
OSC Frequency Voltage Stability



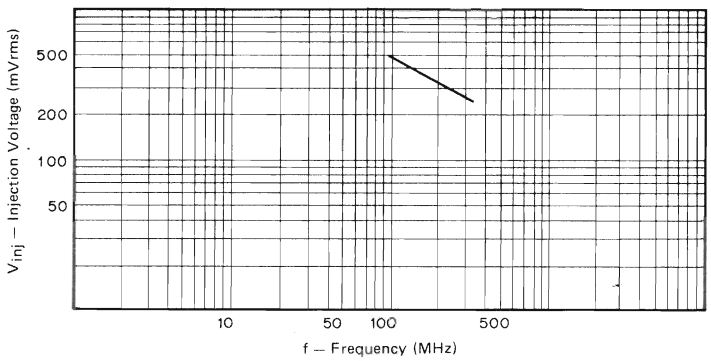
OSC Frequency Temperature Stability



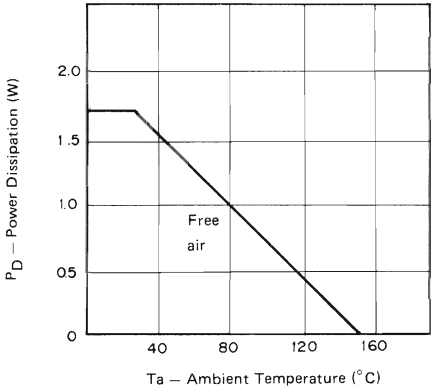
Mixer Input Impedance Frequency Characteristics



Injection Voltage Frequency Characteristics

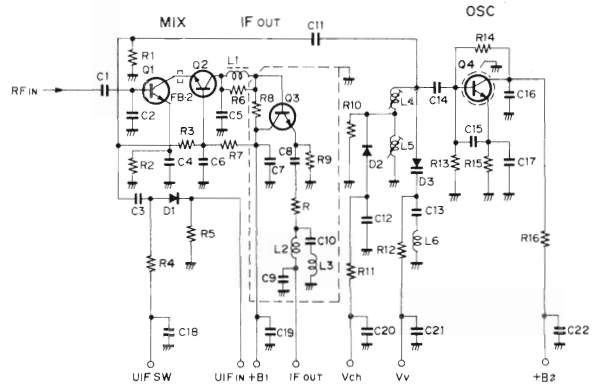


Allowable Power Dissipation Derating Curve

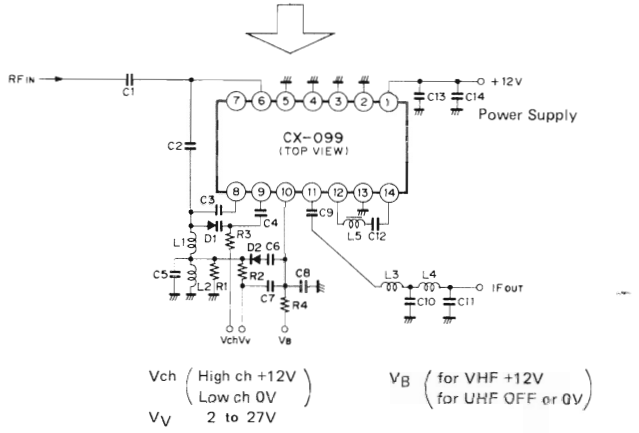


Application Circuit (JAPAN Tuner)

Conventional Circuit



IC Circuit



Vch (High ch +12V / Low ch 0V) VB (for VHF +12V / for UHF OFF or 0V)

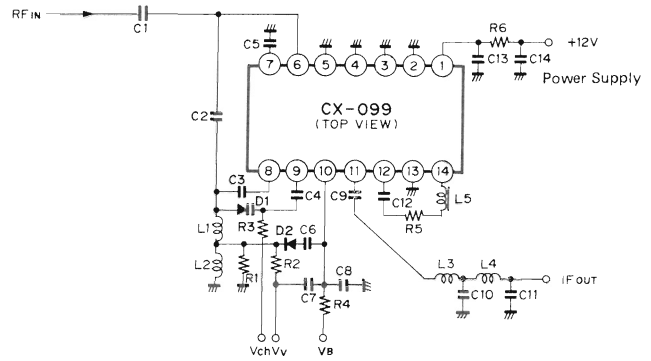
VV 2 to 27V

Parts List

Capacitor	Value	Characteristics Temperature	Capacitor	Value	Characteristics Temperature	Resistor	Value	Coil	Wire	Bobbin	Turns
C1	[F] 1n	SL	C8	[F] 4.7n	SL	R1	[Ω] 2.2k	L1	[mmφ] 0.5	[mmφ] 2.6	[t] 3.5
C2	1.5p	CH	C9	10n	SL	R2	5.1k	L2	0.5	3.0	4.5
C3	5p	SH	C10	39p	SL	R3	10k	L3	0.45	3.0	8.5
C4	18p	SH	C11	24p	SL	R4	620	L4	0.45	3.0	15.5
C5	3p	AH	C12	82p	SL			L5	0.27	drum core	7.5
C6	82p	TH	C13	4.7n	SL						
C7	4.7n	SL	C14	680p	SL						

Note) L5 is 0.6to0.8μH

Application Circuit (USA Tuner)



Vch (High ch +12V / Low ch 0V) V_B (For VHF +12V / For UHF OFF or 0V)

V_V 2 to 27V

Parts List

Capacitor	Value	Characteristics Temperature	Capacitor	Value	Characteristics Temperature	Resistance	Value	Coil	Wire	Bobbin	Turns
C1	[F] 1n	SL	C8	[F] 4.7n	SL	R1	[Ω] 3.6k	L1	[mmφ] 0.5	[mmφ] 2.6	[t] 3.5
C2	1.5p	AH	C9	10n	SL	R2	2.2k	L2	0.5	3.0	8.5
C3	6p	RH	C10	56p	SL	R3	10k	L3	0.45	3.0	12.5
C4	27p	CH	C11	33p	SL	R4	620	L4	0.45	3.0	17.5
C5	4p	SH	C12	68p	SL	R5	33	L5	0.27	drum core	9.5
C6	100p	UJ	C13	4.7n	SL	R6	10				
C7	4.7n	SL	C14	4.7n	SL						

Note) L5 is 0.8to1.1 μH

SONY CX20014A/20015A

VIF/SIF Amplifier

Description

The CX20014A/CX20015A are bipolar monolithic integrated circuits for the color TV set, with perform the functions of VIF, SIF, and AFT. The CX20014A/CX20015A include VIF amplifier, limiter amplifier for sound carrier detection, inter-carrier syncronous detector, ANC, RF AGC amplifier, AFT, AFT defeat input, AFT control signal output, SIF limiter amplifier, and muting circuit for detected sound output.

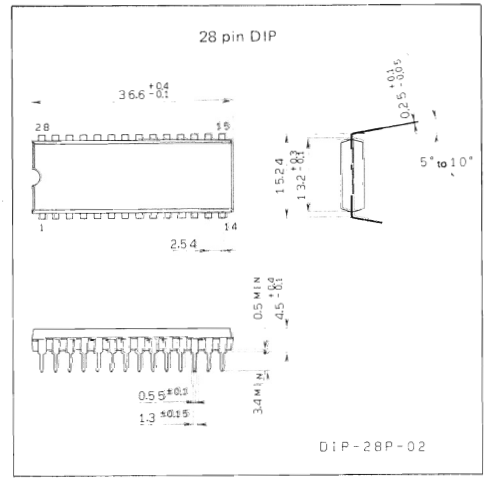
The CX20014A is designed for 9.0V operation, and the CX20015A is for 12.0V, respectively.

Features

- It is possible to employ the CX20014A/CX20015A for all the color TV sets (NTSC, PAL, SECAM).
- The CX20014A/CX20015A offer the VIF output suitable to the multiplex sound system.

Package Outline

Unit: mm



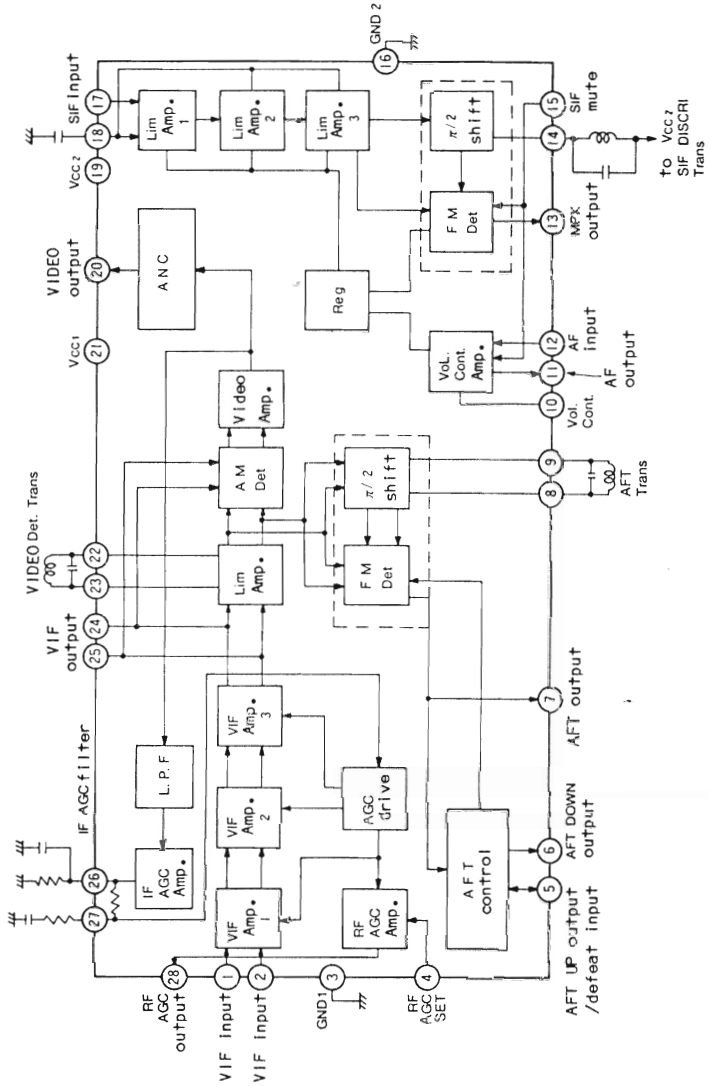
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	15	V	
• VIF input voltage	$V_{1\text{-}2}$	5	Vp-p	Between terminal 1 and 2
• SIF input voltage	$V_{17\text{-}18}$	3	Vp-p	Between terminal 17 and 18
• Sound input voltage	V_{12}	3	Vp-p	Terminal 12
• Operating temperature	Topr	−20 to +75	°C	
• Storage temperature	Tstg	−55 to +150	°C	
• Allowable power dissipation	P_D	1.15	W	

Recommended Operating Conditions

• Supply voltage	V_{CC}	8.7 to 9.3	V	(CX20014A)
	V_{CC}	11.7 to 12.3	V	(CX20015A)

Block Diagram



Electrical Characteristics

(Ta = 25°, V_{CC} = 9V)

Item	Symbol	Conditions				Test point	Min.	Typ.	Max.	Unit	Remark
		Input signal	Input level	Input point	ON-SW						
Sync Peak Voltage of Video Det. Out	VSPD	58.75MHz CW	−25dBm	IN1	S8	I	2.56	2.97	3.41	V	
Video Det. Output Level	VVAC	58.75MHz TV AM 15.75kHz 87.5%	−20dBm	IN1	S8	I	1.58	1.95	2.37	Vp-p	
Video Det. Sensitivity	VVSen	58.75MHz TV AM 15.75kHz 87.5%	−60dBm	IN1	S8	I	1.26			Vp-p	
VIF Gain Reduction	VGR	58.75MHz TV AM 15.75kHz 87.5%	−7dBm	IN1 IN1	S8	I	1.62	1.97	2.42	Vp-p	
Video Det. Differential Gain	DG	58.75MHz TV AM 15.75kHz 87.5% 54.25MHz CW	−25dBm −45dBm	IN1	S8	I			20	%	DG is to be measured, B.P.F(4.5MHz) Connecting Measurement Point "I", to read Detector output Level of 15.75kHz
IF AGC Max. Voltage	VIAMD	58.75MHz CW	−25dBm	IN1	S1-B	K	6.75	7.54		V	
ANC turned over Voltage	VANCD	58.75MHz CW	−25dBm	IN1	S1-B	I	4.00	4.50	5.00	V	
RF AGC Min. Voltage	VRAMD				S1-A S2-B	L			0.22	V	
RF AGC Max. Voltage	VRAMX				S2-B	L	7.00 (7.95)	7.50 (8.57)	8.00 (9.00)	V	Note 1
RF/IE AGC Amp. Voltage Gain	AMP	15.75kHz CW	−45dBm	IN5	S1-C, S9, S10, S11	L	41 (42)	45 (46)	49 (50)	dB	ADD 9.5dB (12dB) to a measured value, that is a loss of connected external Resistor (10kΩ) with terminal "28".
RF AGC Set Voltage	VRASD	58.75MHz CW	−15dBm	IN1	S2-A S8	A	3.8	4.65	5.6	V	Voltage source "E2" is adjusted to get at 3 to 4 volts of Measurement Point "L", and is fixed.

Item	Symbol	Conditions				Test point	Min.	Typ.	Max.	Unit	Remark
		Input Signal	Input level	Input Point	ON-SW						
AFT Sensitivity	VASen	58.75MHz 400Hz±10kHz FM	−25dBm	IN1	S8	D	24	34	48	mV/ kHz	
AFT Output Voltage at Zero Signal	VAND				S1-A	D	3.7	4.4	5.2	V	
AFT Max. Voltage	VAMAX	58.50MHz CW	−25dBm	IN1	S8	D	7.82			V	
AFT Min. Voltage	VAMIN	59.00MHz CW	−25dBm	IN1	S8	D			1.0	V	
AFT Defeat Voltage	VADFD	59.00MHz CW	−25dBm	IN1	S3-B S8	D	3.9	4.5	5.2	V	
AFT Defeat Drive Voltage	VADDR	59.00MHz CW	−25dBm	IN1	S3-A S8	B	6.19	6.72	7.27	V	Voltage source "E4" is adjusted to get same a value of measurement point "D" as "VADFD", is increased from zero Volts, and is fixed. To measure point "B".
AFT Up Voltage	VAFUP				S1-A S4-B	B	4.0	4.8	5.1	V	
AFT Up Drive Voltage	VAUPD				S1-A S4-A	D	6.1	6.6	7.2	V	Voltage source "E6" is adjusted to get same a value of measurement point "B" as "VAFUP", is increased from zero Volts, and is fixed. To measure point "D".
AFT Down Voltage	VAFDN				S1-A S4-C	C	4.0	4.9	5.1	V	

Item	Symbol	Conditions				Test point	Min.	Typ.	Max.	Unit	Remark
		Input signal	Input level	Input point	ON-SW						
AFT Down Drive Voltage	VADND				S1-A S4-A	D	1.93	2.35	2.80	V	Voltage Source "E6" is adjusted to get same a value of measurement point "C" as "VAFDN", is decreased from 9 volts, and is fixed. To measure point "D"
SIF Det. Sensitivity	VSSen	4.5MHz FM 400Hz±25kHz	−75dBm	IN3	S7-A	G	−21	−14.8		dBs	
SIF Det. Output Level	VSACL	4.5MHz FM 400Hz±25kHz	−20dBm	IN3	S7-A	G	−9.5	−7.0	−3.0	dBs	
SIF Det. Output Distortion	THDs	4.5MHz FM 400Hz±25kHz	−20dBm	IN3	S7-A	G			1	%	
SIF AM Rejection Ratio	AMR	4.5MHz AM 30% 400Hz	−17.7 dBm	IN3	S7-A	G	47	66.6		dB	
S Curve Max. Voltage	VSCMX	4.6MHz CW	−20dBm	IN3	S7-A	G	5.2	6.0	6.8	V	
S Curve Min. Voltage	VSCMN	4.4MHz CW	−20dBm	IN3	S7-A	G	1.2	1.8	2.2	V	
SIF Muting Attenuation	SMR	4.5MHz FM 400Hz±25kHz	−20dBm	IN3	S6-B S7-A	G	69			dB	Level ratio of measurement point "B" value at a condition of S6-B ON/at a condition of S6-B OFF.
SIF Muting Drive Voltage	VSMTD	4.5MHz FM 400Hz±25kHz	−20dBm	IN3	S6-A S7-A	H	2.4	3.0	3.6	V	Voltage Source "E13" is adjusted to get same a value of measurement point "G" as "SMR", is increased from zero Volts, and is fixed. To measure point "H".
SIF Muting Voltage	VSMDC				S6-B S7-A	G	3.4	3.9	4.3	V	

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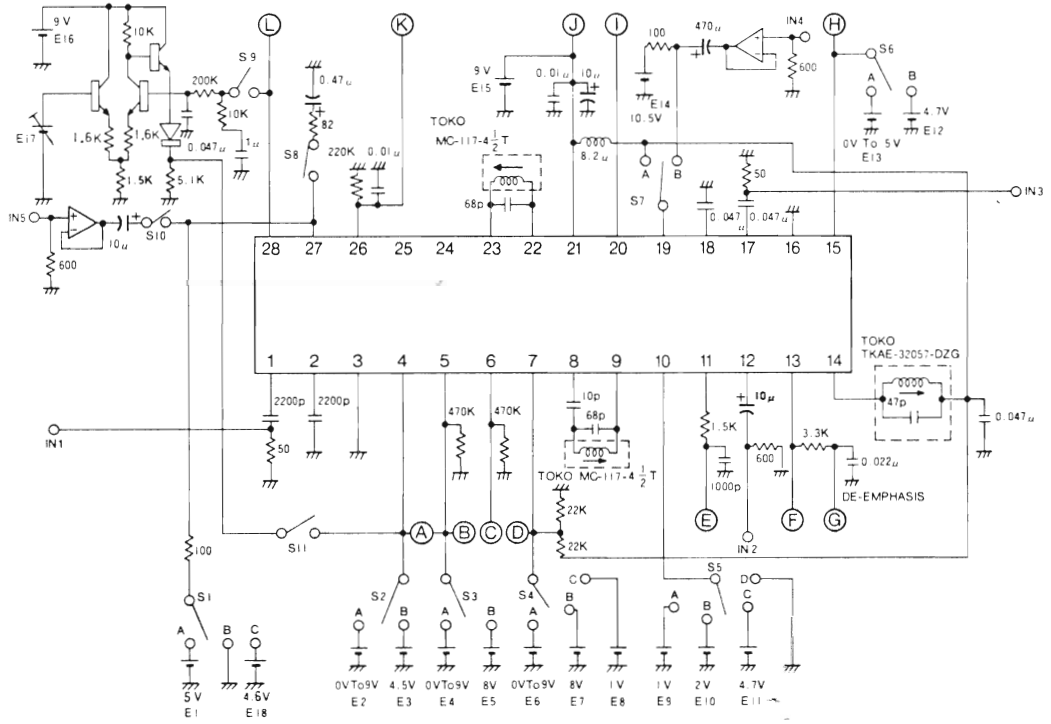
Item	Symbol	Conditions				Test point	Min.	Typ.	Max.	Unit	Remark
		Input Signal	Input level	Input Point	ON-SW						
SIF Ripple Suppression Ratio	SRP	4.5MHz CW 50Hz CW	−20dBm −20dBs	IN3 IN4	S7-B	G	17	26.3		dB	Suppression Ratio toward Ripple of terminal "19".
AF Ripple Suppression Ratio	VRP	50Hz CW	−20dBs	IN4	S7-B	E	32	37.8		dB	Suppression Ratio toward Ripple of terminal "19".
AF Muting Attenuation	VMR	15.75kHz CW	1Vp-p	IN2	S5-C, S6-B, S7-A	E	64	69.5		dB	Level ratio of measurement point "B" value at a condition of "S6-B ON"/at a condition of "S6-B OFF".
AF Muting Drive Voltage	VVMDD	15.75kHz CW	1Vp-p	IN2	S5-C, S6-A, S7-A	H	2.20	2.64	3.14	V	Voltage Source "E13" is adjusted to get a value of measurement point "E" as "−65dBs", and is fixed. To measure point "H".
AF Vol. Cont. Curve 1	V_{CC1}	15.75kHz CW	1Vp-p	IN2	S5-A S7-A	E	0.5	1.1	2.1	mVrms	
AF Vol. Cont. Curve 2	V_{CC2}	15.75kHz CW	1Vp-p	IN2	S5-B S7-A	E	23	38	62	mVrms	
AF Vol. Cont. Curve 3	V_{CC3}	15.75kHz CW	1Vp-p	IN2	S5-C S7-A	E	446	605	786	mVrms	
Vol. Cont. Amp. Output Distortion	THDV	15.75kHz CW	1Vp-p	IN2	S5-C S7-A	E		0.22	0.55	%	
A change of Vol. Cont. Amp. Out DC	VVDLV				S5-C, S5-D, S7-A	E		0.24	0.44	V	Output Voltage Difference of measurement point "E" is measured at "S5-C ON" and "S5-D ON" condition.
Supply Current	I_{CC}	58.75MHz CW	−25dBm		S7-A S8	J		68	88	mA	

Note 1:Value without a parenthesis is CX20014A, Value with a parenthesis is CX20015A.
COMPLEMENT: 0 dBs = 0.775V

Electrical Characteristics Test Circuit

The Circuit pulls in DC voltage for RF/IF AGC Amp



Note) Voltage source "E17" is adjusted to get at 3 volts of Test point "L", and is fixed when to measure Characteristics "RF/IF AGC Amp Voltage Gain".

Pin Description

No.	Symbol	Description
1	VIF input	Input terminal of VIF signal. To use Capacitor coupling in case of putting signal.
2	VIF input	Input terminal of VIF signal. To use Capacitor coupling in case of putting signal.
3	GND1	GND terminal of VIF block
4	RF AGC SET	AGC Voltage appears in terminal "28" by supplied Voltage source with terminal "4" and VIF Input Level, and is decreased, when VIF Input Level becomes more than Input Level of supplied a set Voltage source with terminal "4".
5	AFT UP output/ defeat input	DC voltage appears in this terminal, when VIF Input Frequency becomes less than a certain value. More over, AFT defeat voltage appears in terminal "7" of AFT output, when you supply this terminal with voltage source. It is a set voltage source with "AFT Defeat Drive Voltage" referred "ELECTRICAL CHARACTERISTICS"
6	AFT DOWN output	DC voltage appears in this terminal, when VIF Picture Signal becomes more than a certain value.
7	AFT output	DC voltage appears by a change of VIF Picture Signal Frequency.
8	AFT Trans	To connect a transformer tuned in VIF Picture Signal.
9	AFT Trans	To connect a transformer tuned in VIF Picture Signal.
10	Vol. Cont.	It is possible to control Gain of Volume Control Amp., when you supply this terminal with voltage source.
11	AF output	Output terminal of Volume Control Amp.
12	AF input	Input terminal of Volume Control Amp.
13	MPX output	Output terminal of SIF Detector
14	SIF Discri Trans	To connect a transformer used SIF FM Detector.
15	SIF mute	A muting terminal for detected SIF Sound output and Volume Control Amp. output. A voltage source supplies this terminal, and is a set voltage Level.
16	GND2	GND terminal of SIF block
17	SIF input	To put SIF signal in this terminal, to use capacitor coupling in case you put a signal. Terminal "18" is DC feed back terminal, is AC grounding.
18	SIF input	To put SIF signal in this terminal, to use capacitor coupling in case you put signal. Terminal "18" is DC feed back terminal, is AC grounding.
19	V_{CC2}	Power Supply terminal of SIF block, applied +9 Volts usually.
20	VIDEO output	Output terminal of VIF detector for picture.
21	V_{CC1}	Power Supply terminal of VIF block, applied +9 Volts usually.
22	VIDEO Det. Trans	To connect a transformer tuned in VIF Picture Signal.

No.	Symbol	Description
23	VIDEO Det. Trans	To connect a transformer tuned in VIF Picture Signal.
24	VIF output	Output terminal of amplified VIF Signal.
25	VIF output	Output terminal of amplified VIF Signal.
26	IF AGC filter	To connect a filter for IF AGC
27	IF AGC filter	To connect a filter for IF AGC
28	RF AGC output	AGC voltage appears for tuner by a change of VIF input signal level.

PLL Video Synchronous Detection

Description

The CX20139 is a PLL video synchronous detection bipolar IC to be used in combination with the CX20014A/20015A. It is provided with PLL, synchronous detection, AGC, ANC/WNL, and internally stabilized power supply false synchronous detection/synchronous detection switching circuits.

Features

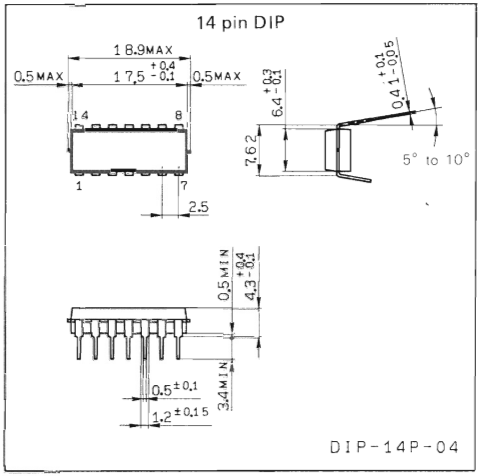
- Due to the PLL synchronous detection, video detection output with least distortion can be obtained.
- It has a function to select synchronous detection and false detection.

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



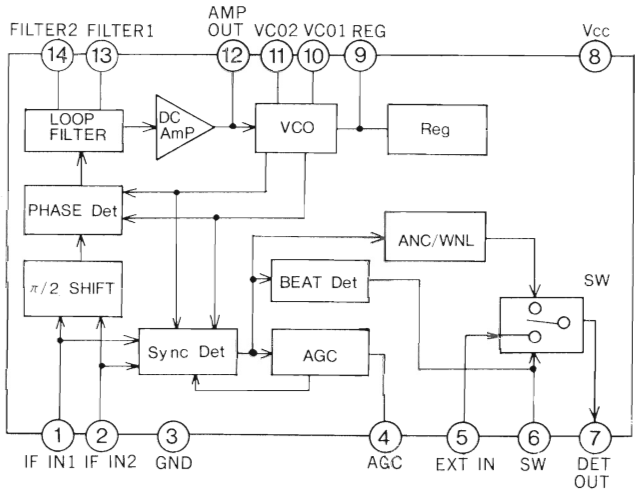
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	17	V
• Input voltage	V_{1-2}	4 (Pins 1 and 2 inputs)	Vp-p
• Applied voltage of pin 5	V_5	9	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1.04	W

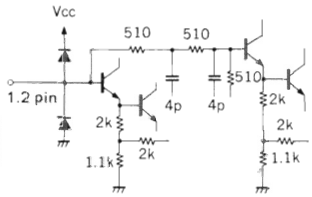
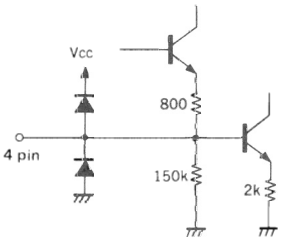
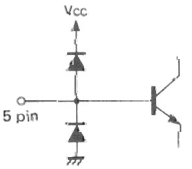
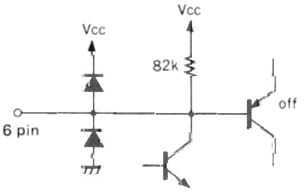
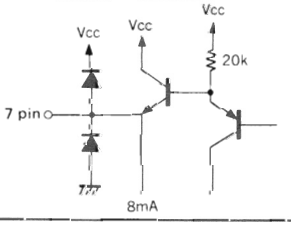
Recommended Operating Condition

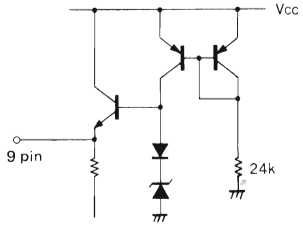
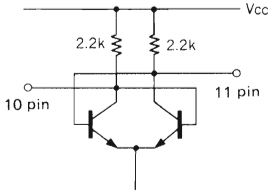
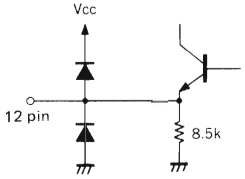
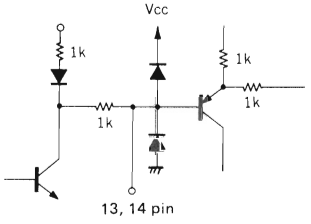
• Supply voltage	V_{CC}	9 ±0.3	V

Block Diagram



Pin Description

No.	Symbol	Equivalent circuit	*1 Pin voltage or current	Impedance	Description
1 2	IF IN1 IF IN2		3.4V	1kΩ 3pF	IF signal input pin. It is coupled with a capacitor when signal is input.
3	GND	GND pin	—	—	GND pin
4	AGC		0V	1.6kΩ	AGC filter pin. Connect a capacitor between this pin and GND. VCO control sensitivity: 1.7V with one condition in the Electrical characteristics measuring circuit diagram.
5	EXT IN		1μA	4MΩ	False synchronous detection signal input pin. It is directly connected to pin 20 of CX20014A/15A. Recommended apply voltage: 3 to 5V
6	SW		8.8V	82kΩ	The synchronous detection and false detection can be switched forcibly. Normally connect a capacitor between this pin and GND.
7	DET OUT		5.4V	10Ω	Video detection output pin

No.	Symbol	Equivalent circuit	*1 Pin voltage or current	Impedance	Description
8	Vcc	Power supply pin	25mA	—	Power supply pin
9	REG		6.7V	30Ω	Connect a capacitor between this and GND. Filter pin for internal power supply
10	VCO1		4.8V	2.2kΩ	Parallel resonance circuit connection pin for VCO.
11	VCO2				
12	AMP OUT		2.7V	80Ω	Control voltage output pin for VCO.
13	FILTER1		7.6V	2kΩ	Loop filter connection pin for PLL
14	FILTER2				

*1: See the DC Characteristics Test Circuit

Electrical Characteristics

(Ta=25°C, V_{CC}=9V See the Electrical Characteristics Test Circuit)

No.	Item	Symbol	Test condition				Test point	Min.	Typ.	Max.	Unit	Remark
			Signal	Level	Input point	ON-SW						
1	Top sync output level	Vsync	58.75MHz CW	−13dBm	IN 1	S2-B	A	2.90	3.20	3.50	V	
2	Video output signal	Vdet	58.75MHz 15.75kHz 87.5% TV AM	−11dBm	IN 1	S2-B	A	1.60	1.95	2.40	V	A standard input which specifies the voltage at the test point B as V1
3	Minimum IF input	IFmin	58.75MHz 15.75kHz 87.5% TV AM	−17dBm	IN 1	S2-B	A	1.60	1.95	—	V	
4	Maximum IF input	IFmax	58.75MHz 15.75kHz 87.5% TV AM	−8dBm	IN 1	S2-B	A	—	2.25	2.70	V	
5	Detection output distortion ratio	Vdet THD	58.75MHz 15.75kHz 87.5% TV AM	−8dBm	IN 1	S2-B	A	—	0.6	6.0	%	Measure the distortion ratio of 15.75kHz
6	ANC insertion level	V_{ANC}	58.75MHz CW	−7dBm	IN 1	S2-B	A	4.10	4.73	5.30	V	
7	VCO control sensitivity 1	VCO1	58.75MHz 15.75kHz 87.5% TV AM	−11dBm	IN 1	S2-C	B	0.6	1.0	2.00	MHz/V	Specifies the voltage at point B as V2. The output waveform at point A is 15.75kHz CW approx. 2Vp-p, VCO1=$(V2-V1)^{-1}$

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No.	Item	Symbol	Test condition				Test point	Min.	Typ.	Max.	Unit	Remark
			Signal	Level	Input point	ON-SW						
8	VCO control sensitivity 2	VCO2	58.75MHz 15.75kHz 87.5% TV AM	−11dBm	IN 1	S2-A	B	0.6	1.0	1.4	MHz/V	Specifies the voltage at point B as V3. The output waveform at point A is 15.75kHz CW approx. 2Vp-p, $VCO2=(V1-V3)^{-1}$
9	Isolation 1	ISO1	58.75MHz CW	−13dBm	IN 1	S1 S2-C S3	A	—	1.7	15	mVp-p	Measure the frequency components between frequency difference of 58.75MHz and VCO oscillation.
10	Isolation 2	ISO2	58.75MHz CW 15.75kHz CW	−13dBm 2Vp-p	IN 1 IN 2	S2-B	A	—	—	15	mVp-p	Measure the frequency components of 15.75kHz
11	SW Loss	Lsw	58.75MHz CW 15.75kHz CW	−13dBm 2Vp-p	IN 1 IN 2	S1 S2-A	A	1.70	1.94	2.20	Vp-p	Measure 15.75kHz CW
12	VCO non-signal DC	V_{IN}	—	—	—	S2-B	B	1.80	2.66	3.6	V	
13	Stabilized voltage	Vz	58.75MHz 15.75kHz 87.5% TV AM	−11dBm	IN 1	S1 S3 S2-B	C	6.00	6.70	7.50	V	
14	Power consumption	Icc	58.75MHz 15.75kHz 87.5% TV AM	−11dBm	IN 1	S1 S2-B	D	18	25	33	mA	Measure the current which flows through E1.

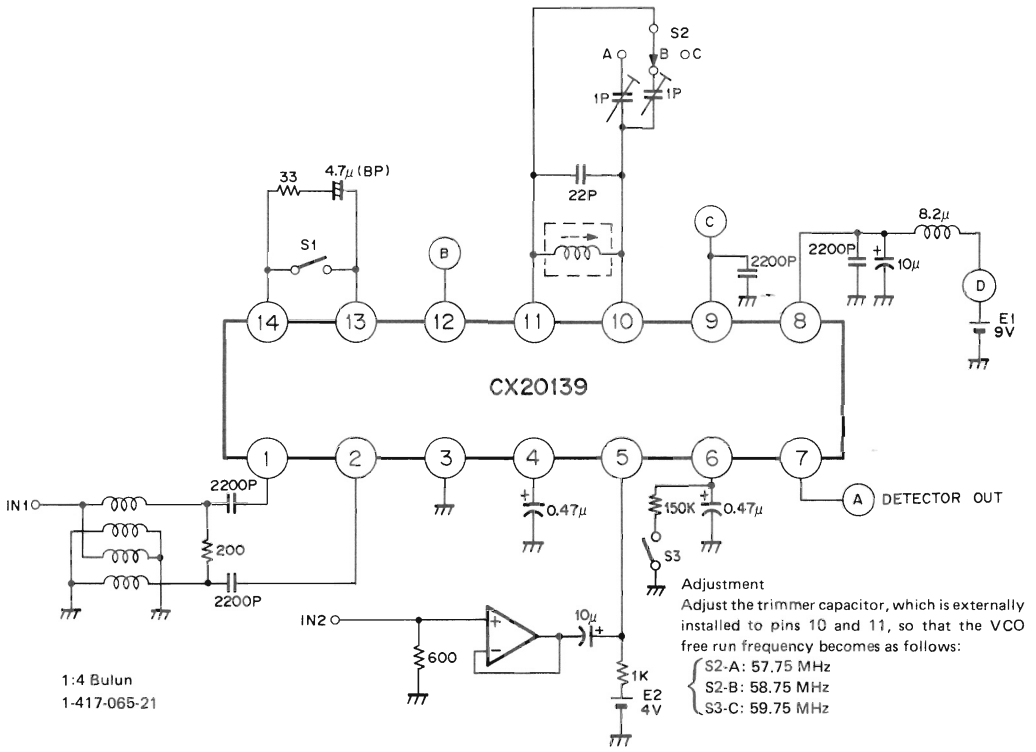
Supplement

1) The input signal levels of 58.75 MHz, 15.75 kHz and 87.5% TV AM are peak values of the evelop curve. (50Ω terminated)
2) Turn the switches S2-A, S2-B and S2-C ON prior to input of the signal.

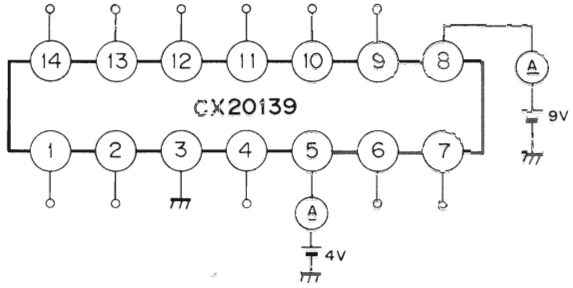
Description of Operation
(Block Diagram and Electrical Characteristics Test Circuit)

An IF signal is input to pins 1 and 2. Then, the VCO free run frequency and the input IF signal are phase compared, and the VCO is locked to the VIF signal by the PLL loop. The locked VCO output and the input signal are synchronously detected and the video detection signal is output from pin 7. An AGC circuit is added to the synchronous detection circuit. When abnormal IF frequency or level fluctuation occur and the loop lock of the PLL becomes free, "BEAT Det" is detected. Switch the "SW" to the "EXT IN" side and thus false synchronous detection signal is output from pin 7. When the PLL loop is reversed, the "SW" is switched and it becomes into synchronous detection output circuit. The "ANC" cancels the black side noise of the video signal and the "WNL" suppresses the white side noise and mitigates blurring of the TV image due to transitional noise mixing into it. In addition to above, as shown in the application circuit example, connect a resistance between pin 6 and GND, it becomes possible to be switched forcibly to the false synchronous detection.

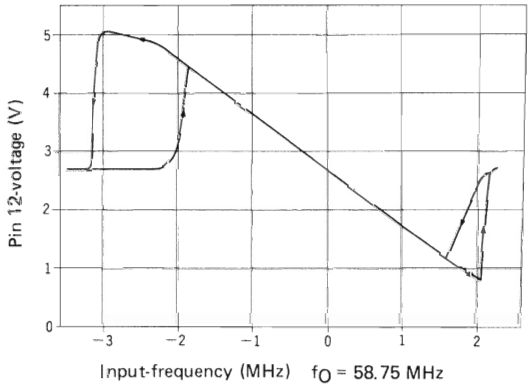
Electrical Characteristics Test Circuit



DC Characteristics Test Circuit

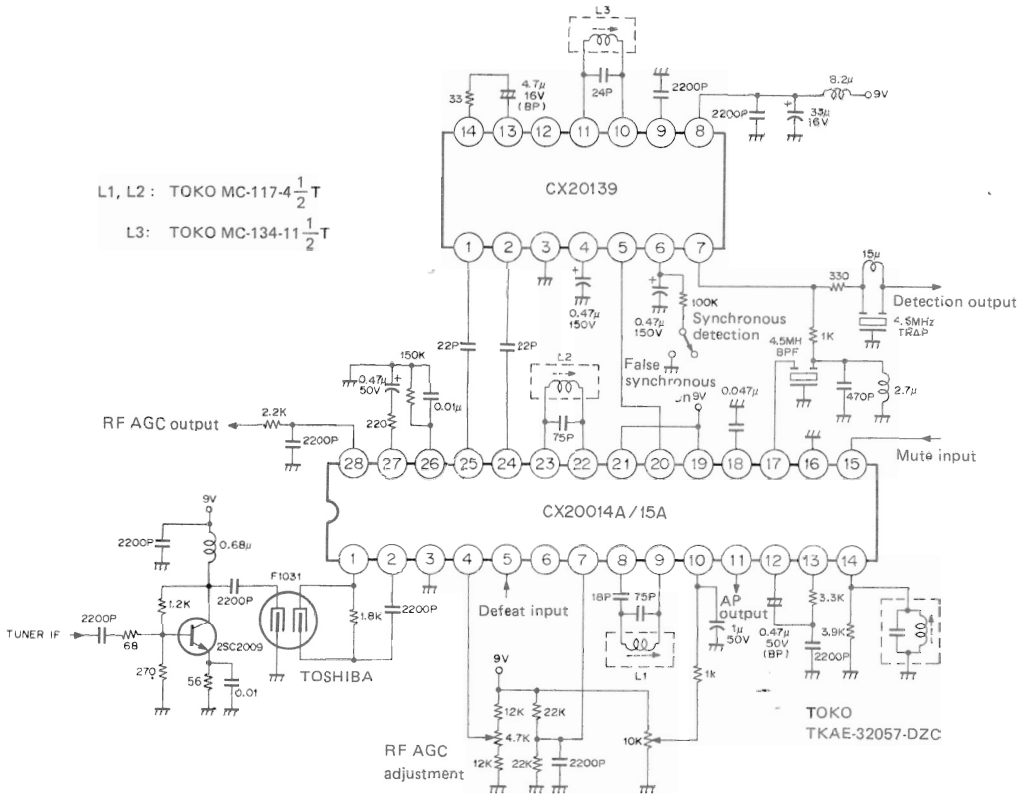


VCO Control Voltage Characteristics



Test condition
Vary the input signal frequency under the same conditions as those of item 2 of the Electrical Characteristics (Det AC level).

Application Circuit



CATV and VHF TV Tuner

Description

The CX20155 is a silicon monolithic bipolar IC which has been developed for CATV and VHF television tuner, and is composed of local oscillator, mixer, IF amplifier, UIF amplifier, VHF/UIF change-over switch, and constant inpedance output circuit.

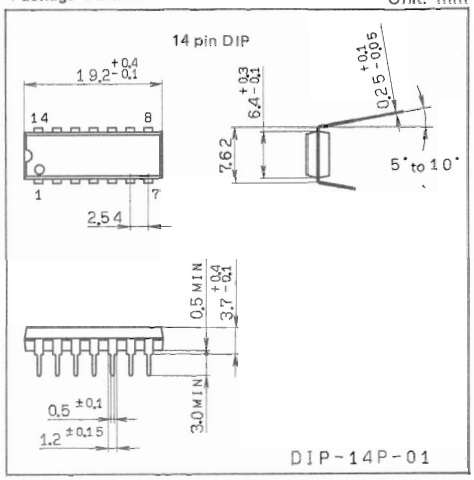
The local oscillator is composed of the differential type and operates stably against change in temperature and power supply voltage.

The mixer can obtain a flat conversion gain in a wide band, and IF stage possesses a wide band characteristics, and is unnecessary to perform adjustment.

The constant impedance output circuit can obtain excellent V.SWR and has the advantage of enabling easy connection to the next stage operating frequency Band is 55 to 440 MHz.

Package Outline

Unit: mm



Function

- Local oscillator, mixer, IF amplifier and UIF amplifier
- VHF/UIF change-over switch and constant impedance IF output amplifier

Structure

Bipolar silicon monolithic IC

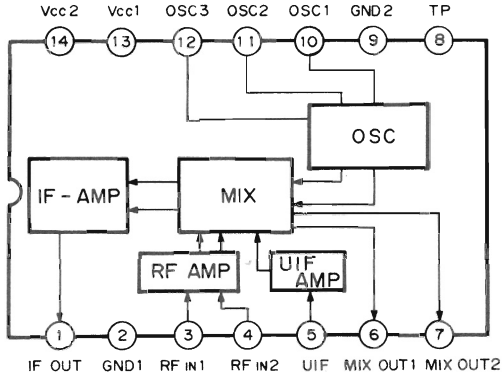
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	$V_{CC}1$, $V_{CC}2$	7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	0.8	W

Recommended Operating Condition

• Supply voltage	4.75 to 5.3	V

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	Symbol	Description	DC voltage (V)
1	IF OUT	IF signal Output	2.5
2	GND1	IF System Ground	0
3	RF IN1	RF Input 1	2.0
4	RF IN2	RF Input 2	2.0
5	UIF IN/SW	When Tuner Receiver SW is off When UHF Receiver SW is on and UIF input signal	OFF 0.0 ON 5.0
6	MIX OUT1	Mixer IF output 1	4.0
7	MIX OUT2	Mixer IF output 2	4.0
8	TP	Test Point	2.9
9	GND2	Oscillator, Mixer, RF system ground	0
10	OSC1	External Oscillator Tank circuit output 1	2.4
11	OSC2	External Oscillator Tank circuit output 2	2.4
12	OSC3	External Oscillator Tank circuit output 3	5
13	$V_{CC}1$	Oscillator, Mixer, RF system power supply	5
14	$V_{CC}2$	IF Amp, UIF Amp system power supply	5

Note) Since terminal number 12 is open collector, it connects the RF system power supply through the choke coil.

Electrical Characteristics

AC characteristics (Ta=25°C, $V_{CC}1$, $V_{CC}2$=5V)
See Test circuit Fig. 1 to 4

Measuring Item	Symbol	Condition		Min.	Typ.	Max.	Unit
IF Power gain PG	PG	f_{UIF}=43.5MHz	Fig. 1	30	34	37	dB
RF Conversion gain CG1	CG1	f_{RF}=55MHz	Fig. 2	23	28	32	dB
RF Conversion gain CG2	CG2	f_{RF}=200MHz	Fig. 2	22	27	31	dB
RF Conversion gain CG3	CG3	f_{RF}=440MHz	Fig. 3	20	24	28	dB
UIF Noise Figure 1 NF1	NF1	f_{UIF}=43.5MHz	Fig. 1		5.0	6.5	dB
RF Noise Figure 2 NF2	NF2	f_{RF}=200MHz	Fig. 2		11.5	14.0	dB
RF Noise Figure 3 NF3	NF3	f_{RF}=440MHz	Fig. 3		13.5	15.0	dB
Local Oscillator starting power supply voltage	Vosc	Vc varicap=30V	Fig. 4			3.5	V

DC characteristics (Ta=25°C, $V_{CC}1$, $V_{CC}2$=5V)
See Test circuit Fig. 5.

Measuring Item	Symbol	Condition	Min.	Typ.	Max.	Unit
DC supply current 1	I_D1	SW OFF	40	46	58	mA
DC supply current 2	I_D2	SW ON	35	44	52	mA

Terminal DC voltage
See Test circuit Fig. 5.

Measuring Item / No.	Condition	Typ.	Unit	Condition	Typ.	Unit
1	SW OFF	2.5	V	SW ON	2.7	V
3	SW OFF	2.0	V	SW ON	0.0	V
4	SW OFF	2.0	V	SW ON	0.0	V
6	SW OFF	4.0	V	SW ON	5.0	V
7	SW OFF	4.0	V	SW ON	3.8	V
8	SW OFF	2.9	V	SW ON	2.8	V
10	SW OFF	2.4	V	SW ON	1.2	V
11	SW OFF	2.4	V	SW ON	1.2	V

(Ta=25°C, Vcc1, Vcc2=5V)

Standard Circuit Design Data

See Test circuit Fig. 4 to10

Measuring Item	Symbol	Condition	Typ.	Unit
UIF Power gain deviation	ΔPG	f_S=41.25 f_P=45.75MHz (Fig. 7)	0.3	dB
UIF Input impedance	r_{uip}	f=45.75MHz Input level −30dBm (Fig. 7)	800	Ω
	C_{uip}		8	pF
RF Input impedance	r_{ip}	f=450MHz Input level −30dBm (Fig. 9)	700	Ω
	C_{ip}		3.2	pF
IF Output voltage standing wave Ratio	VSWR	f=43.5MHz Input level −30dBm (Fig. 10)	1.5	
1% Cross Modulation distortion 1 (UIF)	CM1	f_{Des}=45.75MHz f_{Undes}=f_{Des}±12MHz (Fig. 7)	84	dBμ
1% Cross Modulation distortion 2 (RF)	CM2	f_{Des}=55MHz f_{Undes}=f_{Des}±12MHz, 1kHz 40% AM (Fig. 6)	88	dBμ
1% Cross Modulation distortion 3 (RF)	CM3	f_{Des}=200MHz f_{Undes}=f_{Des}±12MHz (Fig. 6)	94	dBμ
1% Cross Modulation distortion 4 (RF)	CM4	f_{Des}=440MHz f_{Undes}=f_{Des}±12MHz (Fig. 6)	97	dBμ
IF maximum output power	V_{OMax}	f_P=58.75MHz, f_S=54.25MHz f_C=55.17MHz 1) (Fig. 7)	−1.5	dBm
Local oscillator power leakage at RF output	V_{RFOSC}	fosc=100 to 480MHz (Fig. 8)	−26	dBm
Local osillator power leakage at If output	V_{IFOSC}	fosc=100 to 480MHz (Fig. 8)	−15	dBm
Local oscillator frequency Stability	fstb	fosc=100 to 480MHz Vcc±5% (Fig. 4)	±500	kHz
Local oscillator frequency starting drift	fdrif	fosc=100 to 480MHz 2) (Fig. 4)	±200	kHz

Note 1) Input level

f_P: −41 dBm, f_S: −42.7 dBm, f_C: −53 dBm

f_{IFP} level − f_{IFS} Beat level ≧ 40 dB

2) From 3s to 3 min after switching on.

Electrical Characteristics Test Circuits

AC test circuits

UIF power gain, Noise figure

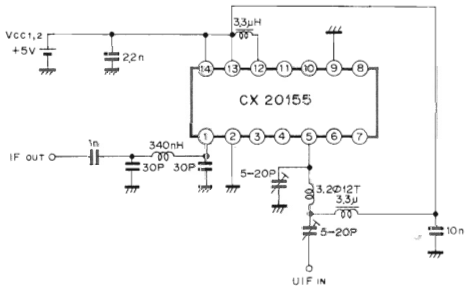
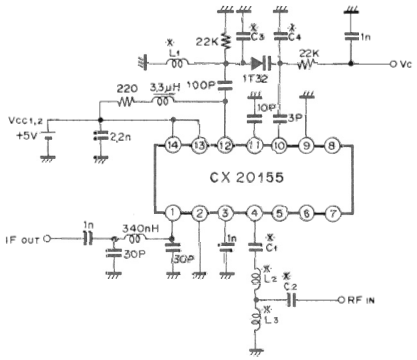


Fig. 1

RF conversion gain, Noise figure (f=55,200 MHz)



Parts List

Parts No. / frequency (MHz)	C_1	C_2	C_3	C_4	L_1	L_2	L_3
55	33P	4.7n	–	33P	3.2φ 12T	3.2φ 30T	3.2φ 10T
200	22P	4.7n	7P	5P	3.0φ 2.5T	3.2φ 8T	3.2φ 3.5T

※ C_1 to C_4, L_1 to L_3 See Parts List

Fig. 2

RF conversion gain, Noise figure (f=440 MHz)

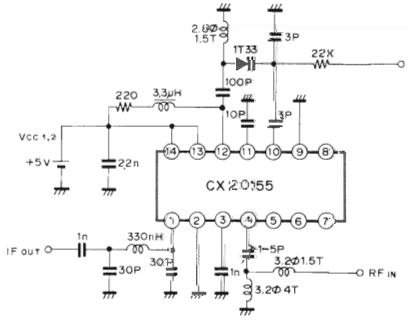


Fig. 3

Local oscillator starting supply voltage, Stability, Starting drift

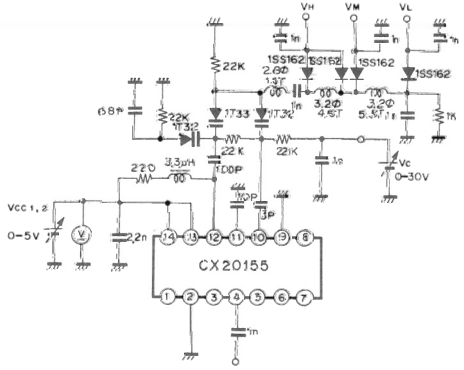
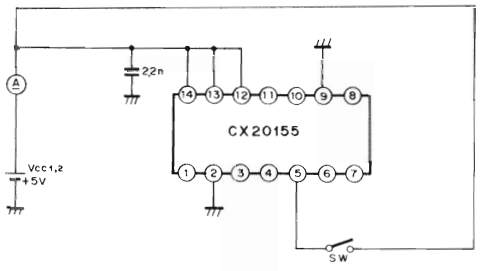


Fig. 4

DC test circuit

Consumption current measuring circuit

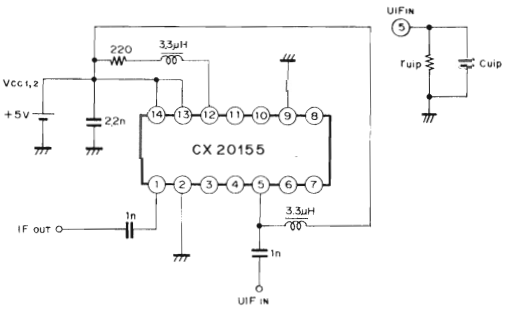


Note) When UIF receiver sw is on.

Fig. 5

1% UIF cross modulation, UIF power gain deviation, UIF input impedance

IF maximum output voltage measuring circuit



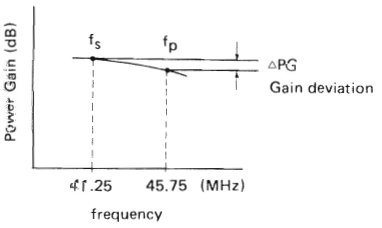
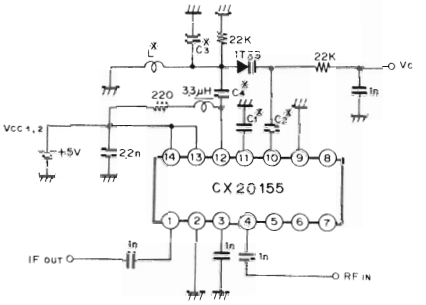


Fig. 7

Cross modulation (f=55,200, 440 MHz)



Parts List

Parts number / frequency (MHz)	C_1	C_2	C_3	C_4	L
55	33P	10P	–	100P	3.2 φ 11T
200	100P	10P	7P	5P	3.2 φ 3T
440	20P	2P	–	1P	2.8 φ 2.5T

※ C_1 to C_4, L See Parts List

Fig. 6

RF, IF local oscillator power leakage

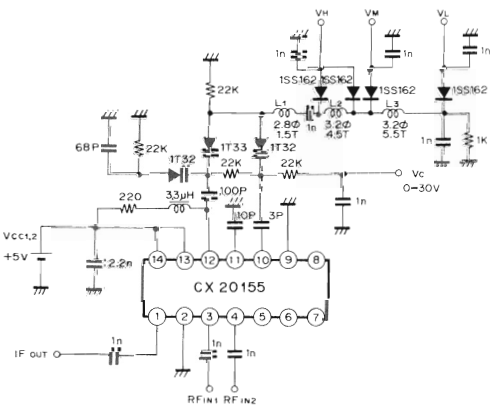


Fig. 8

Mixer (RF) input impedance.

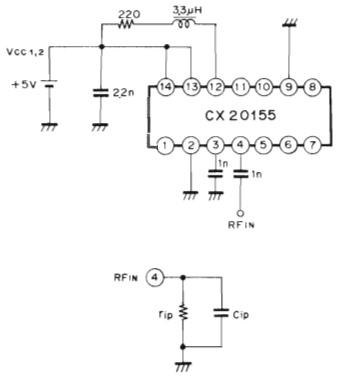


Fig. 9

IF output VSWR

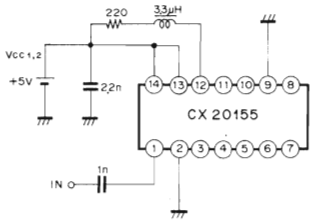


Fig. 10

Description of Operation (See Application Circuit)

Number ⑬ and ⑭ are Pins for power supply. As pin ⑫ , is an open collector, insert choke coil and resister (100 to 200 ohm) in series and connect to power supply.

(a) Oscillator circuit
Tank circuit consist of pin ⑩ and ⑫ to connect through the capacitor.
The oscillating frequency selects each band by change-over of coil and, in addition, varies the voltage of the variable capacitor diode and by varying the resonance of the tank circuit, enables the variation of oscillating frequencies.

(b) Input circuit
Feed RF signal of input into pins ③ and ④ . The range of the frequencies of the input signal is 55 to 440 MHz, and the level is approximately −50dBm. There are two systems in which either one of pins ③ or ④ is used, and the balance input in which the simultaneous use of pins ③ and ④ is performed.

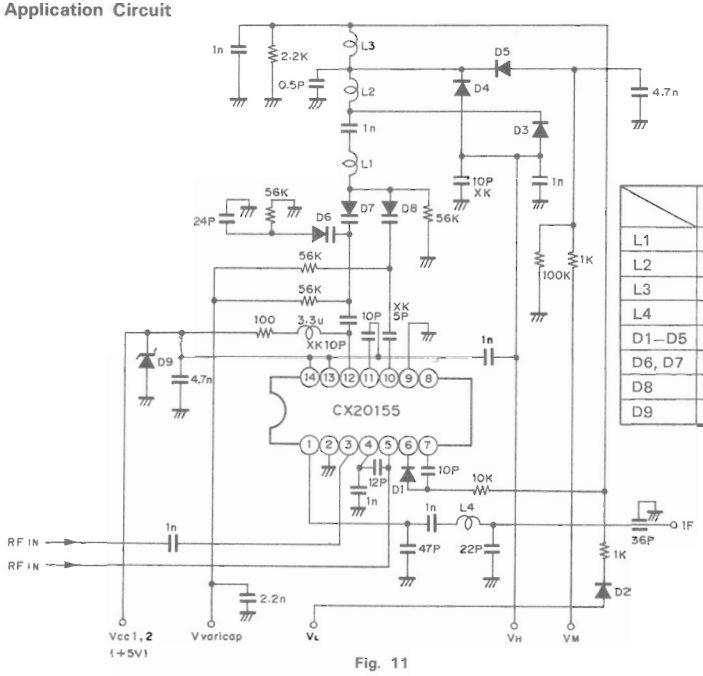
(c) Mixer circuit
The RF signal in which pins ③ and ④ have been fed is converted to IF signal by the mixer, and the IF signal take up to ⑥ and ⑦ .

(d) IF circuit
The IF signal is amplified and can be take from pin ① .
The output impedance is 75Ω. The output 1 dB compression level is +8dBm.

(e) UIF circuit
The signal (UIF signal) which has been converted to IF from the UHF system is fed to pin ⑤ and amplified, and is taken from pin ① . By applying UIF signal and DC voltage of 5V simultaneously to pin ⑤ , during receiving of UHF, it operates as an IF amplifier.

(f) Figure 13, 14 shows following conditions.
Frequency characteristics of RF input impedance and frequency characteristics of UIF input impedance.

Application Circuit



	Line diameter (mm)	Coil diameter (mm)	Number of turns (turn)
L1	0.5	2.2	2.5
L2	0.45	2.8	4.5
L3	0.4	2.6	7.5
L4	0.35	3.2	8.5
D1–D5	1SS162		
D6, D7	1T33		
D8	1T32		
D9	RD6.2		

Fig. 11

Pattern Layout (Component Side)

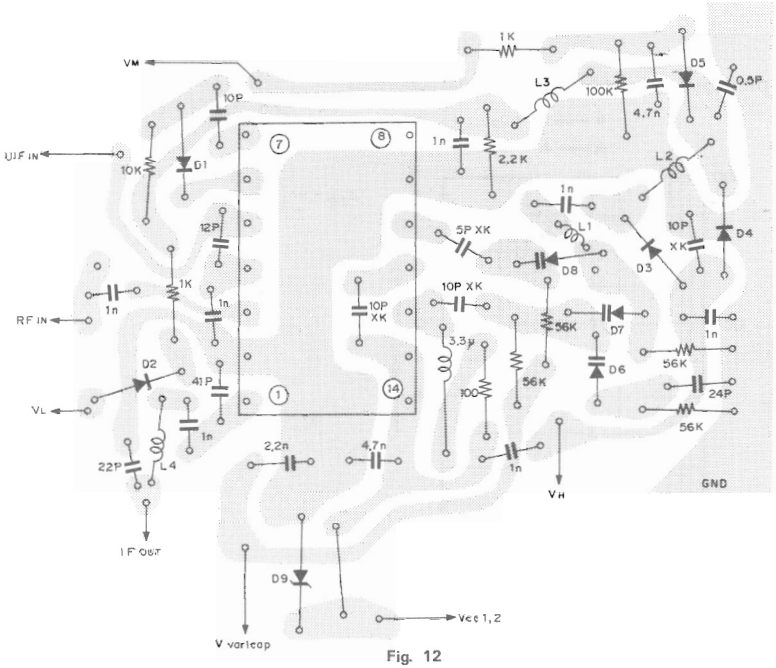
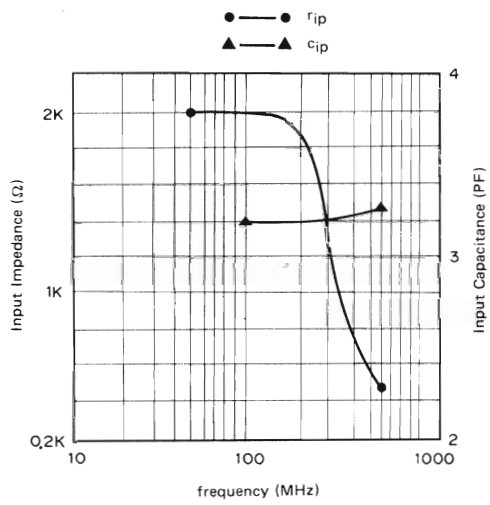


Fig. 12

RF input impedance frequency characteristics



$r_{ip} = Re\left(\frac{1}{Y_{11}}\right)$

$c_{ip} = Im\left(\frac{1}{Y_{11}}\right)$

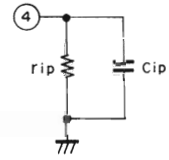
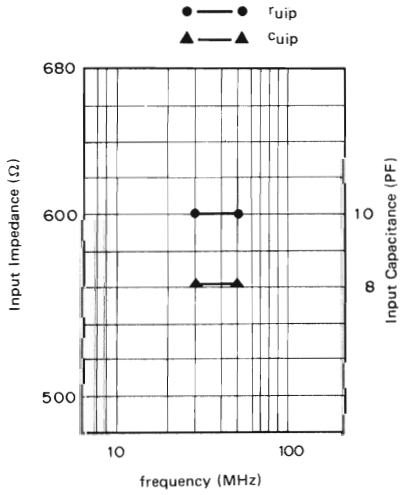


Fig. 13

UIF input impedance frequency characteristics



$r_{uip} = Re\left(\frac{1}{Y_{11}}\right)$

$c_{uip} = Im\left(\frac{1}{Y_{11}}\right)$

Fig. 14

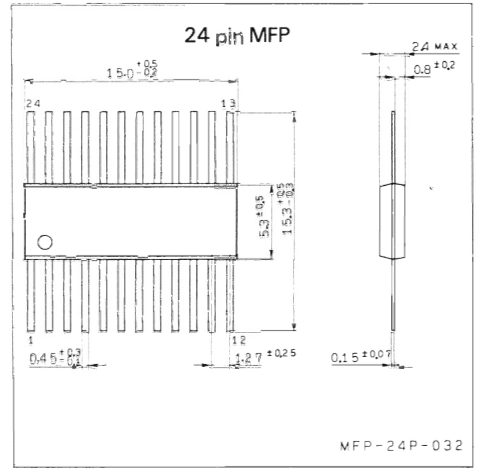
Television Picture Signal Processor IC

Description

The CX20183 is one-chip IC dedicated for use in a small portable television set, in which VIF and SIF circuits are integrated. It is designed for use with a battery power source to realize low current consumption.

Package Outline

Unit: mm



Features

- Operating supply voltage 3 to 6 V
- Current consumption 16 mA
- VIF detector AFT incorporated
- SIF quadrature detection system
- Built-in SIF electronic volume
- Built-in synchronous separation circuit

Functions

Picture IF amplification, picture detection, IF AGC, RF AGC, AFT IF amplification, limiter, FM detection, synchronous separation, ATT

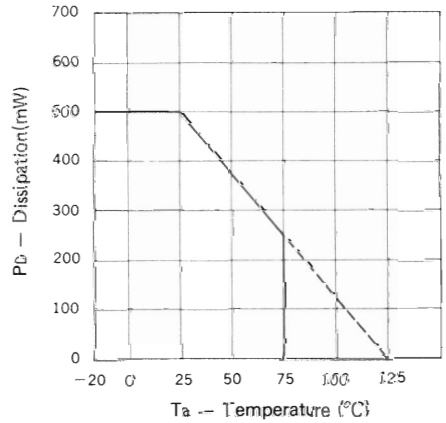
Structure

Bipolar silicon monolithic IC

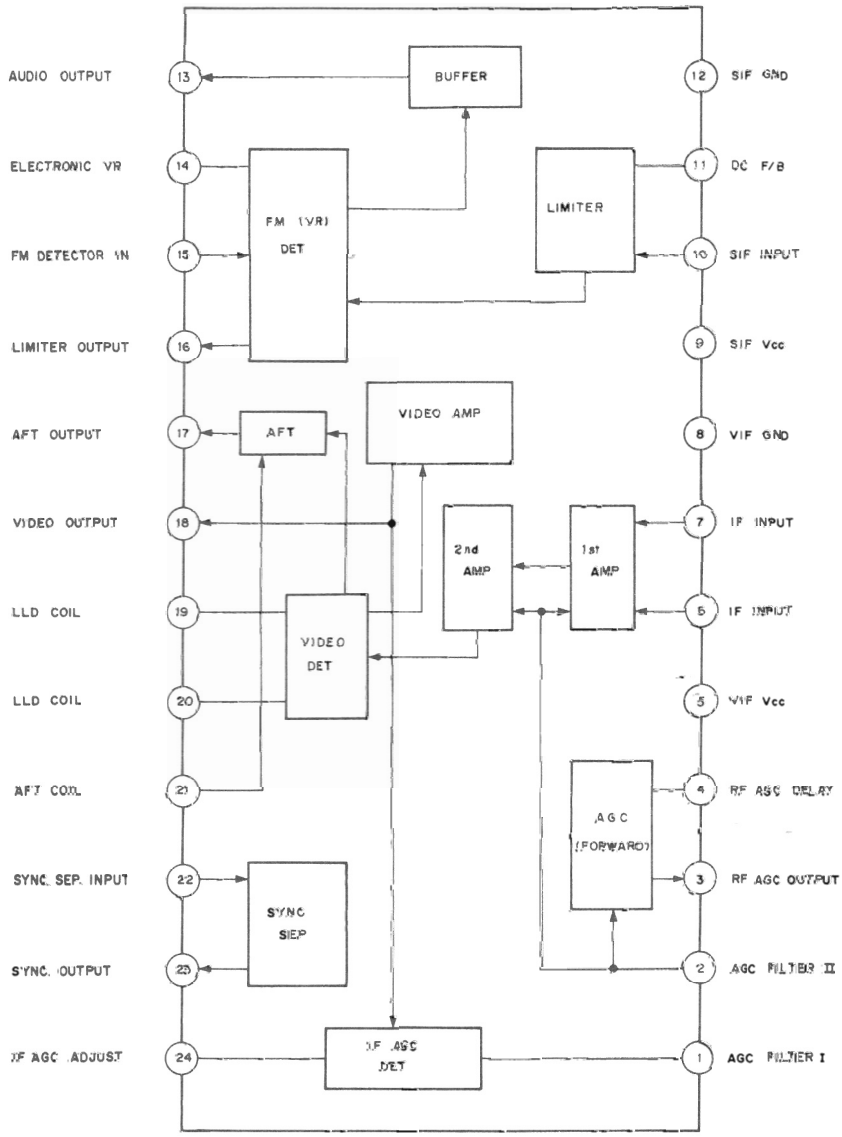
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage 1	V_{CC} (Pin 5)	7.5	V
• Supply voltage 2	V_{CC} (Pin 9)	7.5	V
• Operating temperature	T_{opr}	−20 to +75	°C
• Storage temperature	T_{stg}	−40 to +125	°C
• Allowable power dissipation	P_D	500	mW

Declining Curve of Allowable Power Dissipation



Block Diagram and Pin Configuration



Electrical Characteristics

VIF Characteristics

See the AC test circuit for test points.

No.	Item	Symbol	Test point	Input VIF	Conditions and method	Min.	Typ.	Max.	Unit
1	Circuit current	I_{VIF}	5	SG1 90 dBμ	Incoming current for 4.5 V at Pin 5	10	13.5	17	mA
2	Video detection output	V_o	18	SG1 90 dBμ	Output amplitude	0.8	0.9	1.1	Vp-p
3	Input sensitivity	Vimin	18	SG1 Variable	Input level for the output amplitude 3 dB lower than Vo.		50	55	dBμ
4	Maximum allowable input	Vimax	18	SG1 Variable	Input level for the output amplitude 3 dB higher than Vo.	105	114		dBμ
5	Video frequency characteristics	BW	18	SG2	See Note 1	6	7		MHz
6	Differential gain	DG	18	SG3 90 dBμ	LLD coil is adjusted at 58.4 MHz, the resultant value is measured with an NTSC vectorscope.		7	10	%
7	Differential phase	DP	18	SG3 90 dBμ			3	8	deg
8	Video S/N	S/N	18	SG4 90 dBμ	S/N = 20 log (V_{op-p}/V_N rms); where V_N is output amplitude	50	56		dB
9	Video distortion factor	THD	18	SG1 90 dBμ	Measured with a distortion gauge		3.3	10	%
10	Inter-modulation	I_M	18	SG5	I_M = 20 log (920 kHz beat/3.58 MHz output)		−38	−30	dB
11	Carrier leak	Lfc	18	SG1 90 dBμ	58.75 MHz component		71	80	dBμ
12	Output impedance	Ro	18	SG1 90 dBμ	See Note 2	50	95	150	Ω
13	RF AGC maximum voltage	V_{3H}	3	SG4 90 dBμ	DC voltage for 4.2 V at Pin 4	3.5	3.7	4.1	V
14	RF AGC minimum voltage	V_{3L}	3	SG4 90 dBμ	DC voltage for 2 V at Pin 4	0	0	0.1	V
15	RF AGC gain	GARF	3		See Note 3	40	50	80	dB
16	IF AGC maximum voltage	V_{IH}	1		Output voltage for grounding of Pin 24	4.1	4.3	4.5	V
17	IF AGC minimum voltage	V_{IL}	1		Output voltage for 4.5 V at Pin 24	0.3	0.7	0.9	V
18	IF AGC gain	V_{AIF}	1		See Note 4	40	50	80	dB
19	AFT detection sensitivity	μ	17	SG6 90 dBμ	See Note 5	40	50	65	mV/KHz
20	AFT mute voltage	V_A	17	SG1 90 dBμ	DC output voltage for 0 V at Pin 21	2	2.25	2.5	V
21	AFT center voltage	V_{AC}	17		DC output voltage for 0 V at Pin 2	0.7	1.4	2.1	V
22	AFT maximum voltage	V_{AH}	17	SG6 90 dBμ	High level output voltage	4.3	4.4	4.5	V

No.	Item	Symbol	Test point	Input VIF	Conditions and method	Min.	Typ.	Max.	Unit
23	AFT minimum voltage	V_{AL}	17	SG6 90 dBμ	Low level output voltage	0	0	0.1	V
24	AFT drift	△fd	17	SG6 90 dBμ	Frequency difference appears for 2.25 V at Pin 17 when ambient temperature varies between −20°C and 75°C △fd = f(−20°C) − f(75°C)	100	200	300	KHz
25	Input resistance	Rin	6, 7		See Note 6	1.8	2.6	3.4	kΩ
26	Input capacitance	Cin	6, 7		See Note 6	0.5	1.1	1.7	pF

SIF Characteristics

No.	Item	Symbol	Test point	Input SIF	Conditions and method	Min.	Typ.	Max.	Unit
1	Circuit current	I_{SIF}	9		Incoming current for 4.5 V at Pin 9	2.0	2.8	3.6	mA
2	Detection output voltage	V_{OAF}	13′	SG7 90 dBμ	Output amplitude	220	270	320	mVrms
3	Input limiting sensitivity	Vimin	13′	SG7 Variable	Lowered input level to cause the output 3 dB lower than Vo AF		35	49	dBμ
4	AM suppression ratio	AMR	13′	SG8 90 dBμ	$AMR = 20 \log \frac{V_{OAF}\ (mVrms)}{V_{AH}\ (mVrms)}$; where V_{AM} is output amplitude	40	60		dB
5	Band width	BW(s)	13′	SG9 90 DBμ	See Note 7	100	130		kHz
6	Electronic volume characteristics	VR1	13′	SG7 90 dBμ	The ratio of output amplitude and V_{OAF} when voltage at Pin 14 is varied at 4 V → 2.25 → 1 V VR = 20 log (output amplitude/ V_{OAF}	3.3	3.75	4.2	dB
		VR2				−0.6	−0.2	0.2	
		VR3					−63	−52	
7	Total harmonic distortion factor	THD	13′	SG10 90 dBμ	Measured with a distortion gauge		0.8	1.2	%
8	Increase/decrease voltage, detector output voltage	V_{OHAF}	13′	SG7 90 dBμ	Output amplitude for 5V or 3 V at Pin 9	380	430	480	mVrms
		V_{OLAF}				53	64	75	
9	Noise level	V_N	13′		Output amplitude		4	6	mVrms

Other Characteristics

No.	Item	Symbol	Test point	Input	Conditions and method	Min.	Typ.	Max.	Unit
1	Synchronous separation output	Vosync	23	SG1 90 dBμ	Output amplitude	3.5	3.7	4.0	Vp-p
2	Synchronous separation voltage	Visync	22		Voltage at Pin 22 when 0.1 mA is sent from this pin	3.3	3.5	3.7	V
3	Operating voltage	VminVIF	18	SG1 90 dBμ	Confirm that an output appears when 3 V is applied to Pin 5	3			V
4	Operating voltage	VminSIF	13	SG7 90 dBμ	Confirm that an output appears when 3 V is applied to Pin 9	3			V

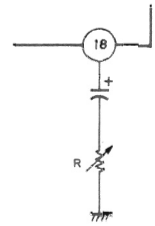
Note 1) Video frequency characteristics "BW"

Apply voltage at Pin 2 to adjust the output amplitude to 0.1 Vp-p for $f_1 - f_2 = 1$ MHz. BW is specified as $f_1 - f_2$ which appears when the output amplitude is 3 dB lower than 0.1 Vp-p.

2) Output impedance "Ro"

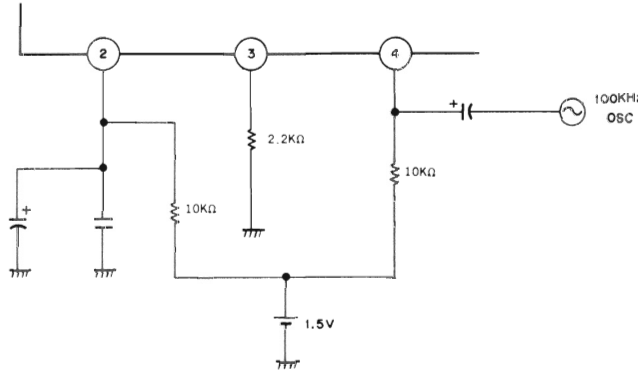
Adjust the modulation factor of SG1 to set the video output to 0.2 Vp-p. Then measure the value of R which gives the output amplitude as 150 mVp-p with the circuit shown below. Output impedance is calculated as follows:

$Ro \simeq R/3$



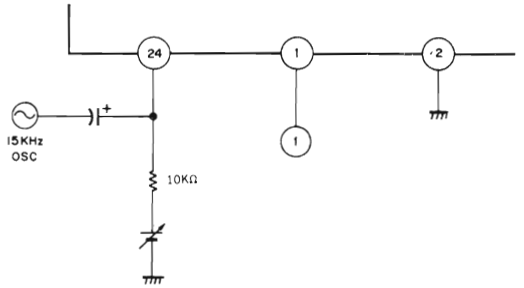
3) RF AGC gain "GARF"

Measure the I/O ratio which causes 0.6 Vp-p output at Pin 3 in the circuit below.



4) IF AGC gain "GAIF"

Measure the I/O ratio which causes 0.6 Vp-p output at Pin 1 in the circuit below.

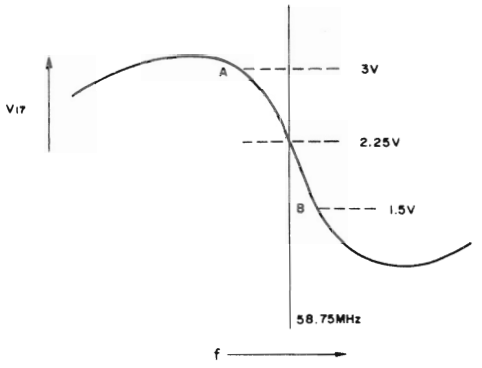


5) AFT detection sensitivity "μ"

This is expressed as

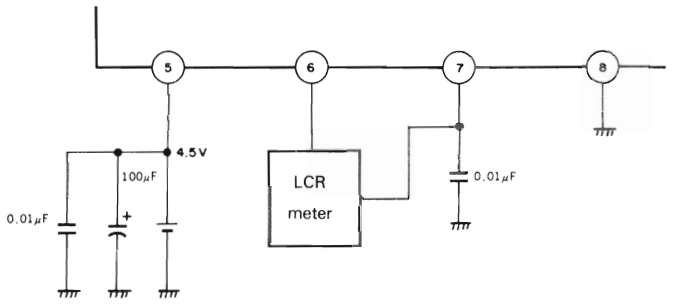
$\mu = 1500\ (mV)/f_B(kHz) - f_A(kHz)$

where f_A and f_B are frequencies at points A and B, respectively.



6) Input resistance and input capacitance, "Rin" and "Cin"

These values are measured using an LCR meter in the circuit below with 58.75 MHz and OSC level at 0.1 vp-p.



7) Band width "BW(s)"

An output amplitude obtained when a signal with f_0 of 4.5 MHz, f_m of 400 Hz and f_{dev} of $\pm$7.5 kHz was applied to SIF IN is specified as $V_{O(DET)}$.

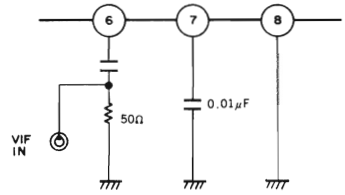
Then f_0 is lowered to obtain the frequency which gives an output amplitude again 3 dB lower than $V_{O(DET)}$, which is defined as f_{OL}. Conversely, f_0 is increased to obtain a frequency which gives an output amplitude again 3 dB lower than $V_{O(DET)}$, which is defined as f_{OH}. Band width is then given in the following equation:

$BW(s) = f_{OH} - f_{OL}$

Notes on AC Characteristics Measurement

1. Supply voltage is usually set to 4.5 V (Pin 5 and 9), unless otherwise specified in the column for conditions. The IC is measured at its socket.

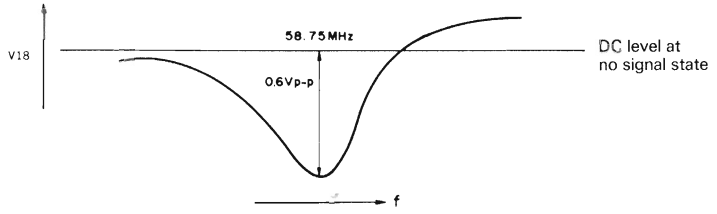
2. VIF input amplitude (V_{in}) is given as the amplitude of VIF IN shown in the circuit below. V_{in} is obtained by measuring DC voltage V_2 at Pin 2 with an input of SG1 90 dBμ in the circuit.



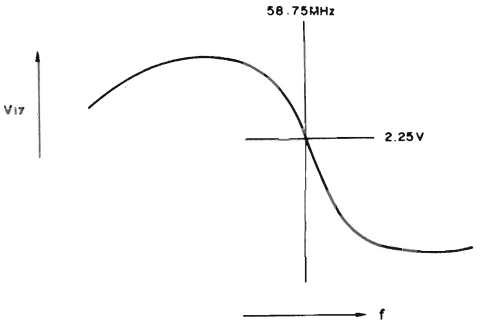
3. Input signals are as follows:

SG1	f_0 = 58.75 MHz	f_m = 20 kHz	77.8%AM	
SG2	f_1 = 58.75 MHz	Vi = 90 dBμ	CW	mixed signal
	f_2 = 53$\pm$5 MHz	Vi = 70 dBμ	CW	mixed signal
SG3	f_0 = 58.75 MHz	LINEARITY 10 step signal		
		87.5% video modulation AM		
SG4	f_0 = 58.75 MHz	CW		
SG5	f_0 = 58.75 MHz	f_1 = 55.17 MHz	f_2 = 54.25 MHz	V_0 = 90 dBμ $V_1 = V_2$ = 80 dBμ (mixed signal)
SG6	f_0 = 58.75 MHz $\pm$5 MHz	CW (sweep)		
SG7	f_0 = 4.5 MHz	FM 25 kHz dev	f_m = 400 Hz	
SG8	f_0 = 4.5 MHz	AM30%	f_m = 400 Hz	
SG9	f_0 = 4.5 MHz $\pm$ 200 kHz	FM 7.5 kHz dev	f_m = 400 Hz	
SG10	f_0 = 4.5 MHz	FM 7.5 kHz dev	f_m = 400 Hz	

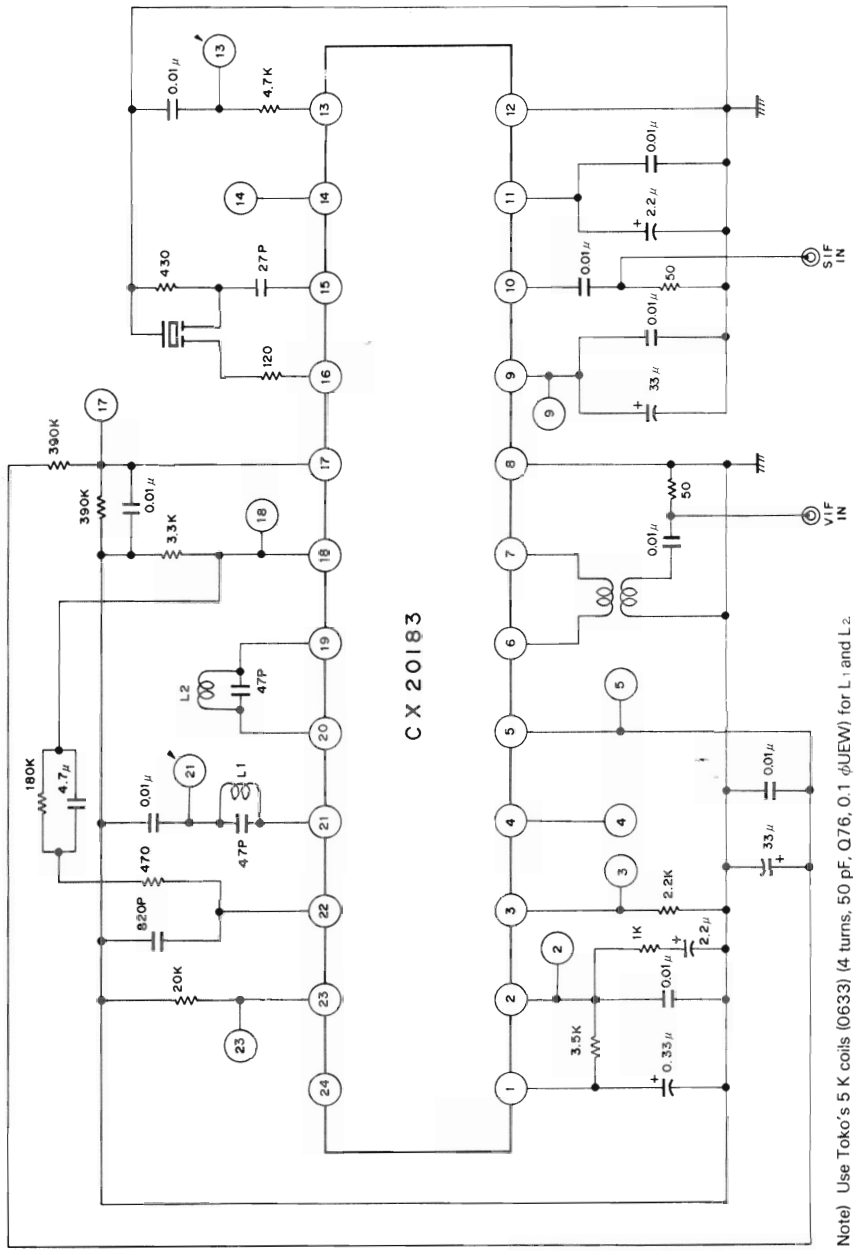
4. Adjusting LLD coil
   1) Input SG6 with Vi = 90 dBμ to VIF IN.
   2) Set the AFT coil inductance with some displacement from 58.75 MHz.
   3) Apply external voltage at Pin 2 and confirm a tank response at Pin 18, as shown below.
   4) Turn the LLD coil to adjust the peak on 58.75 MHz.



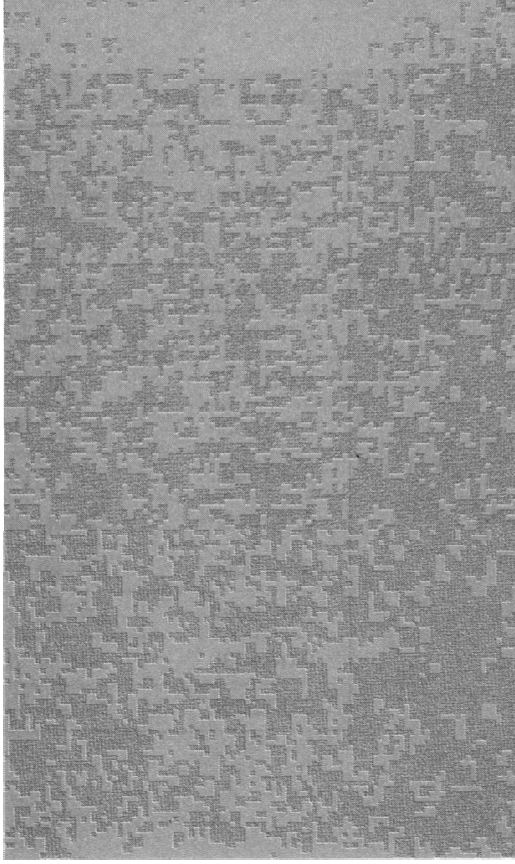
5. AFT coil
   1) Input SG6 with Vi = 90 dBμ to VIF IN.
   2) Turn the AFT coil to so that the output of Pin 17 appears as below.



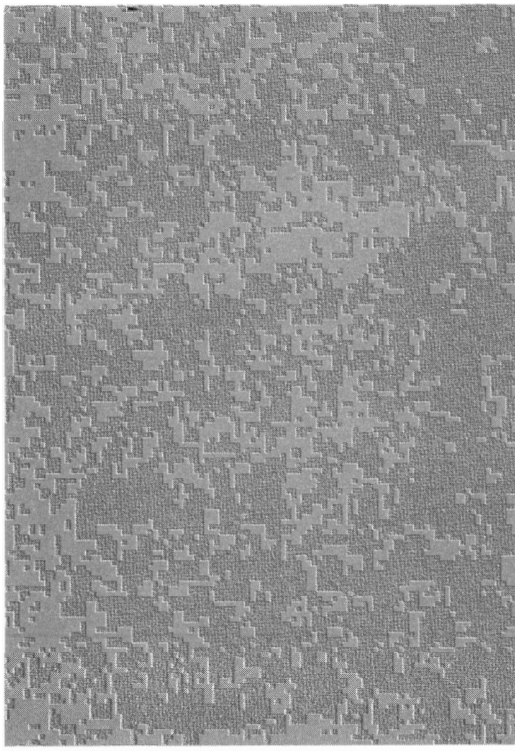
AC Test Circuit



Note) Use Toko's 5 K coils (0633) (4 turns, 50 pF, Q76, 0.1 ϕUEW) for L_1 and L_2.



Tuning System



2) Tuning System

Type	Function	Page
CX-7925B/-1	Frequency Synthesizer PLL	75
CX-7961A/-1	Frequency Synthesizer PLL	86
CX23055/-1	Frequency Synthesizer PLL	97
CXK1001P	640-bit (40 word×16 bit) Non-volatile Memory	108
CXK1002P	560-bit (40 word×14 bit) Non-volatile Memory	118
CXK1003P	320-bit (20 word×16 bit) Non-volatile Memory	128
CXK1004L	512-bit (32 word×16 bit) Non-volatile Memory	138
CXK1005P	512-bit (32 word×16 bit) Non-volatile Memory	144
CXK1006L	1024-bit (64 word×16 bit) Non-volatile Memory (P)	155
CXK1007P	1024-bit (64 word×16 bit) Non-volatile Memory	161
CXK1008L	2048-bit (128 word×16 bit) Non-volatile Memory (P)	172
CXK1009P	2048-bit (128 word×16 bit) Non-volatile Memory	178

(P) : Preliminary

SONY CX-7925B/7925B-1

Frequency Synthesizer PLL

Description

CX-7925B is a PLL IC for the digital selection of AM, FM and TV Broadcasting as well as other radio waves, developed using the high-speed N-channel silicon gate MOS technology.

Features

- The maximum operating frequency is warranted as follows
  CX-7925B Up to 300MHz
  CX-7925B-1 Up to 350MHz
  They can be used up to 1GHz when used combined with an ECL prescaler (general-purpose).
- Programmable divider makes it possible to divide a program frequency up to 1/262,151.
- Programmable reference divider realizes selection of a given reference frequency (e.g. 244Hz–2MHz can be selected when a 4MHz crystal oscillator is used).
- High C/N ratio with the high-speed phase comparator.
- Operation control using three terminals in serial mode.
- Independent 3 terminals (AM1, FM1 and TV1) are provided for a high frequency signal input depending on its frequency band.
- Multi-purpose output terminals are provided (AO, BO).
- Low power consumption (120m W Typ.).

Structure

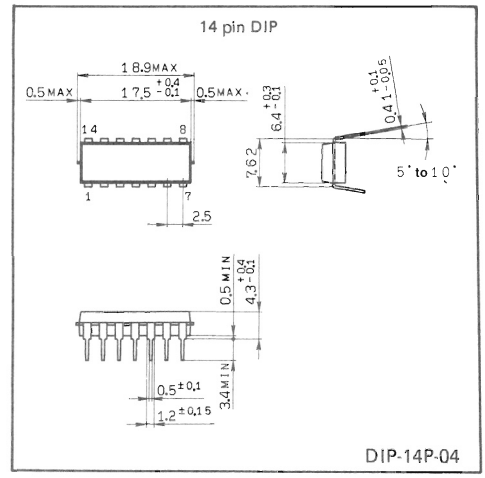
N-channel silicon gate MOS

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

• Supply voltage	V_{DD}	−0.5 to +7	V
• Pin input voltage	V_{IN}	−1 to +7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Package Outline

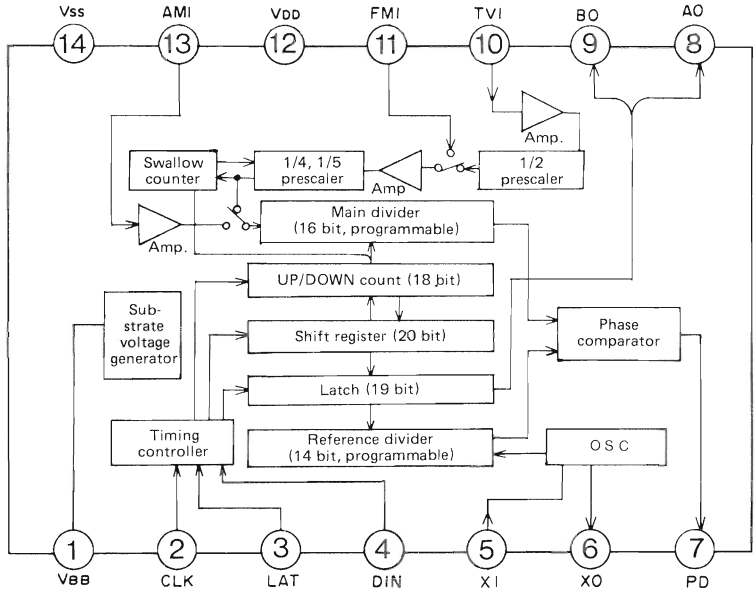
Unit: mm



Recommended Operating Conditions

Item	Pin, remark	Symbol	Operating range	Unit
Supply voltage		V_{DD}	4.5 to 5.5	V
High level input voltage	CLK, DIN	V_{IH}	2.6 to V_{DD} +0.5	V
Low level input voltage	LAT	V_{IL}	−1.0 to 0.8	V
High frequency signal input amplitude	TVI	e_{IN}	0.3 to 4.0	Vp-p
High frequency signal input amplitude	VMI	e_{IN}	0.2 to 4.0	Vp-p
High frequency input amplitude	AMI	e_{IN}	0.2 to 2.5	Vp-p
High frequency input amplitude	XI	e_{IN}	0.6 to 4.0	Vp-p
Operating temperature		Topr	−20 to +70	°C

Block Diagram and Pin Configuration



Pin Description

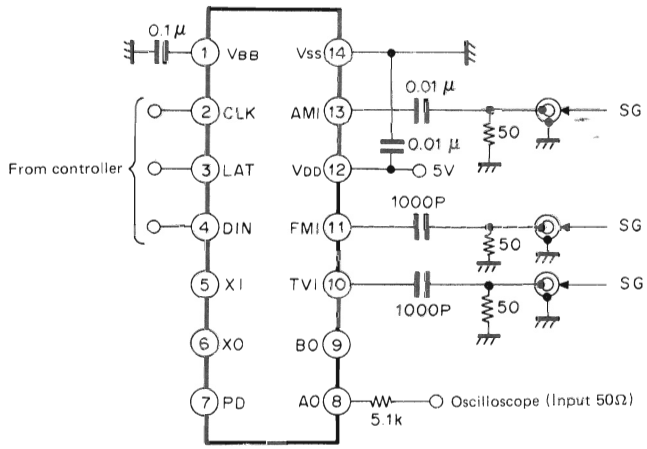
No.	Symbol	Description
1	V_{BB}	Substrate terminal (connect 0.01μF capacitor to the ground)
2	CLK	Clock input terminal for 20-bit serial data input (to be shifted with signal rise)
3	LAT	Latch signal input terminal for shift register input data (to be latched with signal rise) as well as the UP/DOWN clock input terminal (its state to be changed with signal rise)
4	DIN	Data input terminal as well as the UP/DOWN mode switching terminal (UP at "H" level, DOWN at "L" level)
5	XI	Crystal oscillator connection terminal for the reference signal generation (13MHz max., 4.0MHz standard)
6	XO	
7	PD	Phase comparator output terminal (3 states)
8	AO	External control signal output terminal/unlock output terminal (E/E MOS push-pull)
9	BO	External control signal output terminal/data check terminal (E/E MOS push-pull)
10	TVI	High frequency signal input terminal (300MHz or 350MHz max.) 1/2 prescaler is built-in.
11	FMI	High frequency signal input terminal (150MHz or 180MHz max.)
12	V_{DD}	Power supply (+5V)
13	AMI	High frequency signal input terminal (40MHz or 50MHz max.)
14	V_{SS}	Ground terminal

Electrical Characteristics (within the recommended operating condition range, unless otherwise specified) V_{SS} = 0V

Item	Pin, remark	Symbol	Condition	CX-7925B			CX-7925B-1			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating power supply current	V_{DD}	I_{DD}	Note 2		24	40		28	40	mA
Operating input frequency	TVI	fop	e_{IN} = 0.3 to 0.4Vp-p	20		300	20		350	MHz
	FMI	fop	e_{IN} = 0.2 to 4.0Vp-p	20		150	20		180	MHz
	AMI	fop	e_{IN} = 0.2 to 2.5Vp-p	0.05		40	0.05		50	MHz
Input leak current	Logic input	I_{IL}	V_{IH} = 0 to V_{DD} Note 1	−10		+10	−10		+10	μA
High level output current	Phase comparator (3-value output) PD	I_{OH}	V_{OUT} = 3V Note 2			−0.2			−0.2	mA
Low level output current		I_{OL}	V_{OUT} = 1V Note 2	0.2			0.2			mA
High impedance leak current		I_{HZ}	V_{OUT} = 2V Note 1	−50		+50	−50		+50	nA
High level output voltage	Push-pull by E/E MOS: Structure AO, BO	V_{OH}	I_{OH} = −20μA	2.8			2.8			V
Low level output voltage		V_{OL}	I_{OL} = 1mA			0.6			0.6	V

Note 1) Ta = 25°C Note 2) V_{DD} = 5V Ta = 25°C

Operating Input Frequency Measuring Circuit



Control input data to CX-7925B: T1-H, T2-H, A-L, B-H

SG: HP's 8640B (Input level is directly read with the built-in level meter)

Description of Operation

(1) Signal input from the local oscillator

CX-7925B is provided with 3 independent input terminals corresponding to the signal frequency and applications.

- AMI terminal

  Reception terminal of AM broadcast with the warranted signal input up to 40MHz or 50MHz. The frequency division ratio using this terminal is 1/2 to 1/65537.

- FMI terminal

  Reception terminal of FM and TV broadcasts with the warranted signal input up to 150MHz or 180MHz. An external prescaler is not required in reception of FM channels. When TV is received, entire TV band width can be covered with combination of an external prescaler up to 1/8. The frequency division ratio ranges from 1/12 to 1/262.151. This terminal is open when it is not in use.

- TVI terminal

  This terminal is dedicated to reception of TV broadcasts. Signal input up to 300MHz or 350MHz are warranted with the built-in 1/2 prescaler. When combined with an external prescaler up to 1/4, entire TV bandwidth can be covered. The frequency division ranges from 1/24 to 1/524.302. When this terminal is not in use, it is grounded internally via a resistor of more than 100 kilo-ohms.

(2) Phase comparator

The phase comparator output (PD terminal) has a 3-value level. When the input signal is advanced in phase than the reference signal, the terminal becomes HIGH level; LOW level when the phase is lagging behind and high impedance when they are in phase.

(3) Control signal and control system

CX-7925B is designed as a controller compatible with general 4- or 8-bit microcomputers. Three control input terminals, CLK, LAT and DIN, are available. Two control output terminals, AO and BO are also available. By combining these terminals properly, simplification of the system or multi-functional system can be realized.

(3-1) Control signal input modes

CX-7925B has three control signal input modes. DATA INPUT mode (normal mode), UP/DOWN mode and DATA CHECK mode with each of them differing in its signal input system.

(a) DATA INPUT mode (normal mode)

To set all initial values of CX-7925B it is required to input total 40-bit data in 20 bits each in this mode. When data is input to the DIN terminal with the LAT terminal in the LOW state, the data is input in one bit each to the shift register with the rise of clock input to the CLK terminal. After transmitting 20-bit data to the shift register, the data is latched when the LAT terminal is set to HIGH with the CLK in the HIGH state. (After latching of the data, the LAT terminal must be reset to LOW. Varying of the DIN and CLK terminals with the LAT terminal HIGH may affect the data internally.)
As will be described in detail later, input data is input either in the programmable divider or reference divider depending on a state of the last bit C. In practice, input the 20-bit data including the reference divider frequency division number, input terminal selection and AO/BO output terminal data from the controller first of all in the above manner. At this time, the last bit C of the data is set to LOW.
Then, input the 20-bit data including the programmable divider setting data in the same manner with the last bit C set to HIGH. In this manner, all internal states are set. After this setting, the latter 20-bit data only is varied when only the programmable divider value is varied. (At this time, C is set to HIGH without fail.)
When the programmable divider value is varied (selection of a broadcast channel, AFT), the following UP/DOWN mode can be used more effectively.

(b) UP/DOWN mode

After setting the CLK terminal to LOW, the UP/DOWN content can be increased or decreased by one depending on the level of HIGH or LOW of the DIN terminal when the LAT terminal (usually LOW level) is changed from HIGH to LOW. By repeating this process, the setting value of the programmable divider can be varied as required.

(c) DATA CHECK mode

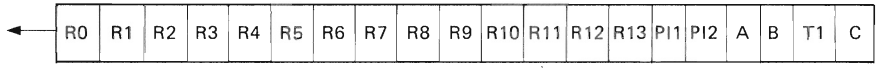
This mode is used to check if the data from the controller is correctly input to the shift register. The data left in the shift register immediately after the input data is latched is output in one bit each from the BO terminal when a clock is input to the CLK terminal after the LAT terminal is set to LOW with the CLK terminal held to HIGH. However, the shift register data is output from the BO terminal when the T1 or T2 bit of the data is respectively at HIGH or LOW only. T1 and T2 bits will be described in the following item.

(3-2) Control data assignment

The CX-7925B control data is assigned in 20 bits. The last 2 bits are the data recognition code and their recognition will tell the data content. Switching to the TEST mode is also performed using this code internally. As is described in the following, each of the frequency division number of the programmable divider and reference divider is given in the binary value with the leading digit of LSB.

(a) Control input data of the reference divider, etc. (C = LOW)

This data can be described as an initialization setting data and it is always input whenever the power supply is fed or a channel band is switched. The input data is assigned as follows.



- R0 – R13: Reference divider frequency division number (binary value with the LSB of R0). In practice, an offset component between the actual frequency division number and the input data. Their relationship is as follows.
  (Actual frequency division number) = (Input data) + 2
- PI1, PI2: Specification of the signal input terminal.

Input / PI1, PI2	AMI	FMI	TVI
PI1	–	L	H
PI2	L	H	H

- A, B, T1: Each of the AO and BO terminals have 2 functions which are switched depending on the T1 value. When T1 is at LOW, A and B values are output as they are to the AO and BO terminals. These signals can be used for switching an external prescaler's frequency division ratio, the filter constant and channel band, etc. When the prescaler M54465P (Mitsubishi) is used, the selection code of frequency division ratio will be as follows:

Frequency division ratio / A, B	1/2	1/4	1/8
A	H	L	L
B	L	H	L

When T1 is at HIGH, the AO output terminal outputs the LOCK/UNLOCK state of the phase comparator.

AO terminal H: UNLOCK
L: LOCK

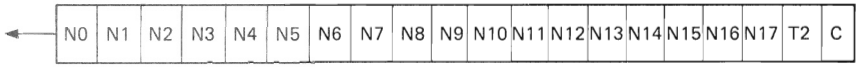
This can be used as a muting signal.
The BO terminal becomes, as described in (3-1) (C), the data output terminal of the shift register and the shift register content is continuously output by inputting the clock to the CLK terminal. It must be noted the AO and BO terminals can not be used for external control when T1 is at HIGH.

• C: This is a code to determine the latch direction of the input data. In this case, set to LOW.

Input data				AO output	BO output
T2	T1	A	B		
L	L			A	B
L	H			UNLOCK signal	Shift register output
H	H	L	L	Reference divider outputs	Main divider output
H	H	L	H	Main divider output	

(b) Programmable divider input data (C = HIGH)

This data determines the programmable divider's frequency division ratio.



• N0 – N17: Programmable divider frequency division number.
(Binary value with N0 as the LSB.) Actual frequency division number will be as follows depending on a terminal selected for the signal input.

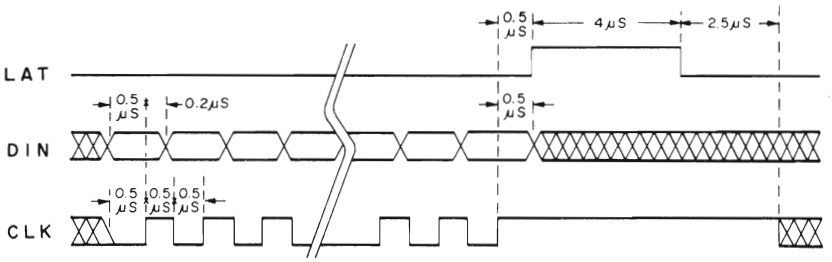
Control data		Input terminal	Range of the frequency division input data N	Relation between N and the true frequency division number ND	Range of the true frequency division number ND
PI1	PI2				
–	L	AMI	0 – 65,535	N + 2	2 – 65,537
L	H	AMI	4 – 262,143	N + 8	12 – 262,151
H	H	TVI	4 – 262,143	2 • (N + 8)	24 – 524,302

• T2: T2 is used for selection of the test mode. Set this data to LOW usually.
When the frequency division output and reference output are to be checked, set this T2 bit and T1 bit to HIGH and A and B bits to LOW. In this instance, the AO and BO output terminals output a reference output and a frequency division output respectively.

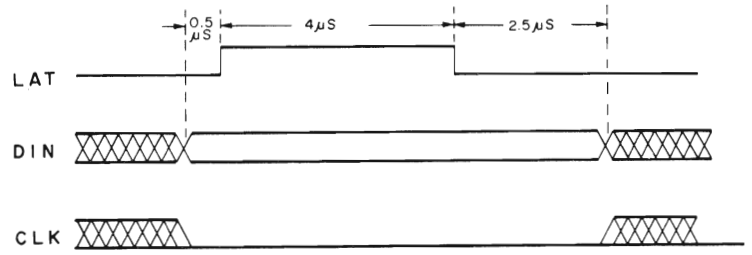
• C: As described before. Set to HIGH in this case.

(3-3) Data input and control signal times

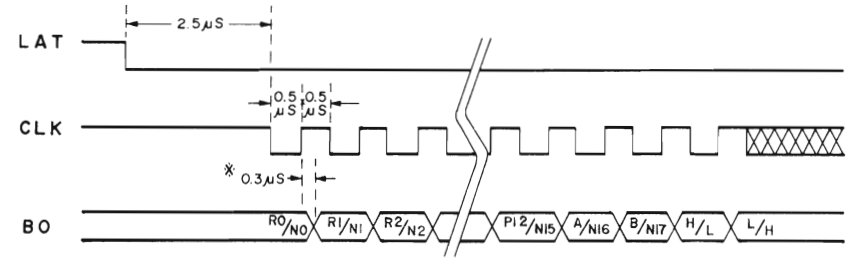
(a) Data input mode (normal mode) Each timing shows the minimum value unless otherwise described.



(b) UP/DOWN mode



(c) DATA CHECK mode (Data check of the shift register)



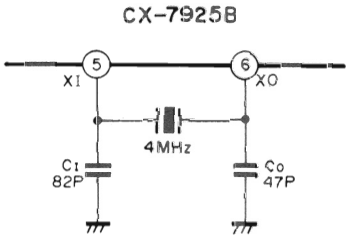
(* denotes data is output within this timing.)

(4) Reference signal (Input signal of the reference divider)

CX-7925B can generate a reference signal by connecting a crystal oscillator to XI and XO. It also allows an external clock to be used as a reference signal by inputting an external clock signal to the XI terminal.

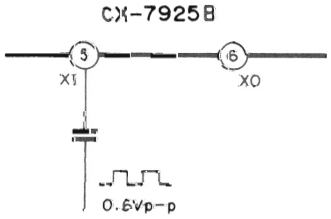
(4-1) Reference signal generator with the built-in oscillator

As shown below, connect a crystal oscillator to the XI and XO terminals. A crystal oscillator with the frequency of 1MHz – 13MHz can be used. The diagram below shows an example when a standard 4MHz oscillator is used. Be sure to make the capacitance ratio of C_I and C_O at 1 – 2 : 1 and theeir serial capacitance values be the specified load capacitance of the crystal oscillator.

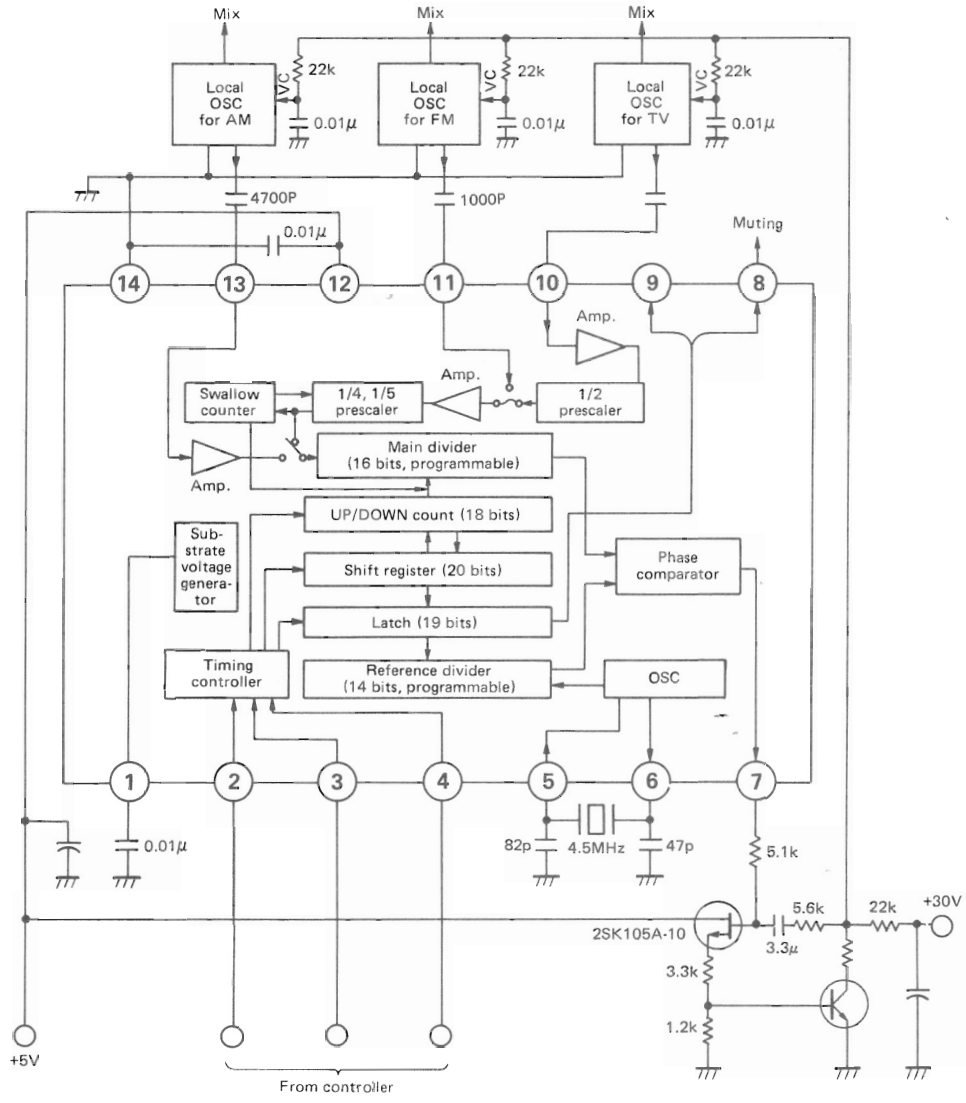


(4-2) Reference signal generator with an external clock

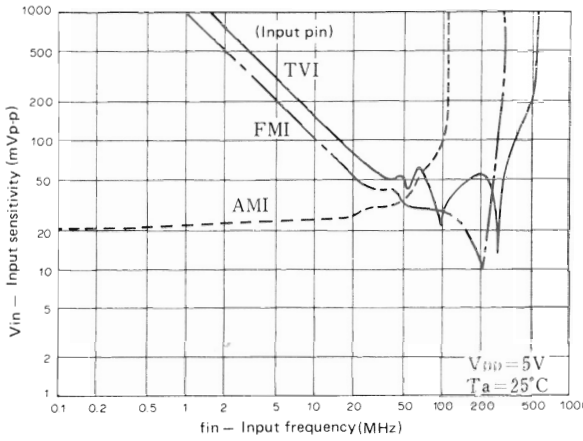
When an external clock signal, e.g. a clock signal obtained from the controller, is used as the reference clock, connect it to the XI terminal via a capacitor as shown below. The clock frequency is warranted up to 13MHz but use signal of proper rise and decay (more than 5V/μs) especially when the frequency is low. This will serve as a protection from malfunction.



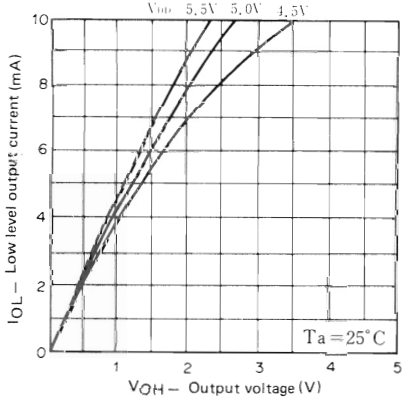
Application Circuit

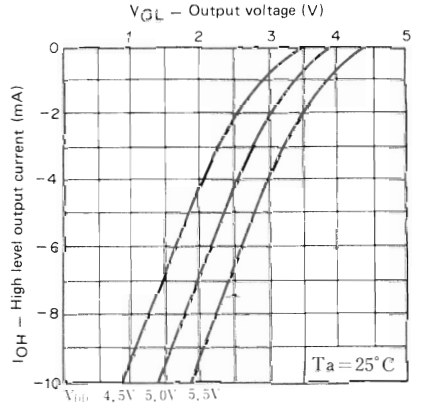


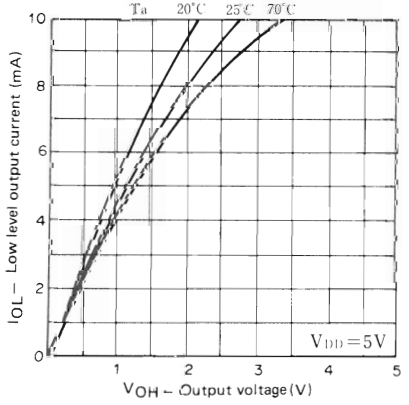
High Frequency Input Sensitivity Characteristics

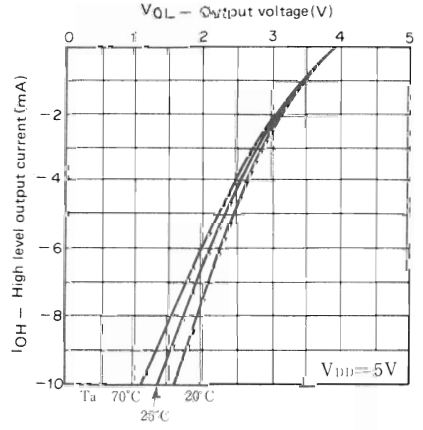


Output Current Characteristics of the AO and BO Terminals

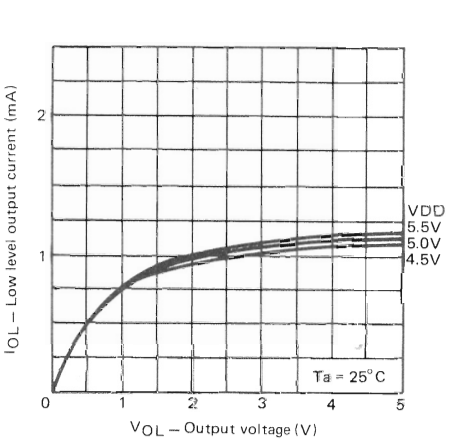


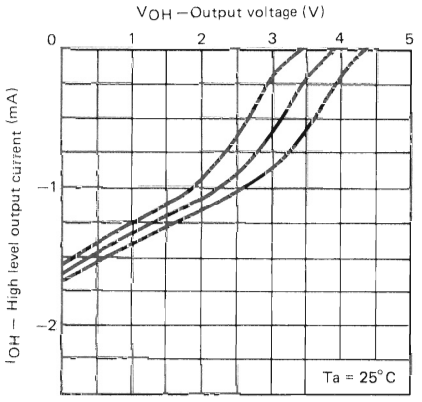


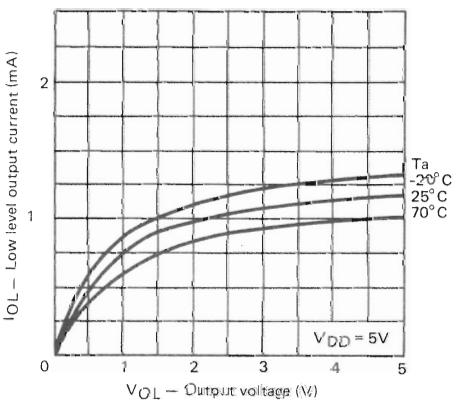


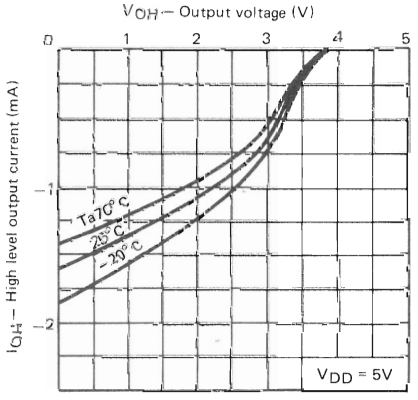


Output Current Characteristics of the PD (Phase Comparator)

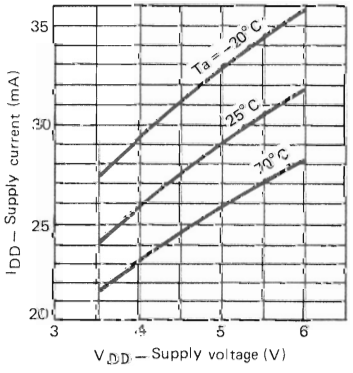








Power Supply Current I_{DD} and Voltage Characteristics



SONY CX-7961A/7961A-1

Frequency Synthesizer PLL

Description

CX-7961A is a PLL IC for the digital selection of AM, FM and TV Broadcasting as well as other radio waves, developed using the high-speed N-channel silicon gate MOS technology.

Features

- The maximum operating frequency is warranted as follows:
  CX-7961A Up to 180MHz
  CX-7961A-1 Up to 240MHz
  They can be used up to 1GHz when used combined with an ECL prescaler (general-purpose).
- Programmable divider makes it possible to divide a program frequency up to 1/262,151.
- Programmable reference divider realizes selection of a given reference frequency (e.g. 244Hz – 2MHz can be selected when a 4MHz crystal oscillator is used).
- High C/N ratio with the high-speed phase comparator.
- Operation control using three terminals in serial mode.
- Independent 3 terminals (AM1, FM1 and TV1) are provided for a high frequency signal input depending on its frequency band.
- Multi-purpose output terminals are provided (AO, BO).
- Low power consumption (35m W Typ.).

Structure

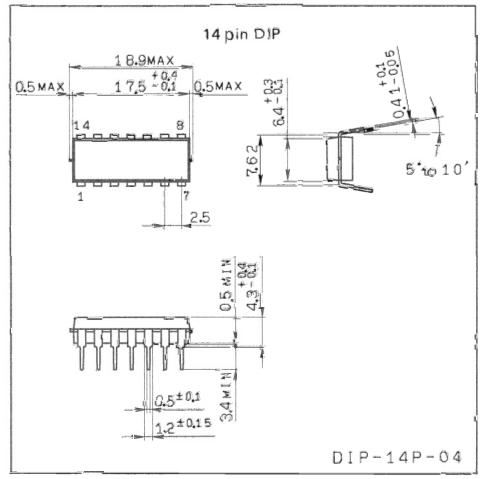
N-channel silicon gate MOS

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

• Supply voltage	V_{DD}	−0.5 to +7	V
• Pin input voltage	V_{IN}	−1 to +7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Package Outline

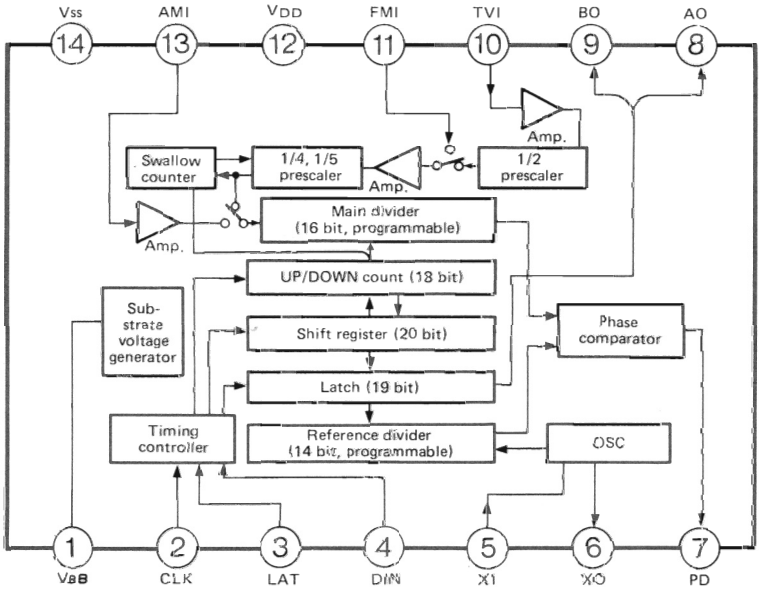
Unit: mm



Recommended Operating Conditions

Item	Pin, remark	Symbol	Operating range	Unit
Supply voltage		V_{DD}	2.7 to 3.3	V
High level input voltage	CLK, DIN	V_{IH}	1.5 to V_{DD} +0.5	V
Low level input voltage	LAT	V_{IL}	−0.5 to +0.5	V
High frequency signal input amplitude	TVI	e_{IN}	0.2 to 2.5	Vp-p
High frequency signal input amplitude	VMI	e_{IN}	0.2 to 2.5	Vp-p
High frequency input amplitude	AMI	e_{IN}	0.2 to 1.5	Vp-p
High frequency input amplitude	XI	e_{IN}	0.6 to 2.5	Vp-p
Operating temperature		Topr	−20 to +70	°C

Block Diagram and Pin Configuration



Pin Description

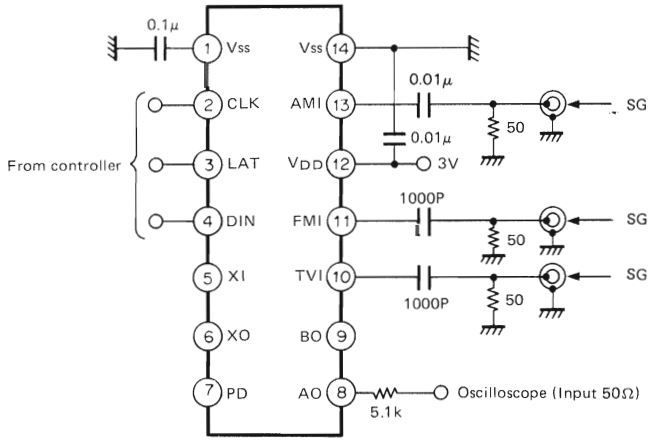
No.	Symbol	Description
1	V_{BB}	Substrate terminal (connect 0.01μF capacitor to the ground)
2	CLK	Clock input terminal for 20-bit serial data input (to be shifted with signal rise)
3	LAT	Latch signal input terminal for shift register input data (to be latched with signal rise) as well as the UP/DOWN clock input terminal (its state to be changed with signal rise)
4	DIN	Data input terminal as well as the UP/DOWN mode switching terminal (UP at "H" level, DOWN at "L" level)
5	XI	Crystal oscillator connection terminal for the reference signal generation (7.2MHz max., 4.0MHz standard)
6	XO	
7	PD	Phase comparator output terminal (three states)
8	AO	External control signal output terminal/unlock output terminal (E/E MOS push-pull)
9	BO	External control signal output terminal/data check terminal (E/E MOS push-pull)
10	TVI	High frequency signal input terminal (180MHz or 240MHz max.) 1/2 prescaler is built-in.
11	FMI	High frequency signal input terminal (90MHz or 125MHz max.)
12	V_{DD}	Power supply (+3V)
13	AMI	High frequency signal input terminal (20MHz or 25MHz max.)
14	V_{SS}	Ground terminal

Electrical Characteristics (within the recommended operating condition range, unless otherwise specified) V_{SS} = 0V

Item	Pin, remark	Symbol	Condition	CX-7961A			CX-7961A-1			Unit
				Min	Typ	Max	Min	Typ	Max	
Operating power supply current	V_{DD}	I_{DD}	f_{IN} = 110MHz Note 2		10	18		13	18	mA
Operating input frequency	TVI	fop	e_{IN} = 0.2 to 2.5Vp-p	10		180	10		240	MHz
	FMI	fop	e_{IN} = 0.2 to 2.5Vp-p	10		90	10		125	MHz
	AMI	fop	e_{IN} = 0.2 to 1.5Vp-p	0.05		20	0.05		25	MHz
Input leak current	Logic input	I_{IL}	V_{IH} = 0 to V_{DD} Note 1	−10		+10	−10		+10	μA
High level output current	Phase comparator (3-value output) PD	I_{OH}	V_{OUT} = 1.5V Note 2			−0.1			−0.1	mA
Low level output current		I_{OL}	V_{OUT} = 0.5V Note 2	+0.1			+0.1			mA
High impedance leak current		I_{HZ}	V_{OUT} = 1.0V Note 1	−50		+50	−50		+50	nA
High level output voltage	Push-pull by E/E MOS: Structure AO, BO	V_{OH}	I_{OH} = −20μA	1.5			1.5			V
Low level output voltage		V_{OL}	I_{OL} = 0.6mA			0.4			0.4	V

Note 1: Ta = 25°C Note 2: V_{DD} = 5V Ta = 25°C

Operating Input Frequency Measuring Circuit



Control input data to CX-7961A/7961A-1: T1-H, T2-H, A-L, B-H

SG: HP's 8640B (Input level is directly read with the built-in level meter)

Description of Operation

(1) Signal input from the local oscillator

CX-7961A is provided with 3 independent input terminals corresponding to the signal frequency and applications.

- AMI terminal

  Reception terminal of AM broadcast with the warranted signal input up to 20MHz or 25MHz. The frequency division ratio using this terminal is 1/2 to 1/65537.

- FMI terminal

  Reception terminal of FM and TV broadcasts with the warranted signal input up to 90MHz or 125MHz. An external prescaler is not required in reception of FM channels. When TV is received, entire TV band width can be covered with combination of an external prescaler up to 1/8. The frequency division ratio ranges from 1/12 to 1/262.151. This terminal is open when it is not in use.

- TVI terminal

  This terminal is dedicated to reception of TV broadcasts. Signal input up to 180MHz or 240MHz are warranted with the built-in 1/2 prescaler. When combined with an external prescaler up to 1/4, entire TV bandwidth can be covered. The frequency division ranges from 1/24 to 1/524.302. When this terminal is not in use, it is grounded internally via a resistor of more than 100 kilo-ohms.

(2) Phase comparator

The phase comparator output (PD terminal) has a 3-value level. When the input signal is advanced in phase than the reference signal, the terminal becomes HIGH level; LOW level when the phase is lagging behind and high impedance when they are in phase.

(3) Control signal and control system

CX-7961A is designed as a controller compatible with general 4-bit or 8-bit microcomputers. Three control input terminals, CLK, LAT and DIN, are available. Two control output terminals, AO and BO are also available. By combining these terminals properly, simplification of the system or multi-functional system can be realized.

(3-1) Control signal input modes

CX-7961A has three control signal input modes. DATA INPUT mode (normal mode), UP/DOWN mode and DATA CHECK mode with each of them differing in its signal input system.

(a) DATA INPUT mode (normal mode)

To set all initial values of CX-7961A it is required to input total 40-bit data in 20 bits each in this mode. When data is input to the DIN terminal with the LAT terminal in the LOW state, the data is input in one bit each to the shift register with the rise of clock input to the CLK terminal. After transmitting 20-bit data to the shift register, the data is latched when the LAT terminal is set to HIGH with the CLK in the HIGH state. (After latching of the data, the LAT terminal must be reset to LOW. Varying of the DIN and CLK terminals with the LAT terminal HIGH may affect the data internally.)
As will be described in detail later, input data is input either in the programmable divider or reference divider depending on a state of the last bit C. In practice, input the 20-bit data including the reference divider frequency division number, input terminal selection and AO/BO output terminal data from the controller first of all in the above manner. At this time, the last bit C of the data is set to LOW.
Then, input the 20-bit data including the programmable divider setting data in the same manner with the last bit C set to HIGH. In this manner, all internal states are set. After this setting, the latter 20-bit data only is varied when only the programmable divider value is varied. (At this time, C is set to HIGH without fail.)
When the programmable divider value is varied (selection of a broadcast channel, AFT), the following UP/DOWN mode can be used more effectively.

(b) UP/DOWN mode

After setting the CLK terminal to LOW, the UP/DOWN content can be increased or decreased by one depending on the level of HIGH or LOW of the DIN terminal when the LAT terminal (usually LOW level) is changed from HIGH to LOW. By repeating this process, the setting value of the programmable divider can be varied as required.

(c) DATA CHECK mode

This mode is used to check if the data from the controller is correctly input to the shift register. The data left in the shift register immediately after the input data is latched is output in one bit each from the BO terminal when a clock is input to the CLK terminal after the LAT terminal is set to LOW with the CLK terminal held to HIGH. However, the shift register data is output from the BO terminal when the T1 or T2 bit of the data is respectively at HIGH or LOW only. T1 and T2 bits will be described in the following item.

(3-2) Control data assignment

The CX-7961A control data is assigned in 20 bits. The last 2 bits are the data recognition code and their recognition will tell the data content. Switching to the TEST mode is also performed using this code internally. As is described in the following, each of the frequency division number of the programmable divider and reference divider is given in the binary value with the leading digit of LSB.

(a) Control input data of the reference divider, etc. (C = LOW)

This data can be described as an initialization setting data and it is always input whenever the power supply is fed or a channel band is switched. The input data is assigned as follows.

- R0 – R13: Reference divider frequency division number (binary value with the LSB of R0). In practice, an offset component between the actual frequency division number and the input data. Their relationship is as follows.
  (Actual frequency division number) = (Input data) + 2
- PI1, PI2: Specification of the signal input terminal.

Input / PI1, PI2	AMI	FMI	TVI
PI1	–	L	H
PI2	L	H	H

- A, B, T1: Each of the AO and BO terminals have 2 functions which are switched depending on the T1 value. When T1 is at LOW, A and B values are output as they are to the AO and BO terminals. These signals can be used for switching an external prescaler's frequency division ratio, the filter constant and channel band, etc. When the prescaler M54465P (Mitsubishi) is used, the selection code of frequency division ratio will be as follows:

Frequency division ratio / A, B	1/2	1/4	1/8
A	H	L	L
B	L	H	L

When T1 is at HIGH, the AO output terminal outputs the LOCK/UNLOCK state of the phase comparator.

AO terminal H: UNLOCK
L: LOCK

This can be used as a muting signal.
The BO terminal becomes, as described in (3-1) (C), the data output terminal of the shift register and the shift register content is continuously output by inputting the clock to the CLK terminal. It must be noted the AO and BO terminals can not be used for external control when T1 is at HIGH.

• C: This is a code to determine the latch direction of the input data. In this case, set to LOW.

Input data				AO output	BO output
T2	T1	A	B		
L	L			A	B
L	H			UNLOCK signal	Shift register output
H	H	L	L	Reference divider output	Main divider output
H	H	L	H	Main divider output	

(b) Programmable divider input data (C = HIGH)

This data determines the programmable divider's frequency division ratio.

←	N0	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16	N17	T2	C

• N0 – N17: Programmable divider frequency division number.
(Binary value with N0 as the LSB.) Actual frequency division number will be as follows depending on a terminal selected for the signal input.

Control data		Input terminal	Range of the frequency division input data N	Relation between N and the true frequency division number ND	Range of the true frequency division number ND
PI1	PI2				
–	L	AMI	0 – 65,535	N + 2	2 – 65,537
L	H	AMI	4 – 262,143	N + 8	12 – 262,151
H	H	TVI	4 – 262,143	2 • (N + 8)	24 – 524,302

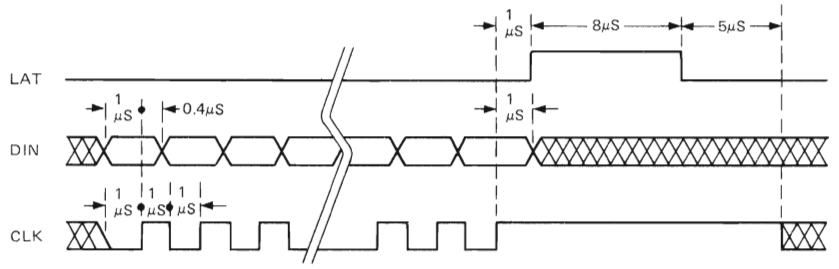
• T2: T2 is used for selection of the test mode. Set this data to LOW usually.
When the frequency division output and reference output are to be checked, set this T2 bit and T1 bit to HIGH and A and B bits to LOW. In this instance, the AO and BO output terminals output a reference output and a frequency division output respectively.

• C: As described before. Set to HIGH in this case.

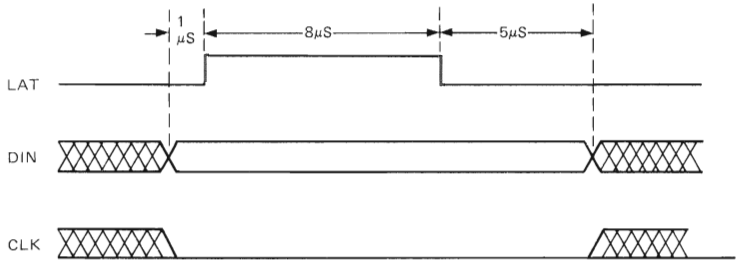
(3-3) Data input and control signal times

(a) Data input mode (normal mode)

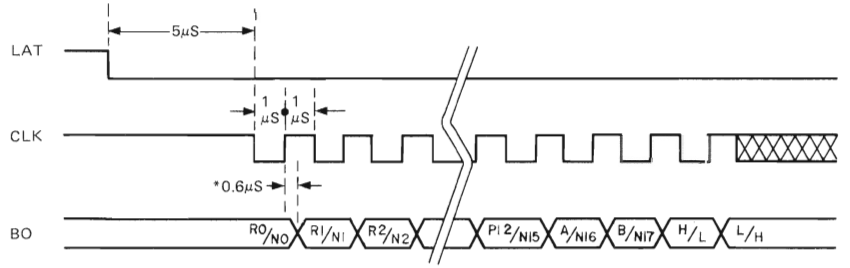
Each timing shows the minimum value unless otherwise described.



(b) UP/DOWN mode



(c) DATA CHECK mode (Data check of the shift register)



(* denotes data is output within this timing.)

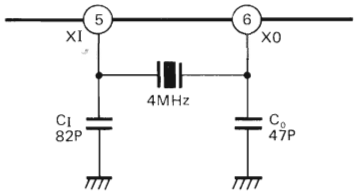
(4) Reference signal (Input signal of the reference divider)

CX-7961A can generate a reference signal by connecting a crystal oscillator to XI and X0. It also allows an external clock to be used as a reference signal by inputting an external clock signal to the XI terminal.

(4-1) Reference signal generator with the built-in oscillator

As shown below, connect a crystal oscillator to the XI and X0. A crystal oscillator with the frequency of 1MHz – 7.2MHz can be used. The diagram below shows an example when a standard 4MHz oscillator is used.
Be sure to make the capacitance ratio of C_I and C_0 at 1 – 1 : 1 and their serial capacitance values be the specified load capacitance of the crystal oscillator.

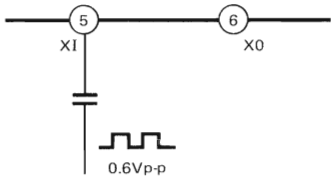
CX-7961A



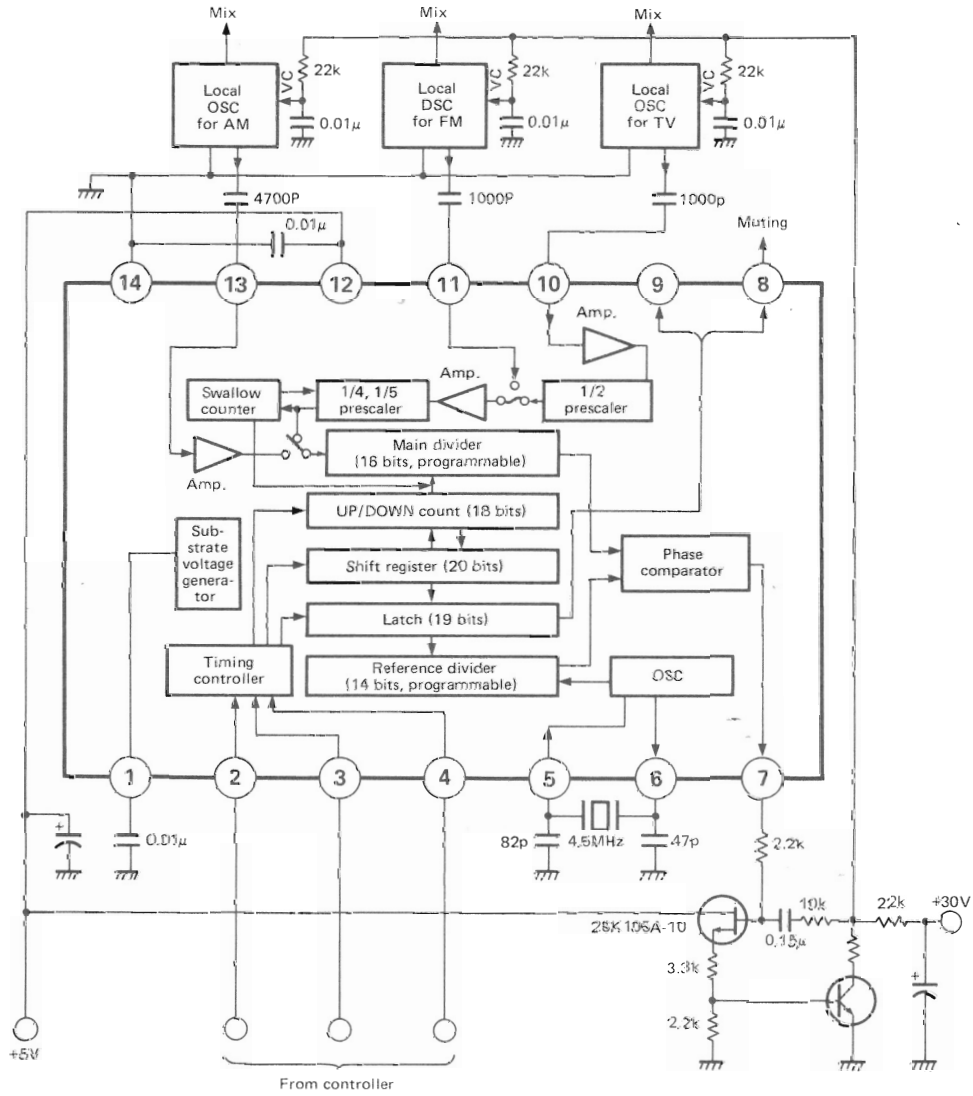
(4-2) Reference signal generator with an external clock

When an external clock signal, e.g. a clock signal obtained from the controller, is used as the reference clock, connect it to the XI terminal via a capacitor as shown below. The clock frequency is warranted up to 7.2MHz but use signal of proper rise and decay (more than 5V/μs) especially when the frequency is low. This will serve as a protection from mulfunction.

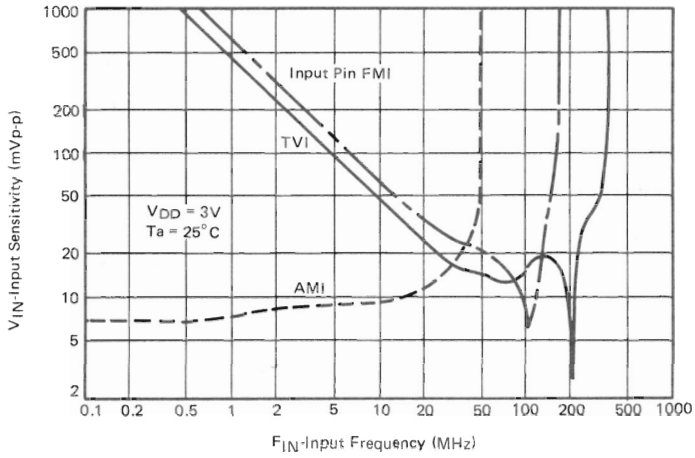
CX-7961A

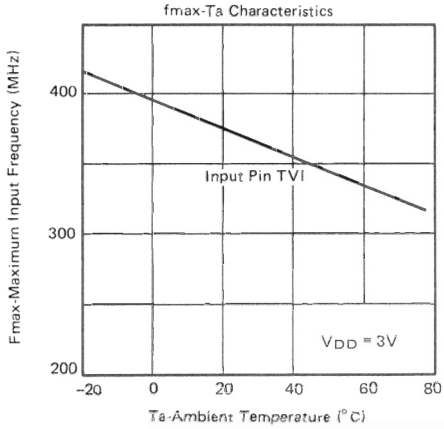


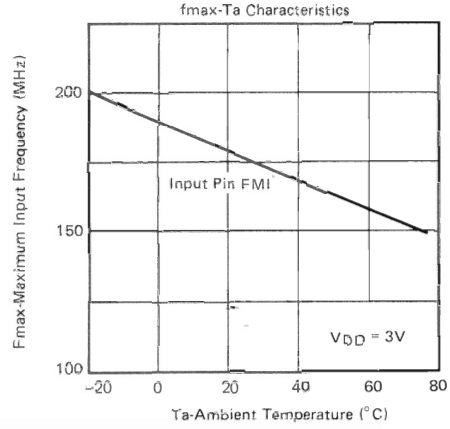
Application Circuit



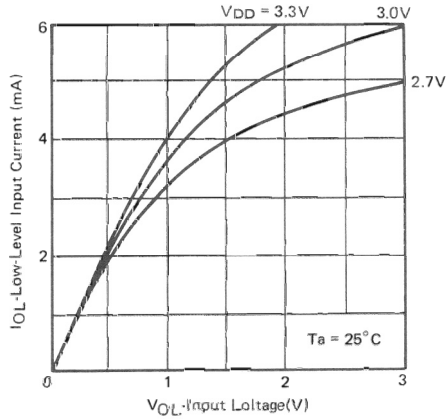
Characteristics of high-frequency input sensitivity

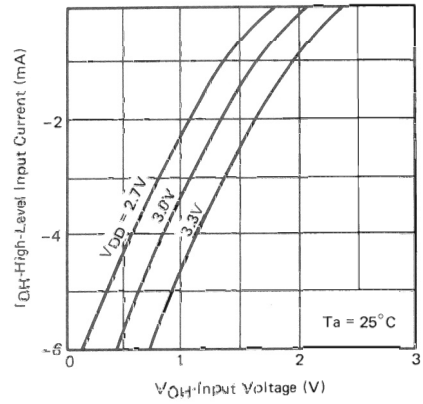




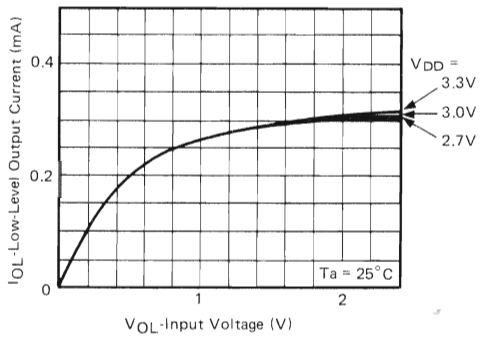


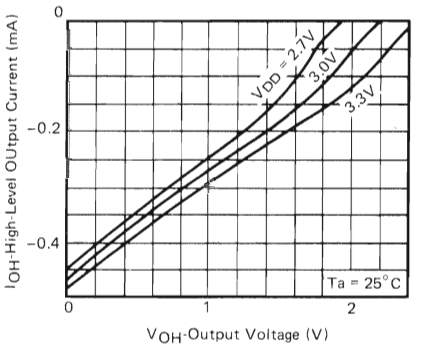
Output current characteristics of AO and BO terminals

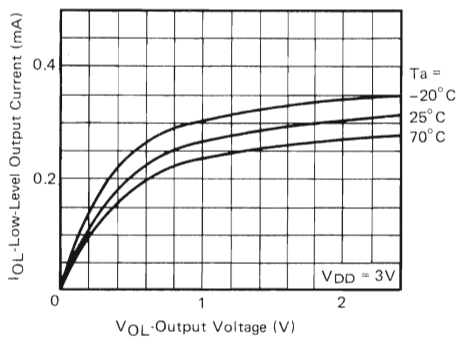


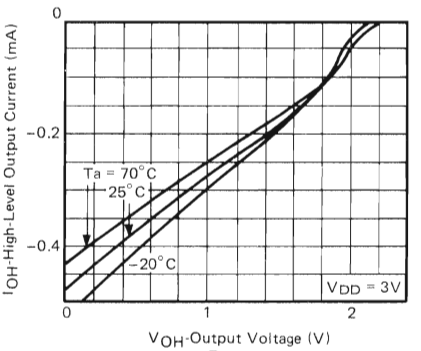


Output Current Characteristics of PD (Phase Discriminator) Terminal

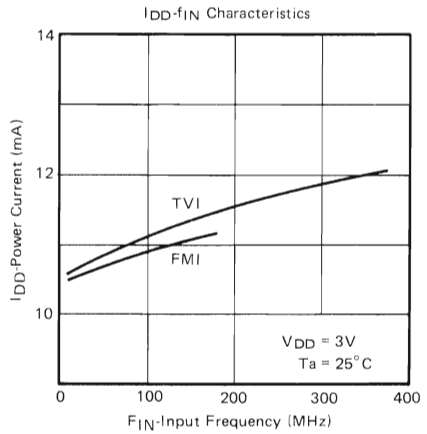


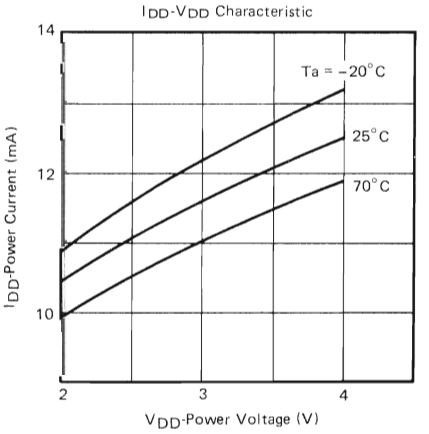






Power Current Characteristics





Frequency Synthesizer PLL

Description

CX23055 is a PLL IC for the digital tuning selection of TV broadcasts and other frequencies, developed using the submicron channel MOS technology. It allows direct signal input up to the frequencies including the UHF band.

Features

- The maximum operating frequency is warranted as follows:
  - CX23055 Up to 870 MHz
  - CX23055-1 Up to 950 MHz
- Program frequency division of 12 to 2^{18} + 7 is possible with the 18-bit programmable divider.
- Any reference frequency can be selected with the programmable reference divider (2 to 2^{14} + 1).
- Serial control using 3 terminals.
- Two independent terminals (RF1 and RF2) are provided for high frequency signal input.
- Multi-purpose output terminals (AO, BO) are provided.
- Low power dissipation (125mW Typ.)
- +5V single power supply.

Structure

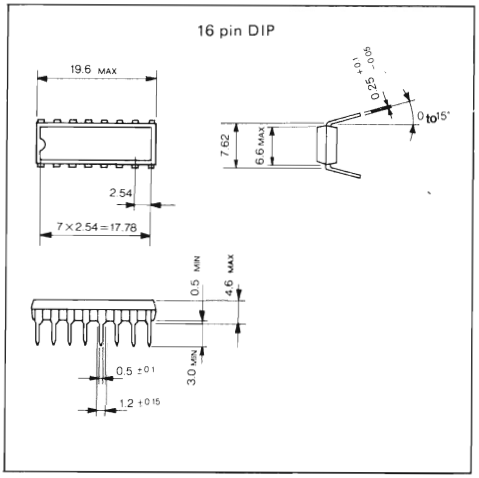
N-channel silicon gate MOS IC.

Applications

PLL IC for the tuning selection of TV, CATV, car telephone, telecommunication equipment, etc.

Package Outline

Unit: mm



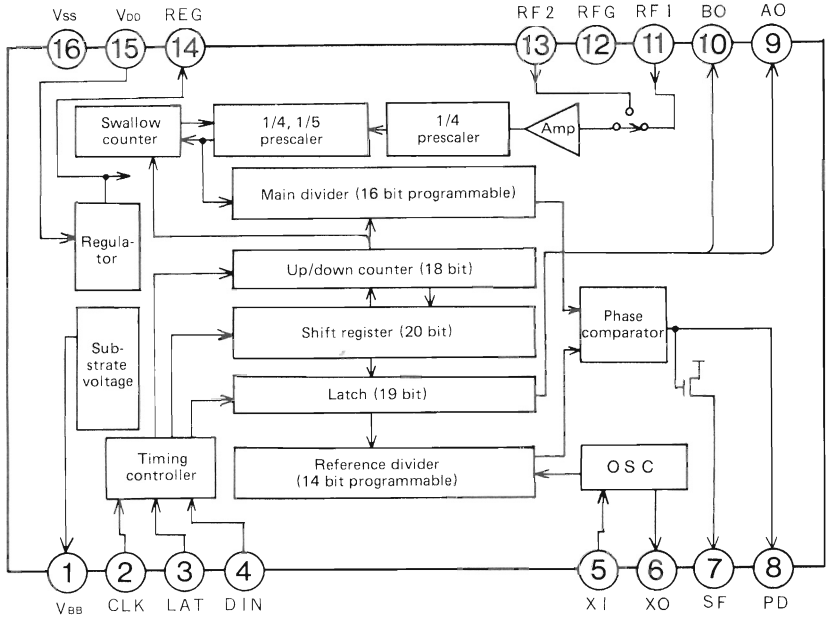
Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

• Supply voltage	V_{DD}	−0.5 to +7	V
• Terminal input voltage	V_{IN}	−1 to +7	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions (V_{SS} = 0V)

• Supply voltage	V_{DD}	4.5 to 5.5	V
• High-level input voltage	V_{IH}	+2.0 to V_{DD} +0.5	V
• Low-level input voltage	V_{IL}	−0.5 to +0.8	V
• XI terminal input amplitude	e_{in}	0.4 to 3	Vp-p
• Operating temperature	Topr	−20 to +70	°C

Block Diagram



Pin Description

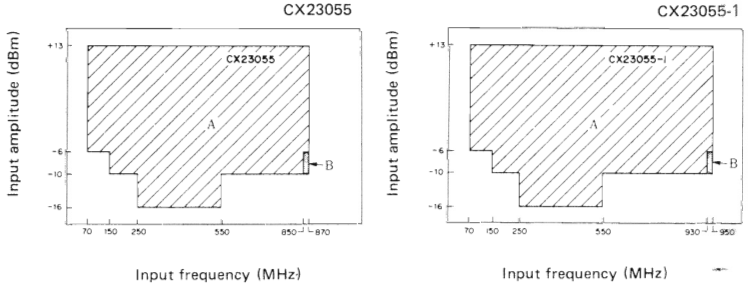
No.	Symbol	Description
1	V_{BB}	Substrate terminal (connect 0.01μF to the ground)
2	CLK	Clock input terminal for 20 bit serial data input
3	LAT	Latch signal input terminal for shift register input data as well as UP/DOWN clock input terminal
4	DIN	Data input terminal as well as UP/DOWN mode switching terminal
5	XI	Crystal oscillator connection terminal for reference signal generator (1 to 15 MHz)
6	XO	
7	SF	Source follower output terminal for filter amplifier
8	PD	Phase comparator output terminal (3 states)
9	AO	External control signal output terminal/Unlock output terminal
10	BO	External control signal output terminal/Data check terminal
11	RF1	High frequency signal input terminal CX23055: 70 to 870 MHz CX23055-1: 70 to 950 MHz
12	RFG	Ground terminal for high frequency signal
13	RF2	High frequency signal input terminal CX23055: 70 to 870 MHz CX23055-1: 70 to 950 MHz
14	REG	Built-in regulator output (3V)
15	V_{DD}	Power supply (+5V)
16	V_{SS}	Ground terminal

Electrical Characteristics (within the recommended operating condition range, unless otherwise specified) V_{SS} = 0V

Item	Terminal, Remarks	Symbol	Condition	CX23055			CX23055-1			Unit
				Min	Typ	Max	Min	Typ	Max	
Operating power supply current	V_{DD}	I_{DD}	f_{IN} = 500 MHz Note 1 ein = –10 dBm		25	39		28	39	mA
Operating input frequency	RF1, RF2	fop	See Notes 2-1 and 2-2	70		870	70		950	MHz
Input leak current	Logic input	I_{IL}	V_{IN} = 0 to V_{DD}	–10		+10	–10		+10	μA
High-level output current	Phase comparator (Three-state output) PD	I_{OH}	V_{OUT} = 1V		–200	–85		–200	–85	μA
Low-level output current		I_{OL}		85	180		85	180		μA
High impedance leak current		I_{HZ}	V_{OUT} = 1V, Note 1	–50		+50	–50		+50	nA
Source follower output voltage	SF	V_{OUT}	V_{IN} = 1V I_{OUT} = –200μA	0.95	1.35	1.70	0.95	1.35	1.70	V
High-level output voltage	Push-Pull output AO, BO	V_{OH}	I_{OH} = –100μA	2			2			V
Low-level output voltage		V_{OL}	I_{OL} = 0.6mA			0.4			0.4	V

Note 1: Ta = 25°C

Note 2-1: High frequency input sensitivity



Condition

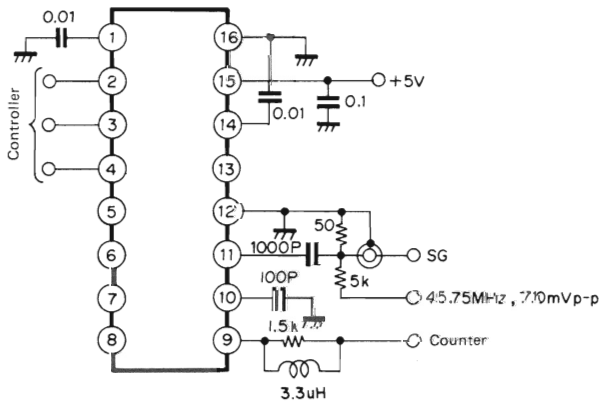
1. Ta = –20 to +65°C
2. V_{DD} = 4.5 to 5.5V
3. Interference input signal 45.75 MHz, –45 dBm
4. Input equivalent frequency division error

A: Within ±25 kHz (PLL design range)

B: Within ±4 MHz (VCO oscillation range)

dBm: 50 ohm oriented
+13 dBm = 2,830 mVp-p
–6 dBm = 317 mVp-p
–10 dBm = 200 mVp-p
–16 dBm = 100 mVp-p

Note 2-2: High frequency input sensitivity measuring circuit



Input data from controller

LSB				MSB
←0001	0000	0000	0000	0011
←1111	1111	1111	1111	0110

Operation Description

CX23055 is a PLL IC for the digital tuning selection of TV broadcasts and other frequencies, designed to cover entire band width of TV broadcasts. CX23055 is designed as a high-speed version of CX-7925A (up to 350MHz), sharing many common features with CX-7925A. Especially, the data input system from the controller is identical allowing use of similar controller programs. However, it is noted the name of high frequency signal input terminal, the number of terminal pins and the fixed frequency division value of the internal prescaler are different. CX23055 has a built-in source follower (MOS FET) for the filter amplifier, eliminating use of the FET which was required as an external device with conventional PLLs.

(1) Signal input from local oscillator

CX23055 is provided with two independent high frequency signal input terminals (RF1 and RF2). Both of them are capable of accepting 70 to 870MHz signals (CX23055) or 70 to 950MHz signals (CX23055-1) allowing 18 bit program frequency division internally through the 1/4 prescaler.
The input impedance of them are almost capacitive and have the input capacity values of 1.4pF (RF1) and 1.2pF (RF2).

(2) Phase comparator output

The phase comparator output (PD terminal) has a 3-state level and it becomes the HIGH level when the input signal is advanced in phase than the reference signal or the LOW level when the phase lags behind; it becomes a high impedance when both signals are in phase.

(3) Control signal and control system

CX23055 is designed to be a controller compatible with generally-used 4 or 8 bit microcomputers. It has 3 terminals of CLK, LAT and DIN as the control input terminals. As the controlling input terminals, 2 terminals of AO and BO are also available. By combined use of them properly, it is possible to simplify the system with multi-functions.

(3-1) Control signal input mode

CX23055 has three control signal input modes, DATA INPUT mode (normal mode), UP/DOWN mode and DATA CHECK mode with each of them differing in its input system.

(a) DATA INPUT mode (normal mode)

To set all initial values of CX23055, it is required to input total 40 bit data in 20 bits each in this mode. When data is input to the DIN terminal with the LAT terminal in the LOW state, the data is input in one bit each to the shift register with the rising of clock input to the CLK terminal. After transmitting 20 bit data to the shift register, the data is latched when the LAT terminal is set to HIGH with the CLK in the HIGH state. (After latching of the data, the LAT terminal must be reset to LOW. Varying of the DIN and CLK terminals with the LAT terminal at HIGH may affect the data internally.)
As will be described in detail later, input data is input either in the programmable divider or reference divider depending on a state of the last bit C. In practice, input the 20 bit data including the reference divider frequency division number, input terminal selection and AO/BO output terminal data from the controller first of all in the above manner. At this time, the last bit C of the data is set to LOW.
Then, input the 20 bit data including the programmable divider setting data in the same manner with the last bit C set to HIGH. In this manner, all internal states are set. After this setting, the latter 20 bit data only is varied when only the programmable divider value is varied. (At this time, C is set to HIGH without fail.)
When the programmable divider value is varied (selection of a broadcast channel, AFT), the following UP/DOWN mode can be used more effectively.

(b) UP/DOWN mode

After setting the CLK terminal to LOW, the content of UP/DOWN counter can be increased or decreased by one depending on the level of HIGH or LOW of the DIN terminal when the LAT terminal (usually LOW level) is changed from HIGH to LOW. By repeating this process, the setting value of the programmable divider can be varied as required.

(c) DATA CHECK mode

This mode is used to check if the data from the controller is correctly input to the shift register. The data left in the shift register immediately after the input data is latched is output in one bit each from the BO terminal when a clock is input to the CLK terminal after the LAT terminal is set to LOW with the CLK terminal held to HIGH. However, the shift register data is output from the BO terminal when the T1 or T2 bits will be described in the following item.

(3-2) Control data construction

The CX23055 control data is assigned in 20 bits. The last 2 bits are the data recognition code and their recognition will tell the data content. Switching to the TEST mode is also performed using this code internally. As is described in the following, each of the frequency division number of the programmable divider and reference divider is given in the binary value with the leading digit of LSB.

(a) Control input data of the reference divider, etc. (C = LOW)

This data can be described as an initialization setting data and it is always input whenever the power supply is fed or a channel band is switched. The input data is assigned as follows.

- R0 to R13: Reference divider frequency division number (binary value with the LSB of R0). In practice, an offset component between the actual frequency division number and the input data. Their relationship is as follows.
  (Actual frequency division number) = (Input data) + 2
- PI1, PI2: Specification of the signal input terminal.

Input / PI1, PI2	RF2	RF1
PI1	L	H
PI2	H	H

- A, B, T1: Each of the AO and BO terminals have 2 functions which are switched depending on the T1 value. When T1 is at LOW, A and B values are output as they are to the AO and BO terminals. These signals can be used for switching the filter constant, channel band, etc.
  When T1 is at HIGH, the AO output terminal outputs the LOCK/UNLOCK state of the phase comparator.

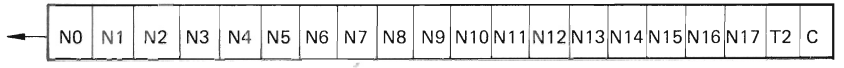
  AO terminal H; UNLOCK
  L; LOCK

  This can be used as a muting signal.
  The BO terminal becomes, as described in (3-1) (C), the data output terminal of the shift register and the shift register content is continuously output by inputting the clock to the CLK terminal. It must be noted the AO and BO terminals can not be used for external control when T1 is at HIGH.
- C This is a code to determine the latch direction of the input data. In this case, set to LOW.

Input data				AO output	BO output
T2	T1	A	B		
L	L			A	B
L	H			UNLOCK signal	Shift register output
H	H	L	L	Reference divider output	Main divider output
H	H	L	H	Main divider output	

(b) Programmable divider input data (C = HIGH)

This data determines the programmable divider's frequency division ratio.



• N0 to N17: Programmable divider frequency division number. (Binary value with N0 as the LSB.) Actual frequency division number will depend on which terminal is selected for the signal input as shown next.

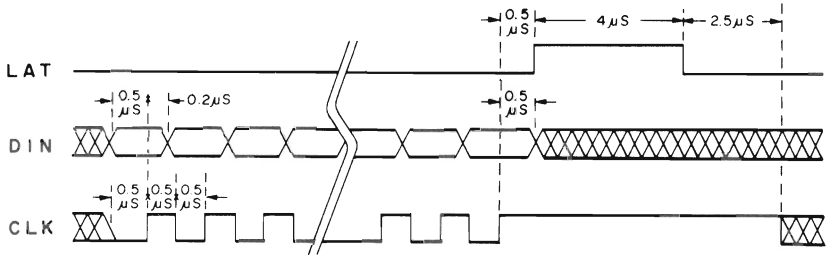
Range of the frequency division input data N	Relation between N and the true frequency division number ND	Range of the true frequency division number ND
4 to 262, 143	4 • (N + 8)	48 to 1,048,604

• T2 ; T2 is used for selection of the test mode. Set this data to LOW usually.
When the frequency division output and reference output are to be checked, set this T2 bit and T1 bit to HIGH and A and B bits to LOW. In this instance, the AO and BO output terminals output a reference output and a frequency division output respectively.

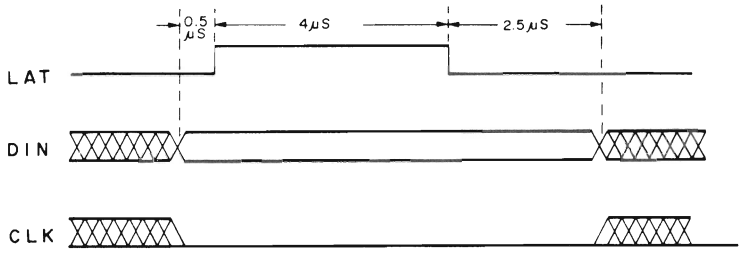
• C ; As described before. Set to HIGH in this case.

(3-3) Data input and control signal timings

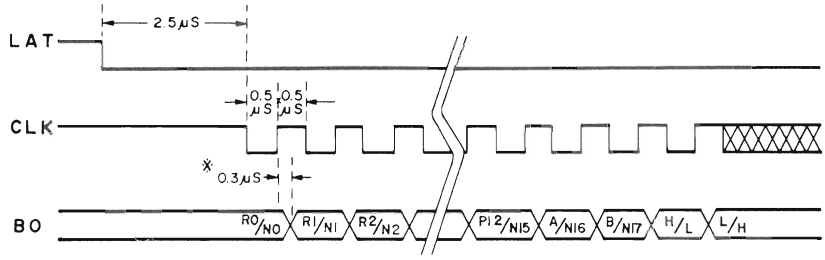
(a) Data input mode (normal mode) Each timing shows the minimum value unless otherwise described.



(b) UP/DOWN mode



(c) DATA CHECK mode (Data check of the shift register)



(* denotes data is output within this timing.)

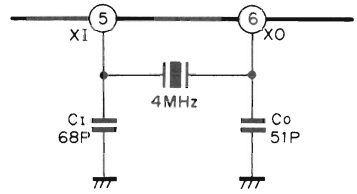
(4) Reference signal (Input signal of the reference divider)

CX23055 can generate a reference signal by connecting a crystal oscillator to XI and X0. It also allows an external clock to be used as a reference signal by inputting an external clock signal to the XI terminal.

(4-1) Reference signal generator with the built-in oscillator

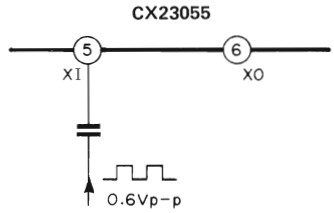
As shown below, connect a crystal oscillator to the XI and X0 terminals. A crystal oscillator with the frequency of 1MHz to 15MHz can be used. The diagram below shows an example when a standard 4MHz oscillator is used. Be sure to make the capacitance ratio of C_I and C_0 at 1 to 2 : 1 and their serial capacitance values be the specified load capacitance of the crystal oscillator.

CX23055

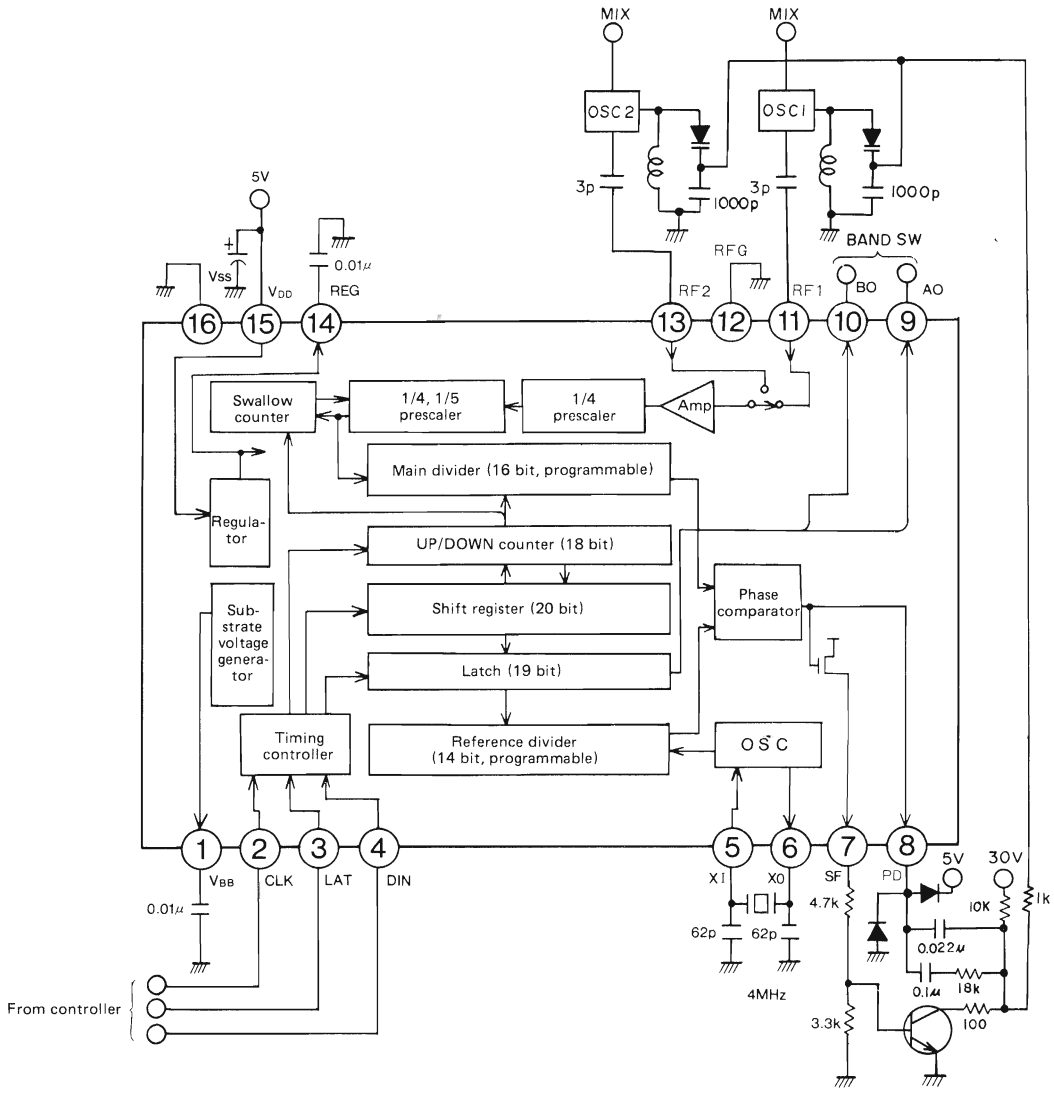


(4-2) Reference signal generator with an external clock

When an external clock signal, e.g. a clock signal obtained from the controller, is used as the reference clock, connect it to the XI terminal via a capacitor as shown below. The clock frequency is warranted up to 15MHz but use a signal of proper rise and decay (more than 5V/μs) especially when the frequency is low. This will serve as a protection from mulfunction.



Application Circuit



Output current characteristics of the AO and BO terminals

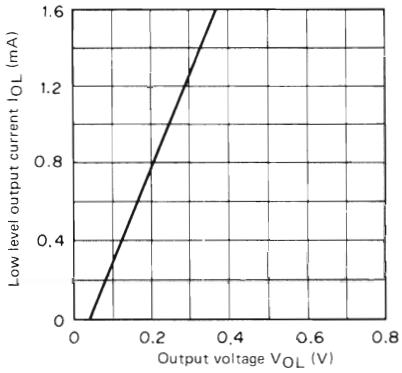


Fig. 1-1

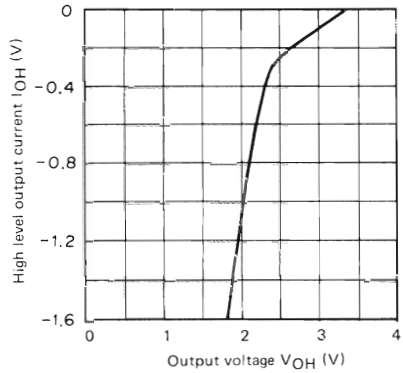


Fig. 1-2

Output current characteristics of PD terminal

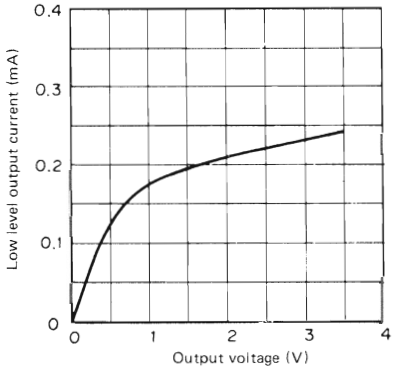


Fig. 2-1

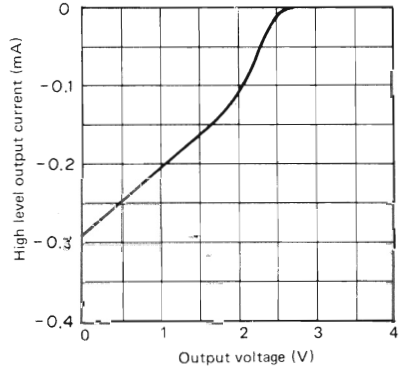


Fig. 2-2

Output characteristics of SF terminal

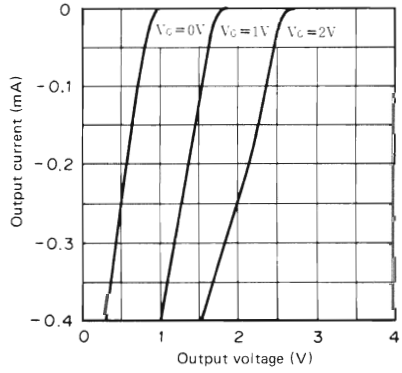
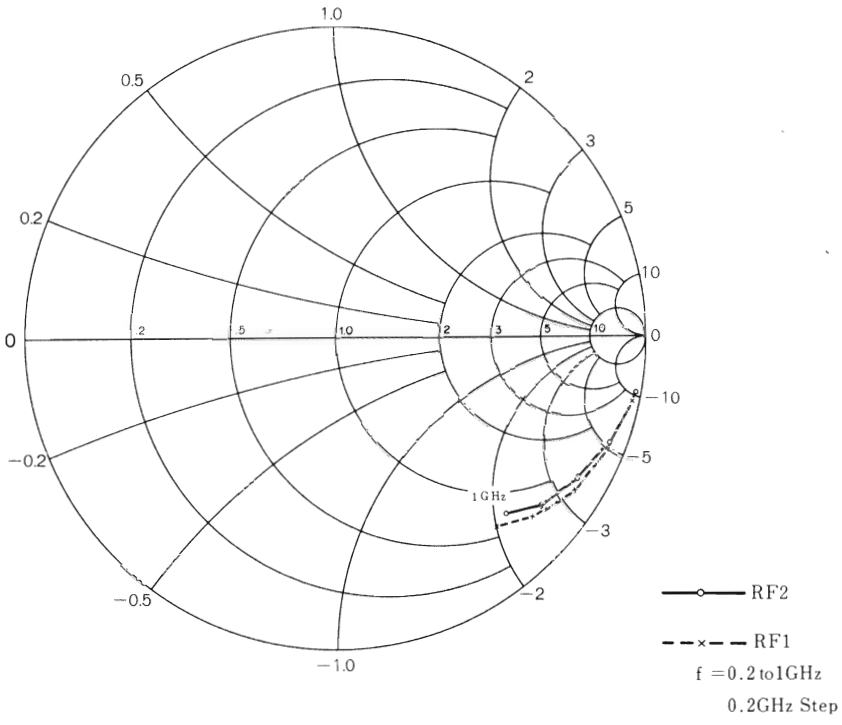
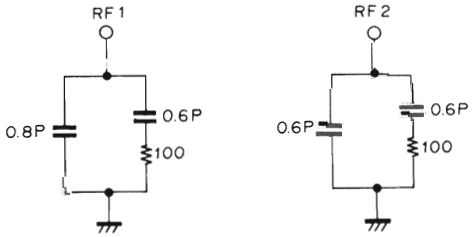


Fig. 3

Input Impedance



Equivalent Circuit



SONY CXK1001P

640-bit (40 word × 16 bit) Non-volatile Memory

Description

The CXK1001P is a serial input/output 640 bit electrically erasable and programable ROM, organized as 40 words of 16 bits each. Data and adress are communicated in serial form via a one-pin bidirectional bus.

It is most suitable for non-volatile channel memory for electronic tuners and a read only memory system which requires rewriting constantly and instantly in the field.

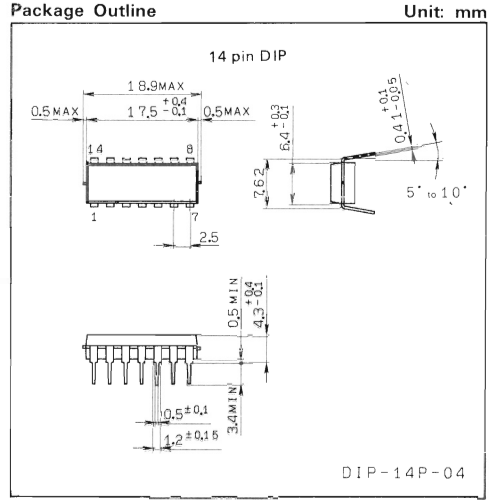
Features

- Full decode 40 word ×16 bit organization
- Word alterable
- 10 year data storage
  Write/Erase time ..... 20 ms/word
- Single −35V supply
- Number of times of erasing and writing
  ..... Over 10^5 times
- Low power consumption design (70 mW typ.)

Structure

P-channel MNOS IC

Package Outline Unit: mm



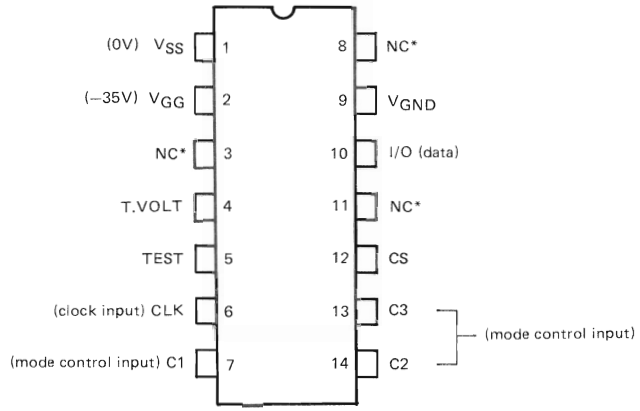
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{GG}	+0.3 to −42	V
• Input voltage	V_I	+0.3 to −20	V
• Operating temperature 1	T_{opr1}	−20 to +75	°C
• Operating temperature 2	T_{opr2}	−20 to +85	°C . . . memory holding state (power OFF)
• Storage temperature	T_{stg}	−55 to +150	°C

Recommended Operating Conditions

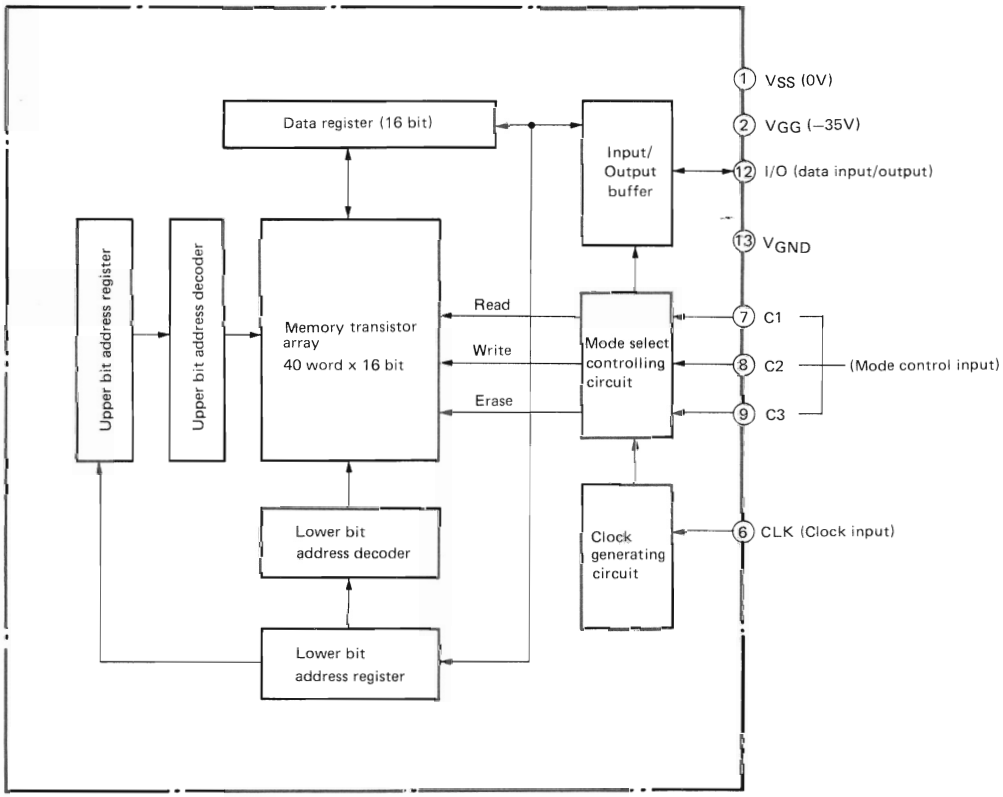
• Supply voltage 1	V_{GG}-V_{SS}	−32.2 to −40	V
• Supply voltage 2	V_{GND}-V_{SS}	−4.25 to −14	V
• High level input voltage	V_{INH}	V_{SS} −1.8 to V_{SS} +0	V
• Low level input voltage	V_{INL}	V_{SS} −14 to V_{SS} −4.25	V

Pin Configuration (Top View)



*NC: non-connection

Block Diagram



Description of Function

The CXK1001P is specified by an address which has 2 continuous 1-OUT-OF-10 codes. Modes selection can be carried out by 3 bits of parallel signals C1 to C3, and those bits specify the seven modes; namely, address input, data input, data output, erase, write, read and standby.

The program of data can be performed by applying negative pulses to MNOS memory transistor selectively, and charging electrons into SiO_2-Si_3N_4 interface of the gate insulation film by the tunnel phenomena.

Electrical characteristics 1 (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	
Power supply current	I_{GG}		2.0	3.4	mA	SB Mode
Input pull-up current 1	I_{IN1}	−45	−90	−180	μA	CS input (V_{IN} = −14V)
Input pull-up current 2	$I_{IN\ 2}$		−10	−30	μA	Other than CS (V_{IN} = − +14V)
High level output voltage	V_{OH}	V_{SS}−1			V	I_{OH} = −200μA
Low level output voltage 1	$V_{OL\ 1}$			V_{GND}+0.5	V	I_{OL} = 40 μA *1
Low level output voltage 2	$V_{OL\ 2}$			V_{GND}+1.0	V	I_{OL} = 500 μA *2
Output leakage current	I_{OLK}			±1.0	μA	V_O = −14V

Note) *1. V_{GND} — V_{SS} = −14.0V.
*2. V_{GND} — V_{SS} = −5.0V.

Electrical characteristics 2 (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	
Clock frequency	f	1 (10)	16	50	kHz	
Clock pulse width	ϕ_{WH}	9			μs	H level width
Clock pulse width	ϕ_{WL}	9			μs	L level width
Rise and Fall time	t_{r1}, t_{f1}			10	μs	CS
Rise and Fall time	t_{r2}, t_{f2}			1	μs	Other than CS
Data reading out time	t_R			5	μs	
Write/Erase time	t_{WE}	16		60	ms	
Non-volatile data storage	$t_{MH\ 1}$	10			year	t_{WE} = 20m *3
Non-volatile data storage	$t_{MH\ 2}$	1			year	t_{WE} = 20ms *4
Number of read accesses between writes	N_R	10^6			time	per word

Note) *3. After rewriting 10^4 times Ta = 85°C
*4. After rewriting 10^5 times Ta = 85°C

Pin Description

No.	Type	Symbol	Description
1		V_{SS}	Power supply (IC board) pin
2		V_{GG}	Power supply pin
3		NC	
4		T.VOLT	Used during test (Normally it is open or connected to V_{SS})
5		TEST	Used during test (Normally it is open or connected to V_{SS})
6	IN	CLK	Synchronized clock input
7	IN	C_1	Mode control 1 input
8	IN	C_2	Mode control 2 input
9	IN	C_3	Mode control 3 input
10	IN	CS	Chip selected input (Selected during open or connected to V_{SS} and not selected when connected to V_{GND})
11		NC	
12	I/O	I/O	Data Input/Output and for address I/O pin
13		V_{GND}	Interface voltage pin
14		NC	

Mode Control

The mode selection is controlled by 3 bits of parallel signals such as C1, C2 and C3, and is controlled into the following seven mode.

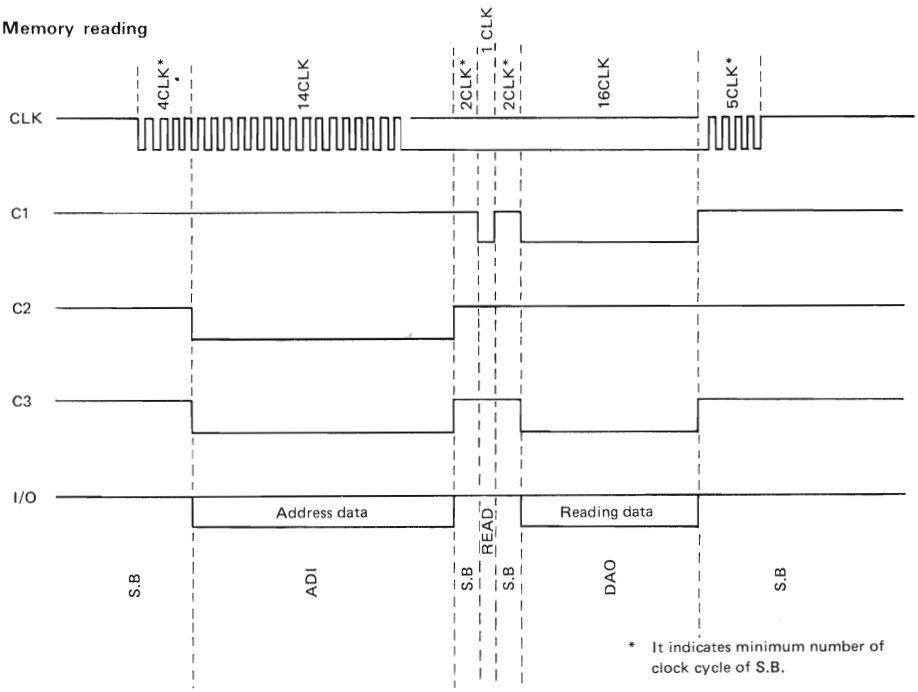
H: V_{SS} level L: V_{GND} level

Mode / Input	S.B	DAO	DAI	WRT	ADI	ERS	READ	NOP
C1	H	L	L	L	H	H	L	H
C2	H	H	L	L	L	L	H	H
C3	H	L	L	H	L	H	H	L

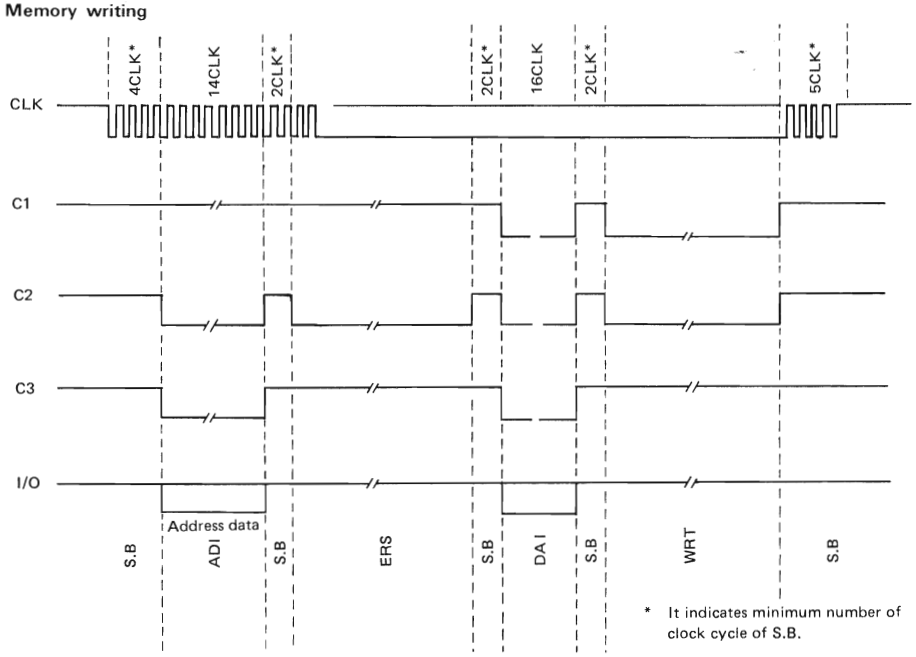
S.B : Standby: Holds the contents of address and data register. The output buffer is left floating.
DAO : Outputs the information of the data register (transferred by READ) from the I/O pin.
DAI : Transfers the information to be memorized to the data register from the I/O pin.
WRT : Writes the information transferred by DAI into the specified address.
ERS : Erases the information memorized in the specified address.
READ : Transfer the memorized information in the specified address to the data register.
ADI : Transfer the address information to be specified to the I/O pin from the address register.
NOP : Not in use.

Neccessary Time Width of Individual Sequences

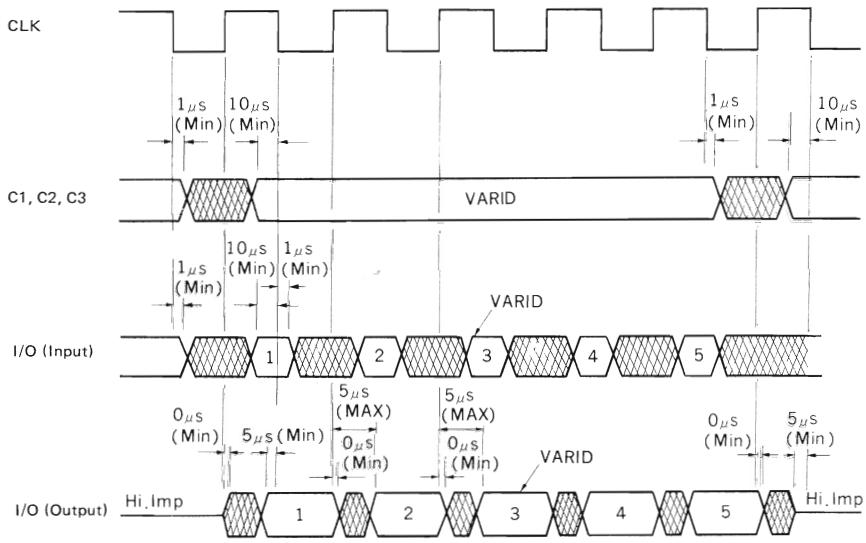
1) Memory reading



2) Memory writing



3) Timing chart



4) Recommended operation

The mode selection signals (C1, C2 and C3) and the input (I/O) are fetched internally only during CLK is at "H". And they are ignored even if selected during CKL is at "L".

Accordingly as shown in Figure above, selection of the signal can be carried out in a wide range. However, on the contrary, it is somewhat to comprehend.

As a result, the following conditions are recommended.

The one clock of the CLK is defined as the L period and the consecutive one as H period.

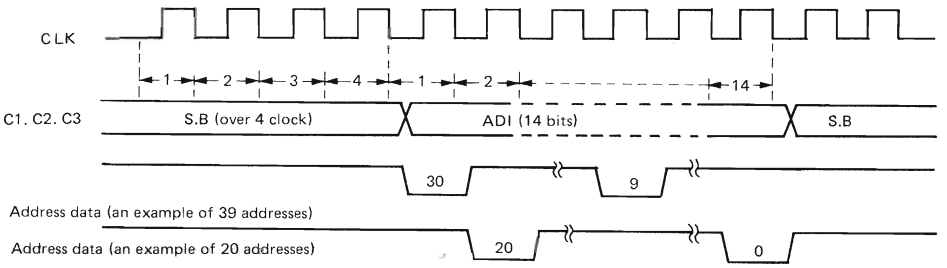
That is, the before half of the one clock is defined as L (VGND) and the latter half as H (V_{SS})

The signal is switched in the before half of the CLK, that is in the L period and fetched into the IC in the latter half period, i.e. in the H period, and thereby starts all the operations.

(1) Memory Reading

Selects a specified word (ADI) and transfers contents of the memory cell into 16 data registers (READ), and then outputs (DAO) the contents of those registers to I/O pin.

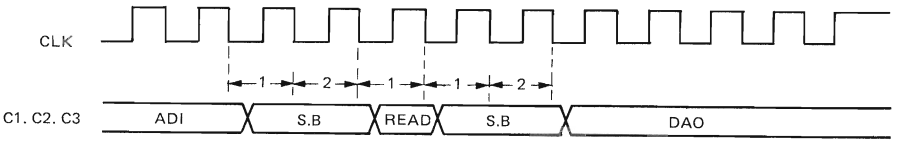
1) ADI



Details of time setting will be described later.

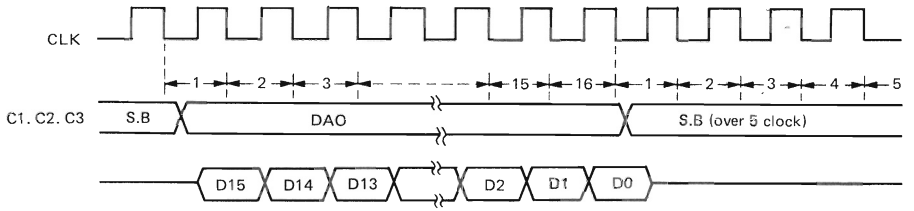
In addition, when address data of more than 14 clocks are input; for example, when 19 clocks are input, the data of the first 5 clocks are ignored and the latter 14 clocks input only can be transferred into the address register.

2) READ

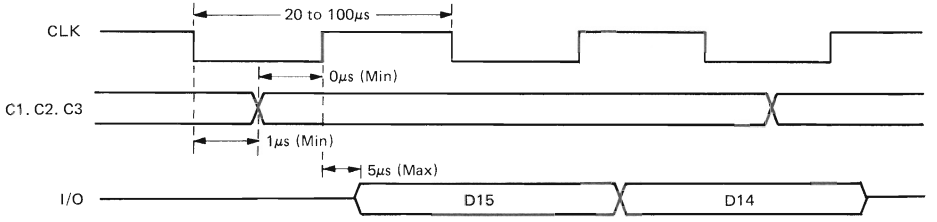


For S.B(standby), over 2 clocks are necessary.

3) DAO



In addition, when over 16 clocks in the DAO section are taken; for example, 20 clocks, the data corresponding to the first 16 clocks are effective, and the rest of 4 clocks being output become indefinite.



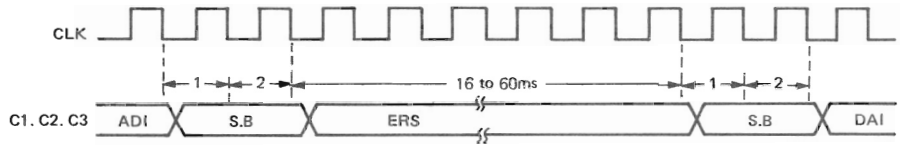
(2) Writing into Memory

Select the specified word (ADI) and erase that word (ERS).
Next, input the data to be written (DAI) and writing (WRT) is performed. Erasure (ERASE) is always necessary before writing (WRITE).

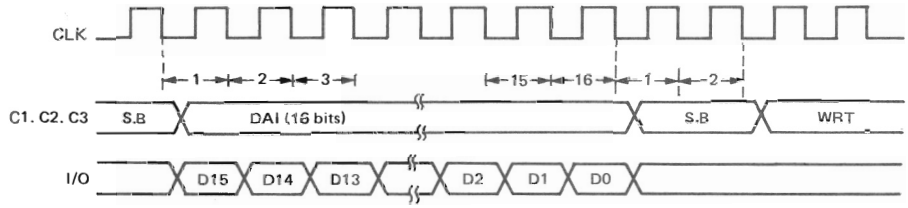
1) ADI

The same as memory reading.

2) ERS

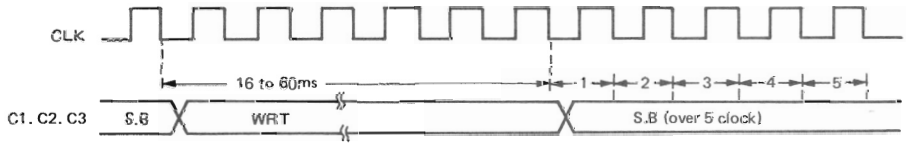


3) DAI



In addition, when over 16 clocks are input; for example, 19 clocks are input, the first 3 clocks are ignored. Therefore only the rest of 16 clocks input can be transferred to the data register.

4) WRT



Others

(1) Caution to be exercised when the POWER switch is ON or OFF.

1) When the POWER switch is ON.
Until the power supply pin V_{GG1} of the CXK1001P reaches $|V_{SS} - V_{GG1}| > 15V$, other power supplies (IC, etc.) should already have been stabilized.

2) When the POWER switch is OFF
After the power supply pin V_{GG1} has become $|V_{SS} - V_{GG1}| \leq 15V$, other power supplies should gradually start to reduce.

(2) CLK

When executing writing and reading, CLK is input, and the clock is generated before 4-bit time in which a series of operations starts, and also during that 4-bit time it should be in the S.B mode. After completing the series of operations, the clock should be generated until reaching the 5-bit time which had become into S.B mode. When CLK is not input, CLK pin should be fixed at H level. (See Figure below.)

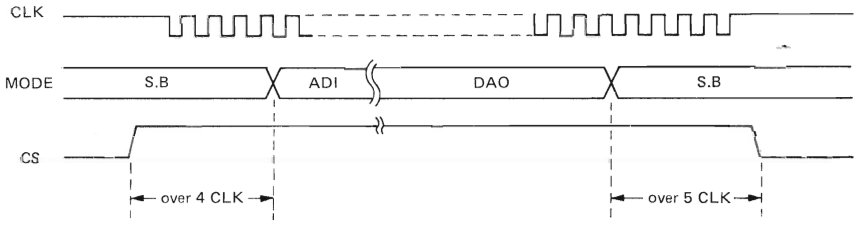
(3) CS

By setting CS pin (10 pin) at H or open, its chip is selected and by setting CS pin at L, the chip becomes unselected.

During unselected state, even if CLK input and mode control inputs C1, C2 and C3 are applied to the chip, it becomes into S.B mode forciblly by prohibiting internally in the IC. I/O Pin output becomes into floating state and therefore expansion of memory contents is possible by commonly connecting many chips and merely CS pin control.

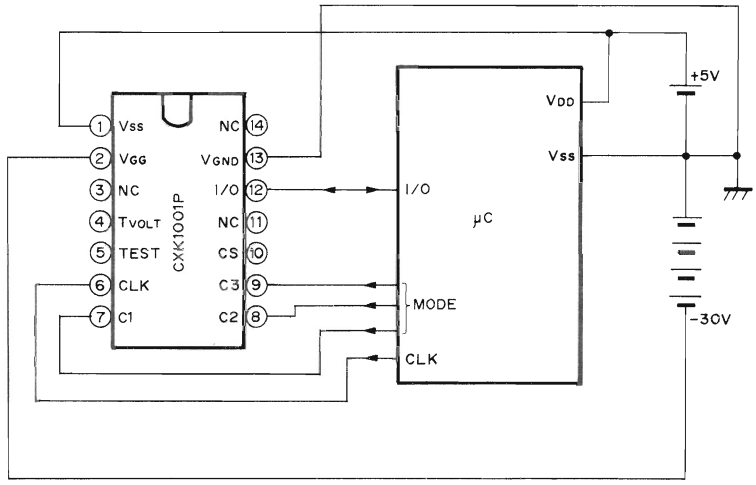
Switchover of CS signal should not be carried out in the course of sequence. Switchover of it should be carried out at a period of over 4 clocks before start of the sequence, and over 5 clocks after the completion of the sequence.

In this case, it is not necessary for the clock to be applied.

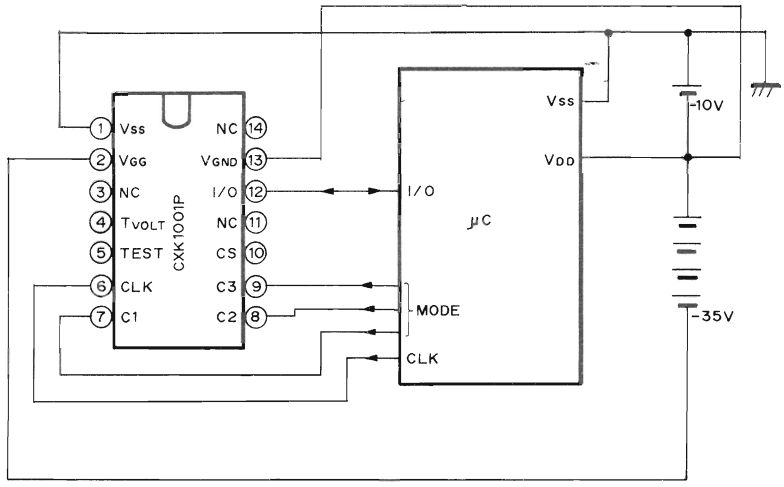


Test Circuits

1. Interface with 5V NMOS and CMOS



2. Interface with 10V PMOS



560-bit (40 word × 14 bit) Non-volatile Memory

Description

The CXK1002P is a 40 word × 14 bit EAROM allowing electrical erase and programming. It is designed using the MNOS process technologies to transmit address and data in serial through a single two-way bus.

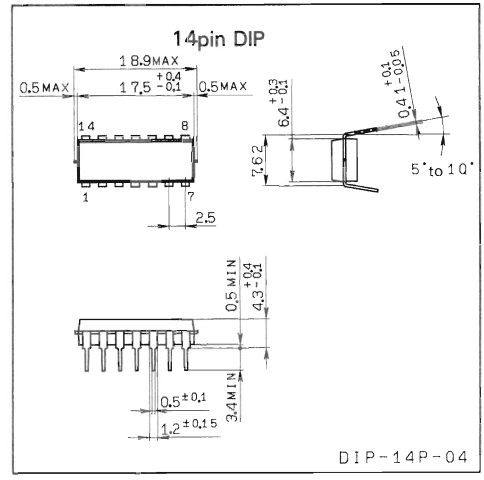
This device is the most suitable for a read-only-memory system requiring repeated rewritings, instantaneously, in the electronic tuner non-volatile channel memory and field.

Features

- Full-decode 40 word × 14 bit composition.
- Rewritable in word units
- Memory storage without power supply .. more than 10 years.
- Write/Erase time ..... 20ms/word.
- −35V single power supply.
- Allowable frequency of writes and erases ..... more than 10^5.
- Low power dissipation design (70 mW Typ.)

Package Outline

Unit:mm



Structure

P-channel MNOS IC

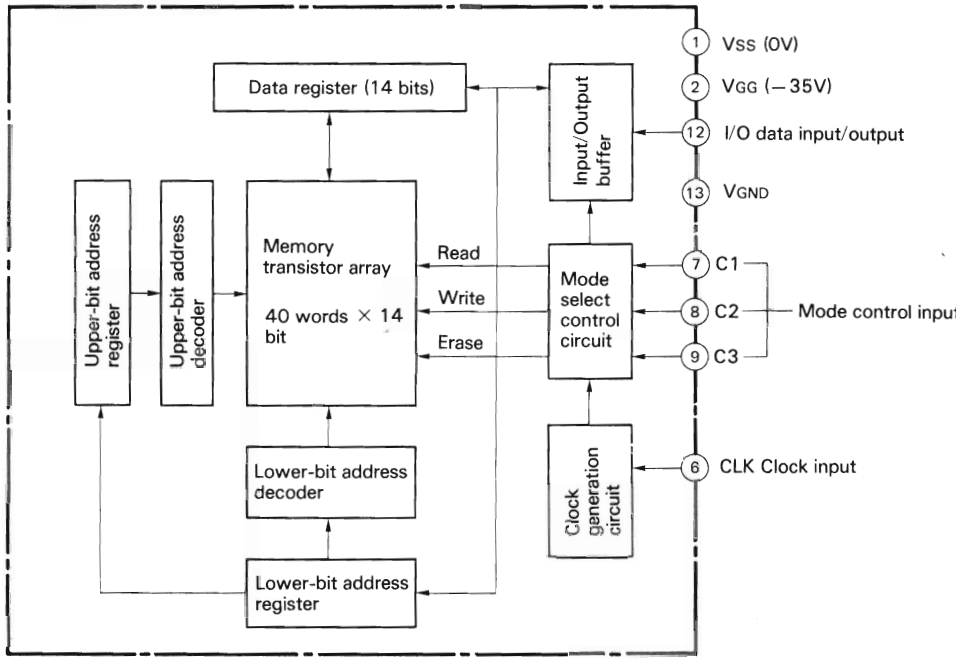
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{GG}	+0.3 to −42	V
• Input voltage	V_I	+0.3 to −20	V
• Operating temperature 1	T_{opr1}	−20 to +75	°C
• Operating temperature 2	T_{opr2}	−20 to +85	°C
	..... memory storage (with power OFF)		
• Storage temperature	T_{stg}	−55 to 150	°C

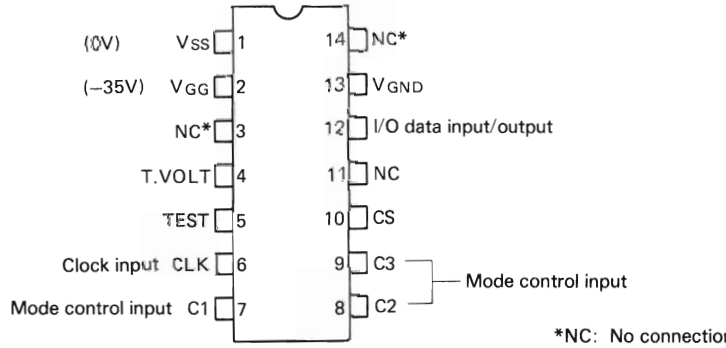
Recommended Operating Conditions (Ta = 25°C)

• Supply voltage 1	$V_{GG} - V_{SS}$	−32.2 to −40	V
• Supply voltage 2	$T_{GND} - V_{SS}$	−4.25 to −14	V
• High level input voltage	V_{INH}	V_{SS} − 1.8 to V_{SS}+0	V
• Low level input voltage	V_{INL}	V_{SS} − 14 to V_{SS} −4.25	V

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Type	Symbol	Description
1		V_{SS}	Power supply (IC board) terminal
2		V_{GG}	Power supply terminal
3		NC	
4		T.VOLT	Used for test. (Usually open or connected to V_{SS})
5		TEST	Used for test. (Usually open or connected to V_{SS})
6	IN	CLK	Sync clock input
7	IN	C_1	Mode control 1 input
8	IN	C_2	Mode control 2 input
9	IN	C_3	Mode control 3 input
10	IN	CS	Chip select input. (Select when open or connected to V_{SS}. Not selected when connected to V_{GND}).
11		NC	
12	I/O	I/O	Data input/output and address input terminal
13		V_{GND}	Interface voltage terminal
14		NC	

Electrical Characteristics 1

(Ta = 25°C)

Item	Symbol	Min.	Typ	Max.	Unit	Remarks
Power supply current	I_{GG}		2.0	3.4	mA	Standby mode
Input pull-up current 1	I_{IN1}	−45	−90	−180	μA	CS input (V_{IN} = −14V)
Input pull-up current 2	I_{IN2}		−10	−30	μA	Other than CS (V_{IN} = −14V)
High level output voltage	V_{OH}	V_{SS}−1			V	I_{OH} = −200μA
Low level output voltage 1	V_{OL1}			V_{GND}+0.5	V	I_{OL} = 40μA *Note 1
Low level output voltage 2	V_{OL2}			V_{GND}+1.0	V	I_{OL} = 500μA *Note 2
Output leakage current	I_{OLK}			±1.0	μA	V_O = −14V

*Note 1) $V_{GND} - V_{SS}$ = −14.0V *Note 2) $V_{GND} - V_{SS}$ = −5.0V

Electrical Characteristics 2

(Ta = 25°C)

Item	Symbol	Min.	Typ	Max.	Unit	Remarks
Clock frequency	f	1 (10)	16	50	kHz	*Note 3
Clock pulse width	ϕ_{WH}	9			μs	H level width
Clock pulse width	ϕ_{WL}	9			μs	L level width
Rise, Fall time	t_{r1}, t_{f1}			10	μs	CS
Rise, Fall time	t_{r2}, t_{f2}			1	μs	Other than CS
Data read out time	t_R			5	μs	
Number of reads	NR	10^6			Times	
Write/Erase time	t_{WE}	16		60	ms	
Memory hold time	t_{MH1}	10			Years	t_{WE} = 20ms *Note 4
Memory hold time	t_{MH2}	1			Years	t_{WE} = 20ms *Note 5

*Note 3) f_{MIN} = 10kHz only in the READ mode. *Note 4) Ta = 85°C after REWRITEs 10^4 times.
*Note 5) Ta = 85°C after REWRITEs 10^5 times.

Description of Functions

The CXK1002P is specified in two 1-OUT-OF-10 codes with continuous addresses. Mode selection is specified, using the 3 bit parallel signals C1 to C3, in 7 modes: address input, data input, data output, data erase, write, read and standby.

Data programming is performed by selectively inputting the internally-generated negative pulse to the MNOS memory transistor and inserting the charge into the gate insulating film SiO_2-Si_3N_4 with a tunnel effect.

Mode Control

Mode selection is controlled in the following seven modes using the 3 bit parallel signals, C1, C2 and C3.

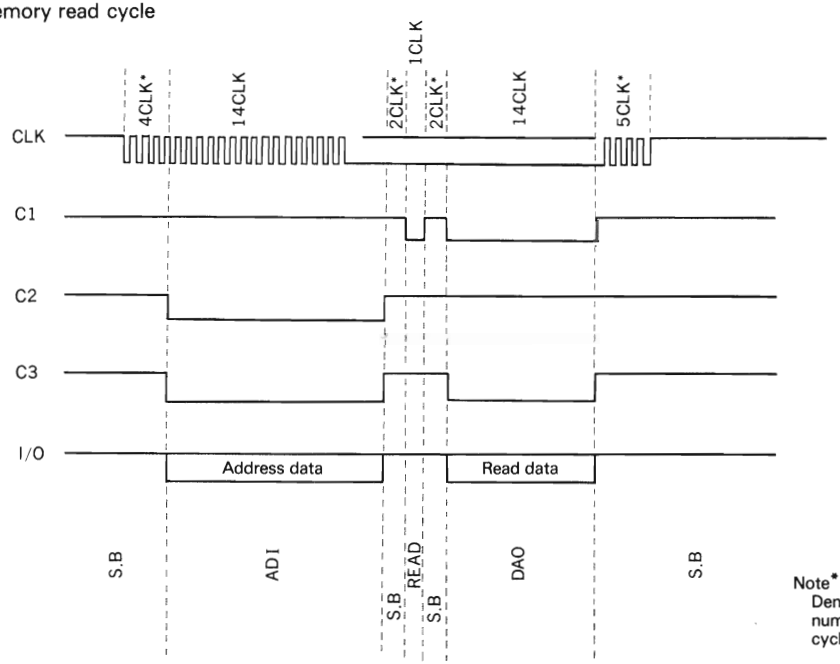
(H: V_{SS} lelvel L: V_{SS} level)

Input \ Mode	S.B	DAO	DAI	WRT	ADI	ERS	READ	NOP
C1	H	L	L	L	H	H	L	H
C2	H	H	L	L	L	L	H	H
C3	H	L	L	H	L	H	H	L

S.B : Holds contents of the standby address and data register. The output buffer becomes floating.
DAO : Outputs the data register information (transferred by READ) from the I/O terminal.
DAI : Transfers information to be stored from the I/O terminal to the data register.
WRT : Writes, in a specified address, information transferred in the DAI mode.
ERS : Erases information stored in a specified address.
READ : Transfers information stored, in a specified address, to the data register.
ADI : Transfers information, in a address, to be specified from the I/O terminal, to the address register.
NOP : Not in use.

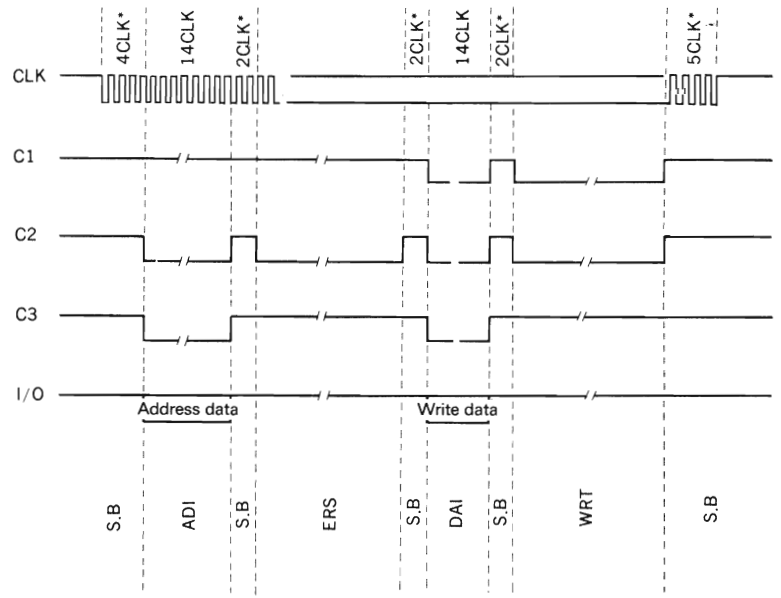
Required Time Width of Each Sequence

1) Memory read cycle



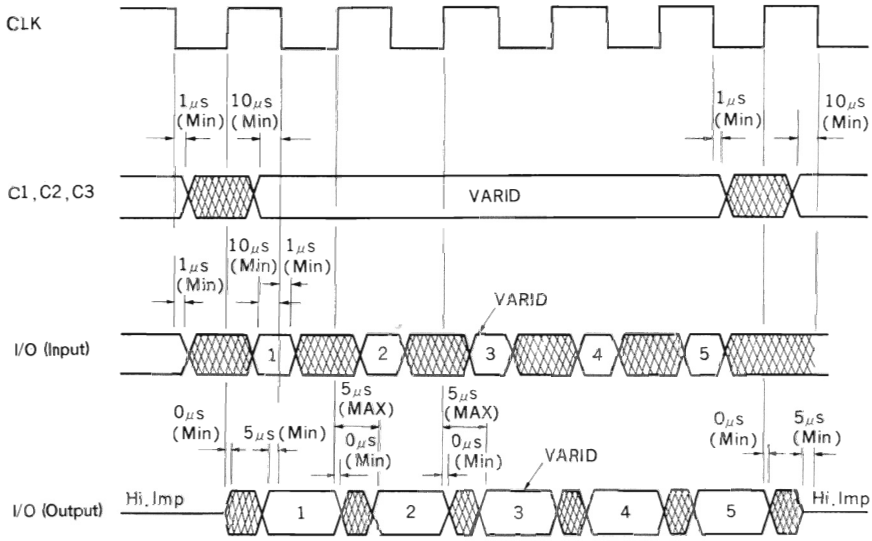
Note*
Denotes the smallest number of S.B clock cycle.

2) Memory write cycle



Note*
Denotes the smallest number of S.B clock cycle.

3) Mode switching, Input/Output timing



4) Recommended operations

The mode switching signals (C1, C2 and C3) and input signal (I/O) are accepted internally only when CLK is at H and disregarded when CLK is at LOW.

Accordingly, the signal switching can be performed in a wide range as shown in the above diagram, but switching is not so easy to understand.

Therefore, the following conditions are recommended.

CLK should be one clock covering an L period and its succeeding H period.

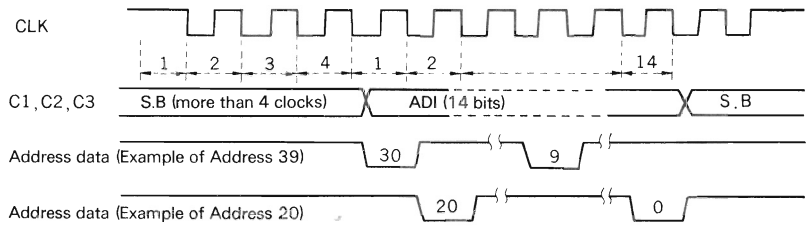
That is, one clock is divided into the first half L (V_{GND}) and the 2nd half H (V_{SS}).

Then, the signal is switched in the 1st half CLK (L period) and accepted into the IC in the 2nd half H period, starting the entire operation.

(1) Memory read out

Select a specific word (ADI), transfer the memory cell contents to a 16 bit data register (READ) and then output its register contents to the I/O terminal (DAO).

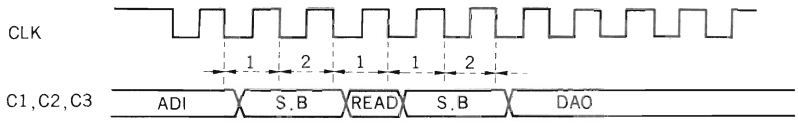
1) ADI



Details of time setting will be described later.

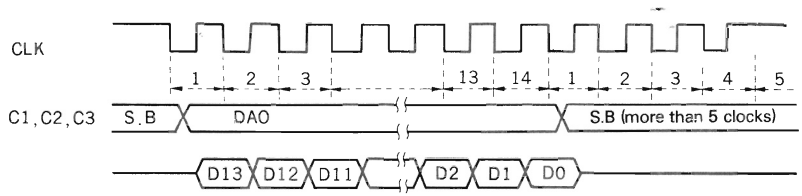
When more than 14 clocks of address data (e.g.19 clocks) are input, data of the first 5 clocks are disregarded and the data of 14 clocks, only, are transferred to the address register.

2) READ

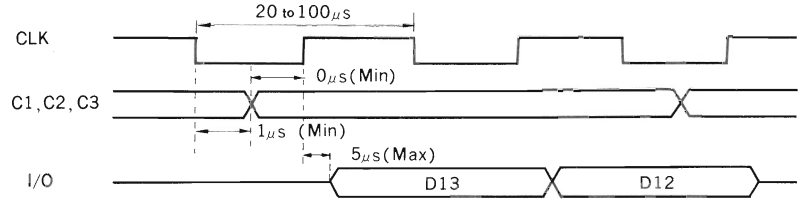


S.B (Standby) requires more than 2 clocks.

3) DAO



When more than 14 clocks of DAO period (e.g.20 clocks) are input, the first 14 clock data, only, 15 effective and the succeeding 6 clock data is disregarded.



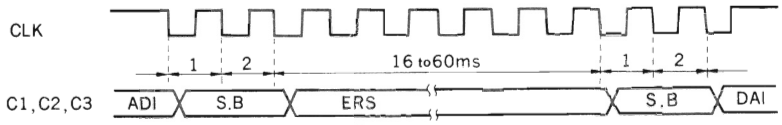
(2) Memory write

Select a specific word (ADI) and erase the word (RES).
Then, input the data to be written (DAI) and write (WRT).
Ensure to erase (ERASE) before write (WRITE).

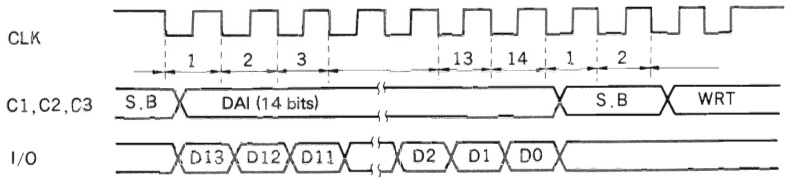
1) ADI

Same as in the memory read out.

2) ERS

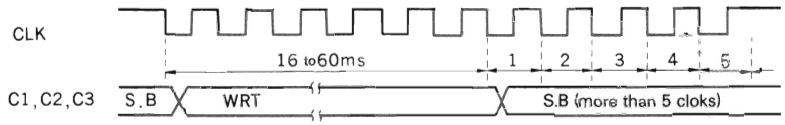


3) DAI



When more than 14 clock data (e.g.19 clocks) is input, the first 5 clock data is disregarded and the last 14 clock data, only, is transferred to the data register.

4) WRT



5) Others

(1) Cautions when switching power supply ON or OFF.

1) ON

Before the CXK1002P power supply terminal V_{GG} reaches $|V_{SS}-V_{GG}| > 15V$, the other power supply (IC, etc) must be sufficiently stable.

2) OFF

After $|V_{SS}-V_{GG}| \leqq 15V$, the other power supply must start decreasing in voltage.

(2) CLK

Clocks are input for write or read, the clocks must generate in 4bit time before the operations and be in the S.B mode during the 4bit time. After the series of operations, generate up to the S.B mode in 5bit time. While clocks are not input, fix the CKL terminal to the H level.

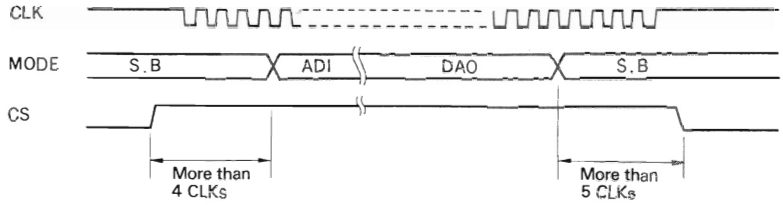
(3) CS

By setting the CS terminal (Pin 10) to H or open, the chip is selected; when set to L, the chip is not selected.

When the chip is not selected, external inputs of CLK and mode control signals of C_1, C_2 and C_3 are inhibited internally in the IC, and the S.B mode is forcibly activated. In this case, because the I/O outputs start floating, the memory capacity can be expanded only with an CS terminal control that has many chips connected in common.

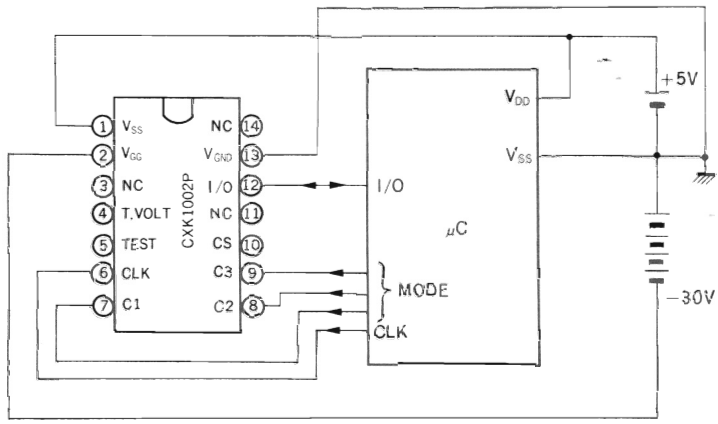
Do not switch the CS signal during the sequence. switch 4 clocks before the sequence start or switch 5 clocks after its completion. When the CS signal is switched while the clock is at L,malfunction may result depending on a combination of C_1, C_2 and C_3. (The mode might be changed to ERS, WRT or DAO).

As malfunction often results when the CS terminal is switched from H to L, ensure the switching while the clock is at H.

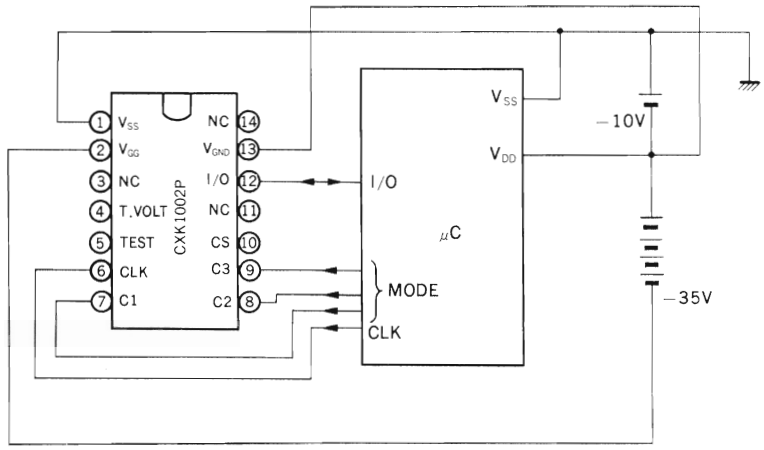


Test Circuits

1. Interface with 5 V NMOS, CMOS



2. Interface with 10 V PMOS



320-bit (20 word × 16 bit) Non-volatile Memory

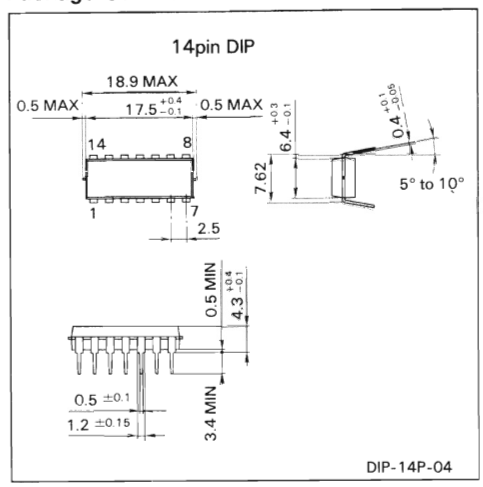
Description

The CXK1003P is a 20 word × 16 bit EAROM allowing electrical erase and programming. It is designed using the MNOS process technologies to transmit address and data serially through a single two-way bus.

This device is the most suitable for a read-only-memory system requiring repeated rewritings, instantaneously, in the electronic tuner non-volatile channel memory and field.

Package Outline

Unit:mm



Features

- Full-decode 20 word × 16 bit composition.
- Rewritable in word units
- Memory storage without power supply .. more than 10 years.
- Write/Erase time ..... 20ms/word.
- −35V single power supply.
- Allowable number of writes and erases ..... more than 10^5.
- Low power consumption design (70 mW typ.).

Structure

P-channel MNOS IC

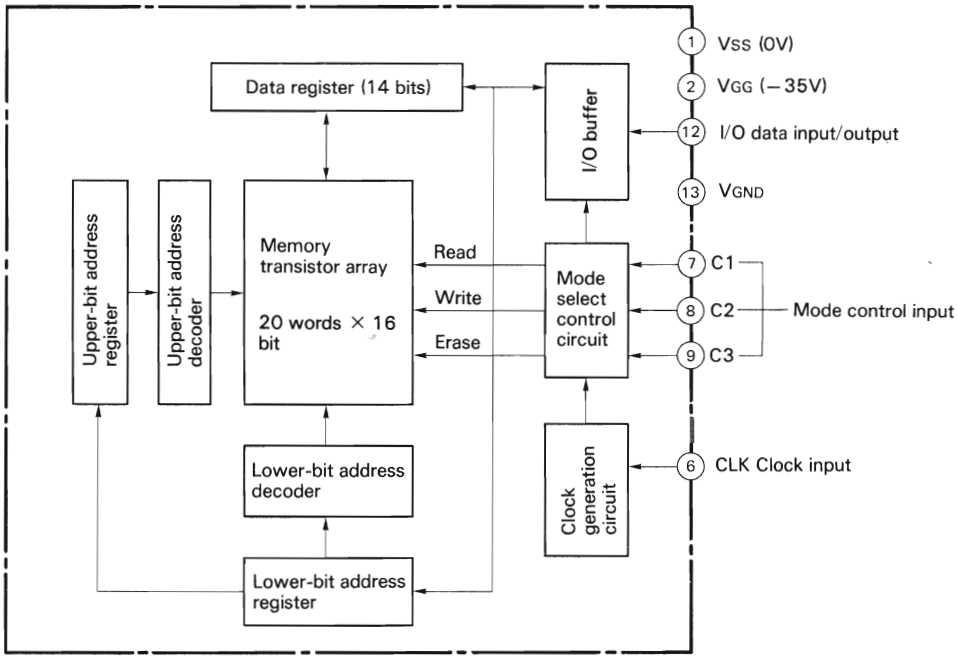
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{GG}	+0.3 to −42	V
• Input voltage	V_I	+0.3 to −20	V
• Operating temperature 1	T_{opr1}	−20 to +75	°C
• Operating temperature 2	T_{opr2}	−20 to +85	°C
	..... memory hold condition (with power off)		
• Storage temperature	T_{stg}	−55 to 150	°C

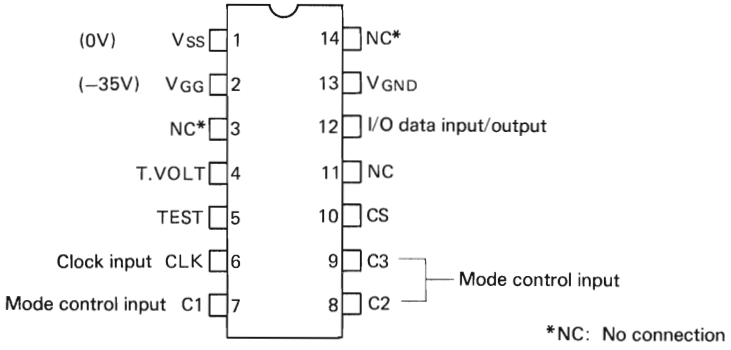
Recommended Operating Conditions (Ta = 25°C)

• Supply voltage 1	$V_{GG} - V_{SS}$	−32.2 to −40	V
• Supply voltage 2	$T_{GND} - V_{SS}$	−4.25 to −14	V
• High level input voltage	V_{INH}	V_{SS} − 1.8 to V_{SS}+0	V
• Low level input voltage	V_{INL}	V_{SS} − 14 to V_{SS} −4.25	V

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Type	Symbol	Description
1		V_{SS}	Power supply (IC board) pin
2		V_{GG}	Power supply pin
3		NC	
4		T.VOLT	Used for test. (Usually open or connected to V_{SS})
5		TEST	Used for test. (Usually open or connected to V_{SS})
6	IN	CLK	Sync clock input
7	IN	C_1	Mode control 1 input
8	IN	C_2	Mode control 2 input
9	IN	C_3	Mode control 3 input
10	IN	CS	Chip select input. (Select when open or connected to V_{SS}. Not selected when connected to V_{GND}).
11		NC	
12	I/O	I/O	Data I/O and address input pin
13		V_{GND}	Interface voltage pin
14		NC	

Electrical Characteristics 1

(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply current	I_{GG}		2.0	3.4	mA	Standby mode
Input pull-up current 1	I_{IN1}	−45	−90	−180	μA	CS input (V_{IN} = −14V)
Input pull-up current 2	I_{IN2}		−10	−30	μA	Other than CS (V_{IN} = −14V)
High Level output voltage	V_{OH}	V_{SS}−1			V	I_{OH} = −200μA
Low level output voltage 1	V_{OL1}			V_{GND}+0.5	V	I_{OL} = 40μA *1
Low level output voltage 2	V_{OL2}			V_{GND}+1.0	V	I_{OL} = 500μA *2
Output leakage current	I_{CLK}			±1.0	μA	V_O = −14V

*1) $V_{GND} - V_{SS}$ = −14.0V *2) $V_{GND} - V_{SS}$ = −5.0V

Electrical characteristics 2

(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Clock frequency	f	1 (10)	16	50	kHz	*3
Clock pulse width	ϕ_{WH}	9			μs	H level width
Clock pulse width	ϕ_{WL}	9			μs	L level width
Rise, Fall time	t_{r1}, t_{f1}			10	μs	CS
Rise, Fall time	t_{r2}, t_{f2}			1	μs	Other than CS
Data read out time	t_R			5	μs	
Number of reads	NR	10^6			Times	
Write/Erase time	t_{WE}	16		60	ms	
Memory hold time	t_{MH1}	10			Years	t_{WE} = 20ms *4
Memory hold time	t_{MH2}	1			Years	t_{WE} = 20ms *5

*3) f_{MIN} = 10kHz only in the READ mode.
*4) Ta = 85°C after REWRITEs 10^4 times.
*5) Ta = 85°C after REWRITEs 10^5 times.

Description of Function

The CXK1003P is specified in two 1-OUT-OF-10 codes with continuous addresses. Mode selection is specified, using the 3 bit parallel signals C1 to C3, in 7 modes: address input, data input, data output, data erase, write, read and standby.

Data programming is performed by selectively inputting the internally-generated negative pulse to the MNOS memory transistor and inserting the charge into the gate insulating film SiO_2-Si_3N_4 with a tunnel effect.

Mode Control

Mode selection is controlled in the following seven modes using the 3 bit parallel signals, C1, C2 and C3.

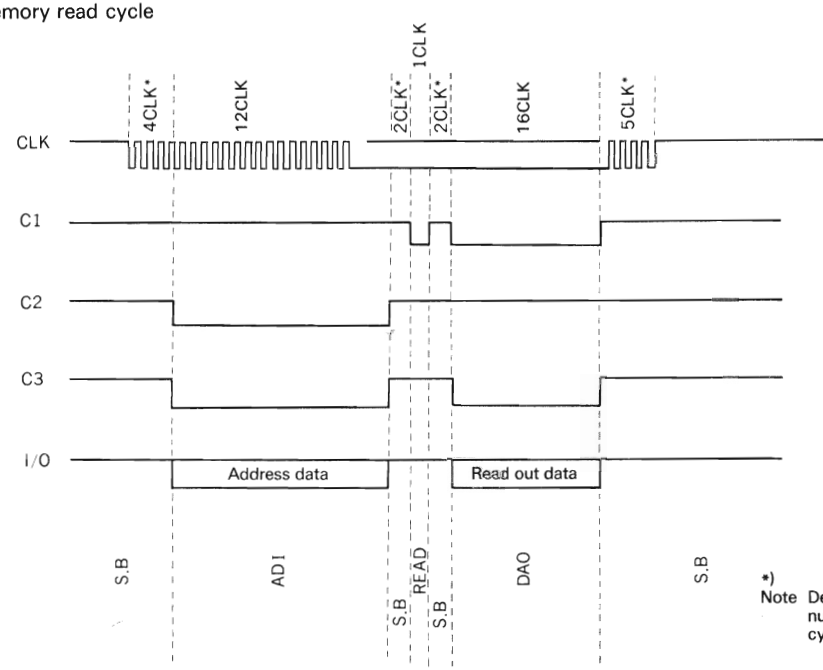
(H: V_{SS} level L: V_{SS} level)

Input \ Mode	S.B	DAO	DAI	WRT	ADI	ERS	READ	NOP
C1	H	L	L	L	H	H	L	H
C2	H	H	L	L	L	L	H	H
C3	H	L	L	H	L	H	H	L

S.B : Holds contents of the standby address and data register. The output buffer becomes floating.
DAO : Outputs the data register information (transferred by READ) from the I/O pin.
DAI : Transfers information to be stored from the I/O pin to the data register.
WRT : Writes, in a specified address, information transferred in the DAI mode.
ERS : Erases information stored in a specified address.
READ : Transfers information stored, in a specified address to the data register.
ADI : Transfers information, in a address, to be specified from the I/O pin, to the address register.
NOP : Not in use.

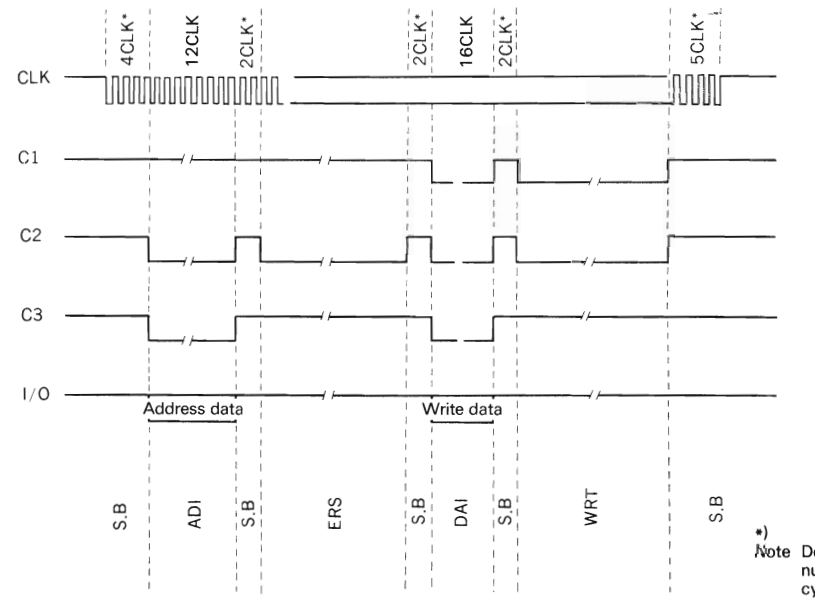
Required Time Width of Each Sequence

1) Memory read cycle



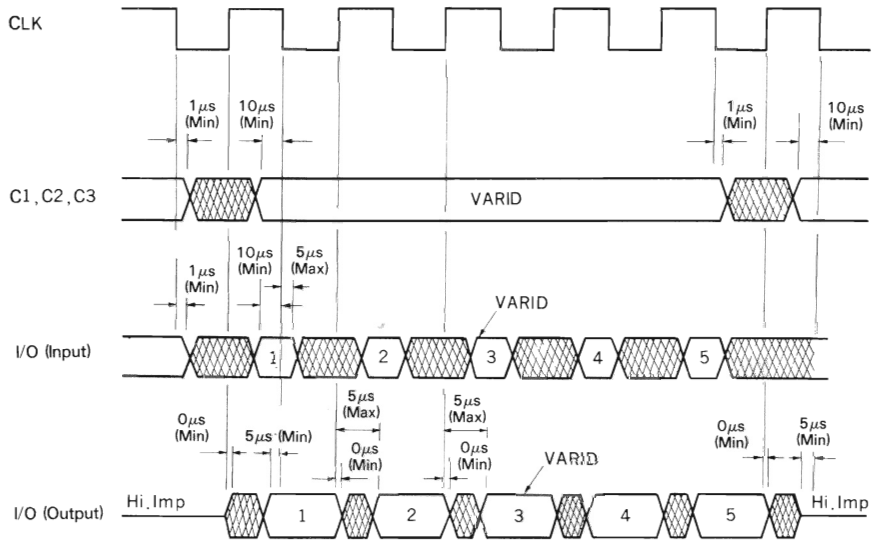
*) Note Denotes the smallest number of S.B clock cycle.

2) Memory write cycle



*) Note Denotes the smallest number of S.B clock cycle.

3) Mode switching, I/O timing



4) Recommended operations

The mode switching signals (C1, C2 and C3) and input signal (I/O) are accepted internally only when CLK is at H and disregarded when CLK is at Low.

Accordingly, the signal switching can be performed in a wide range, as shown in the above diagram; switching, however, is not so easy to understand.

Therefore, the following conditions are recommended.

CLK should be one clock covering an L period and its succeeding H period.

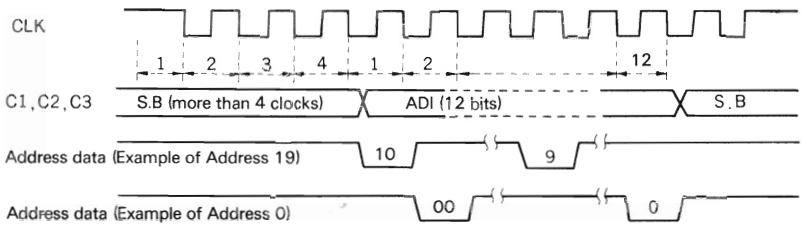
That is, one clock is divided into the first half L (V_{GND}) and the 2nd half H (V_{SS}).

Then, the signal is switched in the 1st half CLK (L period) and accepted into the IC in the 2nd half H period, starting the entire operation.

(1) Memory read out

Select a specific word (ADI), transfer the memory cell contents to a 16 bit data register (READ) and then output its register contents to the I/O pin (DAO).

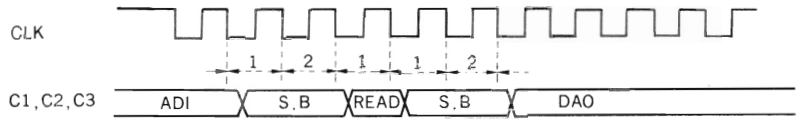
1) ADI



Details of time setting will be described later.

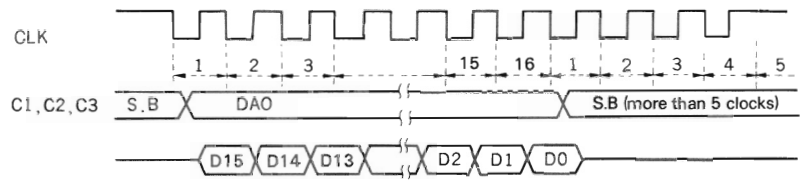
When more than 12 clocks of address data (e.g.19 clocks) is input, data of the first 7 clocks is disregarded and the data of 12 cloks, only, is transferred to the address register.

2) READ

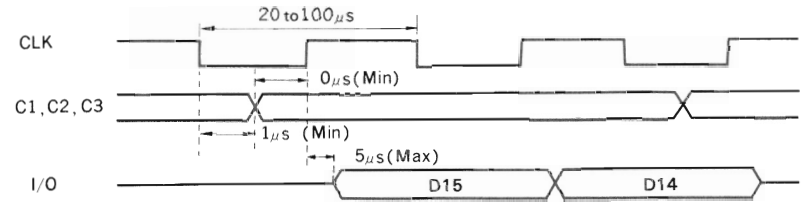


S.B (Standby) requires more than 2 clocks.

3) DAO



When more than 16 clocks of DAO period (e.g.20 clocks) are input, the first 16 clock data, only, is effective and the succeeding 4 clock data is disregarded.



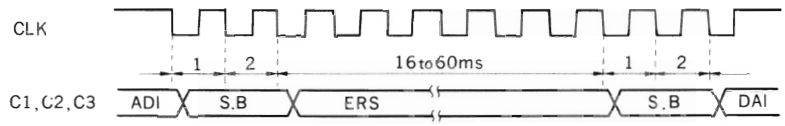
(2) Memory write

Select a specific word (ADI) and erase the word (RES).
Then, input the data to be written (DAI) and write (WRT).
Ensure to erase (ERASE) before write (WRITE).

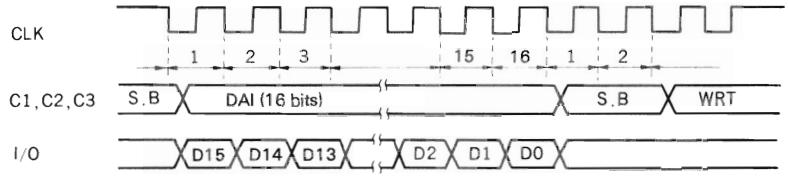
1) ADI

Same as in the memory read.

2) ERS

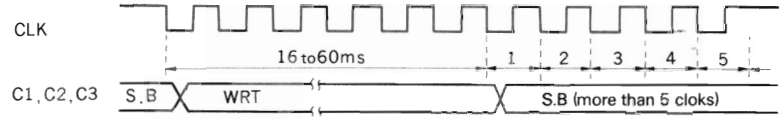


3) DAI



When more than 16 clock data (e.g.19 clocks) is input, the first 3 clock data is disregarded and the last 16 clock data, only, is transferred to the data register.

4) WRT



5) Others

(3) Cautions when switching the power supply ON or OFF.

1) ON

Before the CXK1003P power supply pin V_{GG} reaches $|V_{SS}-V_{GG}| > 15V$, the other power supply (IC, etc) must be sufficiently stable.

OFF

After $|V_{SS}-V_{GG}| \leqq 15V$, the other power supply must start decreasing in voltage.

2) CLK

Clocks are input for write or read, the clocks must generate in 4bit time before the operations and be in the S.B mode during the 4bit time. After the series of operations, generate up to the S.B mode in 5bit time. While clocks are not input, fix the CLK pin to the H level.

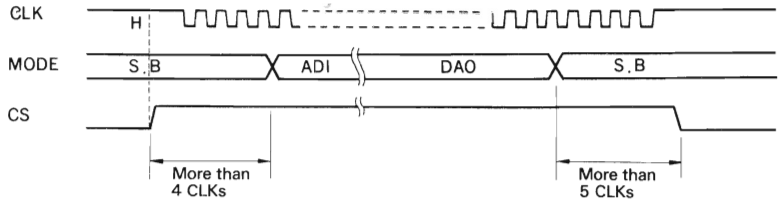
3) CS

By setting the CS pin (Pin 10) to H or open, the chip is selected; when set to L, the chip is not selected.

When the chip is not selected, external inputs of CLK and mode control signals of C_1, C_2 and C_3 are inbibited internally in the IC, and the S.B mode is forcibly activated. In this case. because the I/O outputs start floating, the memory copacity can be expanded only with CS pin control that has many chips connected in common.

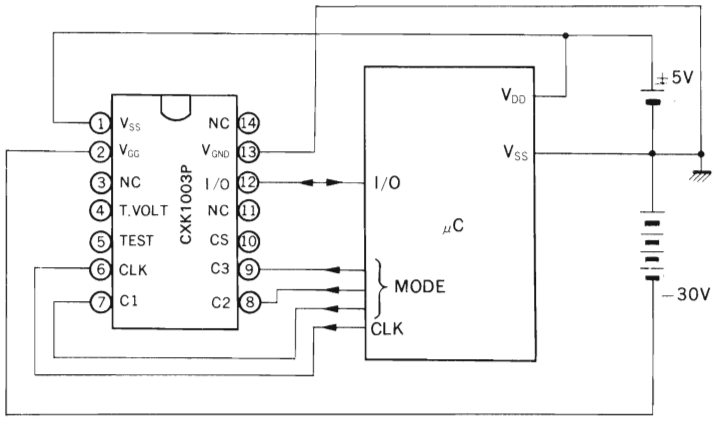
Do not switch the CS signal during the sequence. Switch 4 clocks before the sequence start or switch 5 clocks after its completion. When the CS signal is switched while the clock is at L. malfunction may result depending on a combination of C_1, C_2 and C_3. (The mode might be changed to ERS, WRT or DAO).

As malfunction often results when the CS pin is switched from H to L, ensure the switching while the clock is at H.

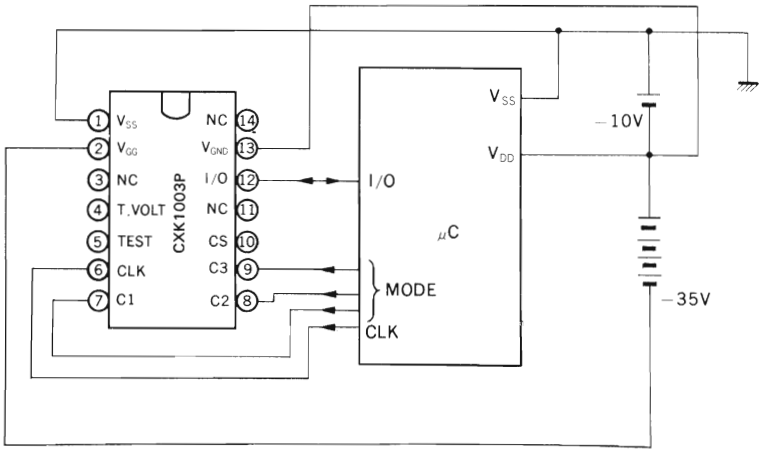


Test Circuits

1. Interface with 5 V NMOS, CMOS



2. Interface with 10 V PMOS



SONY

CXK1004L

512-bit (32 word × 16 bit) Non-Volatile Memory

Description

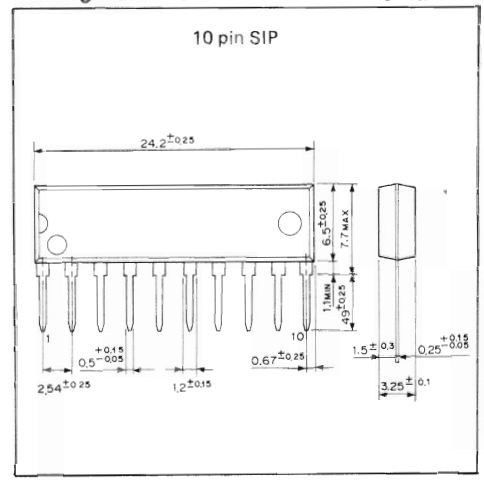
The CXK1004L is an electrically erasable and programmable E^2PROM of 32 words × 16 bit structure, employing the non-volatile memory transistors of the MNOS type.

As the sequence controller is built-in the IC and the control signals necessary for operations are generated within the IC, the chip can be controlled with fewer program steps.

The IC built-in a charge pump circuit and all the operations can be performed with only the 5V power supply. It requires no high voltage, and it is so designed as to require low power consumption (20 mW Typ). It has non-volatile channel memory for the electronic tuner and a most suitable read-only memory system that can be rewritten immediately any time when necessary in the field.

Package Outline

Unit: mm



Features

- Single 5V power supply
- 32 words × 16 bit structure of full decoding
- Rewritable in 1-word unit
- Memory retention time of more than 10 years with no power supply
- Number of erasures and writings of more than 10^5 times
- Built-in sequence controller
- Built-in timing circuit for erasure of writing
- 4 bit I/O control
- Low power consumption design (20 mW Typ.)

Structure

P-channel MNOS IC

Absolute Maximum Ratings (Ta=25°C)

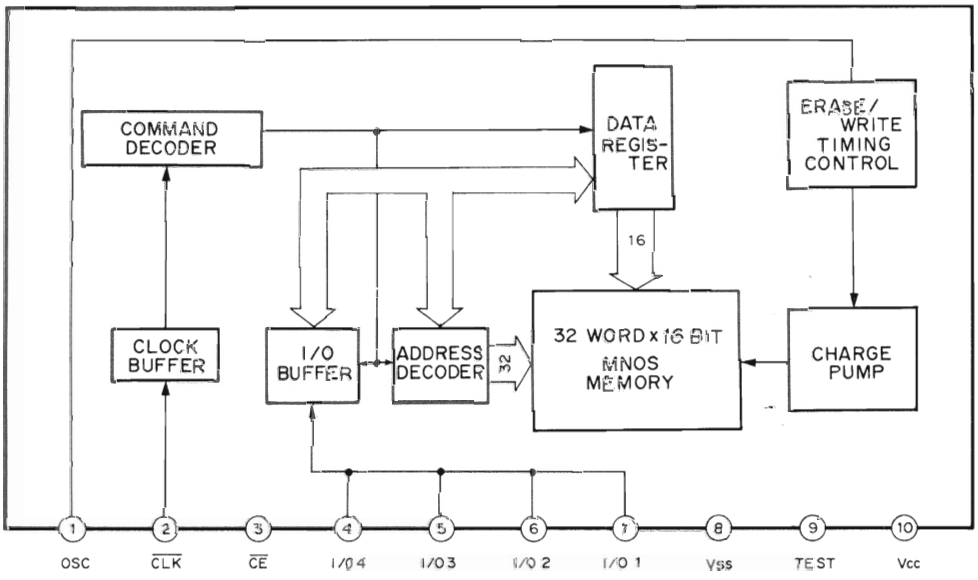
• Supply voltage	V_{CC}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3* to Vcc+0.3*	V
• Operating temperature	Topr	−20 to +75	°C (CXK1004L)
	Topr	−40 to +85	°C (CXK1004L-1)
• Storage temperature	Tstg	−55 to +150	°C

***Note)** This value is at normal condition, it may be 0.5V at the transient time (20 to 30 ms).

Recommended Operating Conditions (Ta=−20 to +75°C, Vss=0V)

• Supply voltage	V_{CC}	4.5 to 5.5	V
• Clock frequency	f_{CLK}	DC to 50	kHz
• High level input voltage	V_{INH1}	V_{CC}−1.5 to V_{CC}	V
• Low level input voltage	V_{INL1}	0 to V_{CC}−3.5	V
• High level input voltage (OSC pin)	V_{INH2}	V_{CC}−0.5 to V_{CC}	V
• Low level input voltage (OSC pin)	V_{INL2}	0 to 1.5	V

Block Diagram and Pin Configuration (Top View)



Pin Description

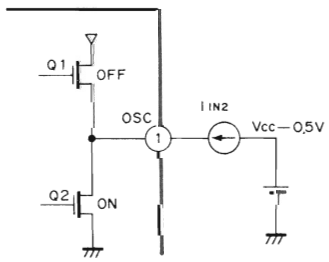
No.	I/O	Symbol	Description
1	I	OSC	Oscillation pin
2	I	$\overline{CLK}$	Sync clock input pin
3	I	$\overline{CE}$	Chip enable input
4	I/O	I/O4	Address and data I/O pin 4
5	I/O	I/O3	Address and data I/O pin 3
6	I/O	I/O2	Address and data I/O pin 2
7	I/O	I/O1	Address and data I/O pin 1
8		Vss	Power supply pin
9		TEST	Test input pin (normally connected to Vcc)
10		Vcc	Power supply pin

Electrical Characteristics 1

(Ta=−20 to +75°C, Vcc=5V±10%, Vss=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply current	Icc	Vcc	*1		4	6	mA
Input pull-up current	IIU	$\overline{CLK}$, $\overline{CE}$		−45	−90	−180	μA
Input leakage current	IILK	All input pins				±20	μA
Output leakage current	IOLK	All output pins				±20	μA
Output voltage high level 1	VOH1	I/O1 to I/O4	IOH=−0.5mA	Vcc−1.0			V
Output voltage low level 1	VOL1	I/O1 to I/O4	IOL=+0.5mA			+1.0	V
Input current 2 *2	IIN2	OSC	VIN2= Vcc−0.5V		1.0	1.5	mA

Note) *1 Includes the erasure and write times.
*2 Only during tOSCH (see Timing Chart (3))



In case when OSC pin is controled by external controller, control IC is required to have more than 1.5 mA of drive-capability because Q2 is on state during tOSCH and enough current is required.

During tE and tW, both Q1 and Q2 are off state and OSC pin is at high impedance.

During the period other than Erase/Write, only Q1 is on state (RON=10 kΩ typ.) and OSC pin is pulled up.

Electrical Characteristics 2

(Ta=−20 to +75°C, V_{CC}=5V±10%, V_{SS}=0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse width	t_{WH}		10			μs
Clock pulse width	t_{WL}		10			μs
Data input setup time	t_{DS}		0			μs
Data input hold time	t_{DH}		0			μs
Rise/fall time	tr, tf				1	μs
Clock setup time	t_{CKS}		10			μs
Data delay time	t_{OD}				5	μs
Number of read	N_R	Refresh time	10^7	10^9		time
Write time	t_W	C=0.47μF, R=150kΩ		30	60	ms
Erasure time	t_E	C=0.47μF, R=150kΩ		30	60	ms
Memory retention time 1	t_{MH1}	After rewriting 10^4 times Store at Ta=85°C	10			year
Memory retention time 2	t_{MH2}	After rewriting 10^5 times Store at Ta=85°C	1			year

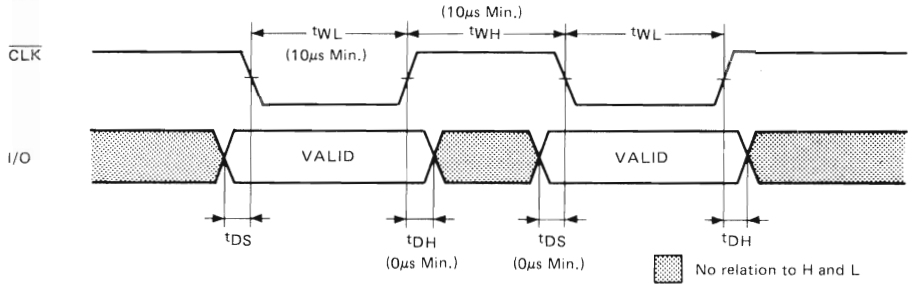
Command Table

$\overline{CE}$	I/O1	I/O2	I/O3	I/O4	Operational command
L	L	L	H	L	DR: Memory read
L	H	L	H	L	DW: Memory write
L	X	X	L	L	No operation
L	X	X	L	H	No operation
L	X	X	H	H	No operation
H	X	X	X	X	No operation

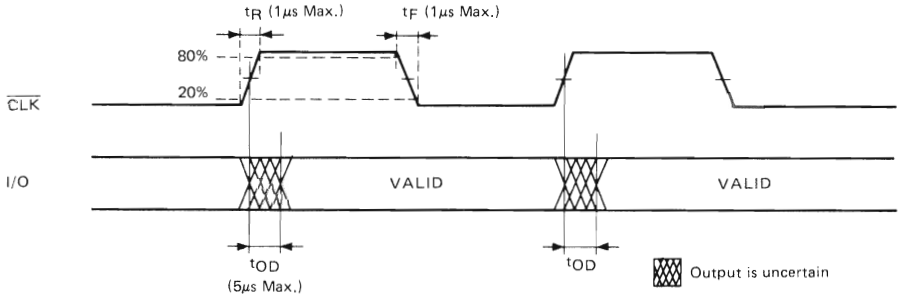
Note) X denotes no relationship.

I/O Timing Chart

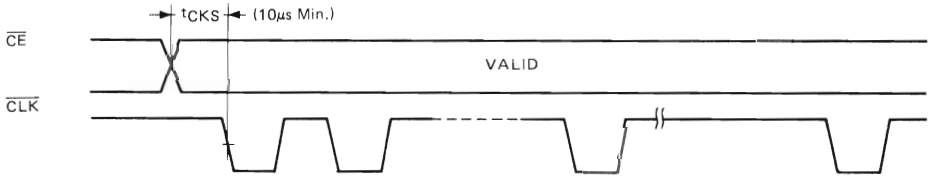
Input Mode



Output Mode

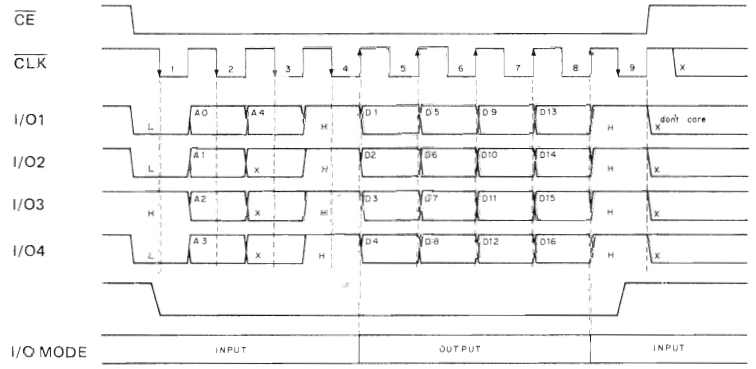


Access Mode

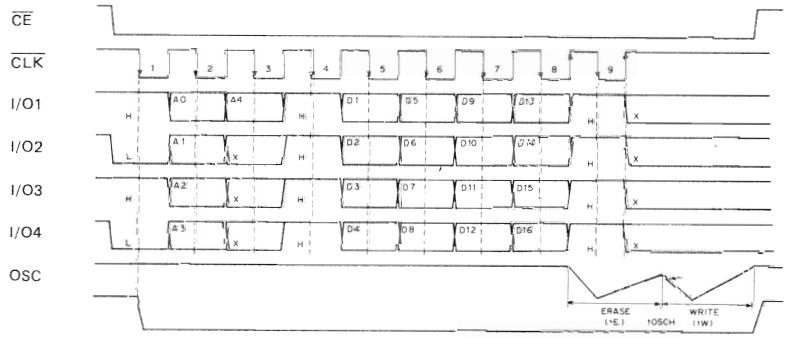


Timing Chart

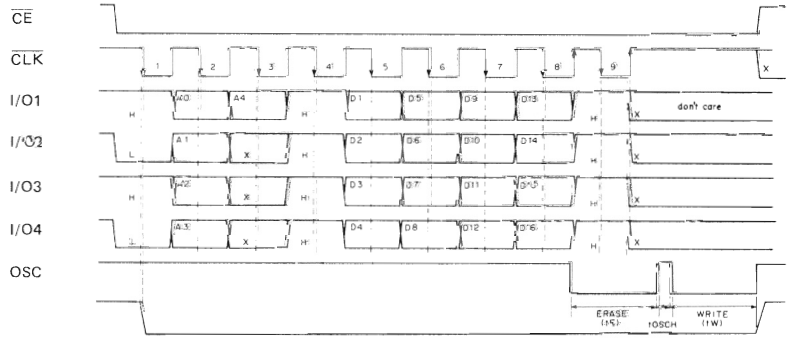
(1) DR: Data Read



(2) DW1: Data Write 1



(3) DW2: Data Write 2



Item	Min.	Max.
tE	30msec	
tW	30msec	
tOSCH	5μsec	50μsec

512-bit (32 word × 16 bit) Non-Volatile Memory

Description

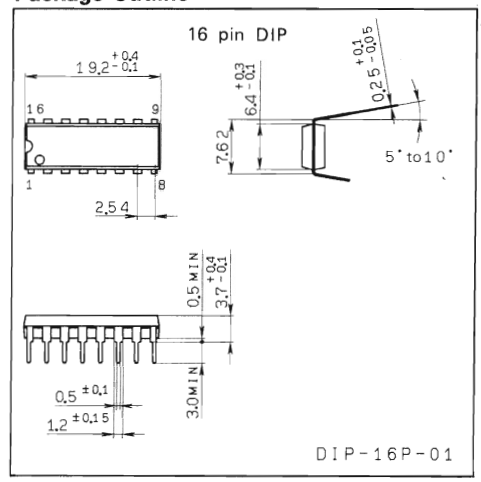
The CXK1005P is an electrically erasable and programmable E^2PROM of 32 word × 16 bit structure, employing the non-volatile memory transistors of the MNOS type.

As the sequence controller is built-in the IC and the control signals necessary for operations are generated within the IC, the chip can be controlled with fewer program steps.

The IC built-in a charge pump circuit and all the operations can be performed with only the 5V power supply. It requires no high voltage, and it is so designed as to require low power consumption (20 mW Typ.). It has a non-volatile channel memory for the electronic tuner and a most suitable read-only memory system that can be rewritten immediately any time when necessary in the field.

Package Outline

Unit: mm



Features

- Single 5V power supply
- 32 word × 16 bit structure of full decoding
- Rewritable in 1-word unit
- Memory retention time of more than 10 years with no power supply
- Number of erasures and writings of more than 10^5 times
- Built-in sequence controller
- Built-in timing circuit for erasure of writing
- 4-bit I/O control
- Low power consumption design (20 mW Typ.)

Structure

P-channel MNOS IC

Absolute Maximum Ratings (Ta=25°C)

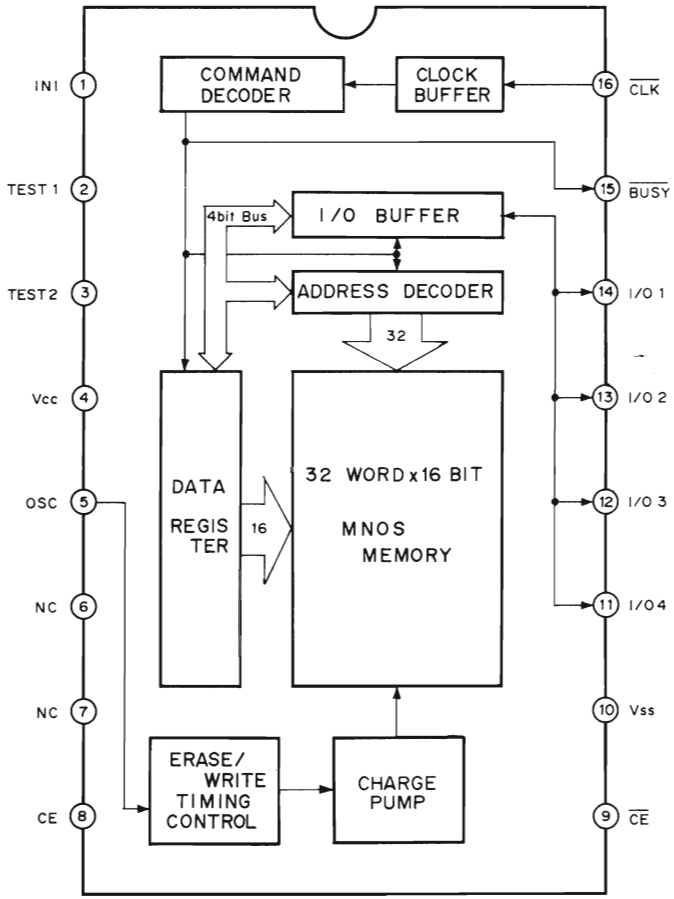
• Supply voltage	V_{CC}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3* to V_{CC}+0.3*	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

***Note)** This value is at normal condition; it may be 0.5V at the transient time (20 to 30 ms).

Recommended Operating Conditions (Ta=−20 to +75°C, Vss=0V)

• Supply voltage	V_{CC}	4.5 to 5.5	V
• Clock frequency	f_{CLK}	DC to 50	kHz
• High level input voltage	V_{INH}	V_{CC}−1.5 to V_{CC}	V
• Low level input voltage	V_{INL}	0 to V_{CC}−3.5	V
• High level input voltage (OSC pin)	V_{INH2}	V_{CC}−0.5 to V_{CC}	V
• Low level input voltage (OSC pin)	V_{INL2}	0 to 1.5	V

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	I/O	Symbol	Description
1	I	INI	Initialize input pin
2		TEST1	Test input pin (normally connected to V_{CC})
3		TEST2	Test input pin (normally connected to V_{CC})
4		V_{CC}	Power supply pin
5	I	OSC	Oscillation pin
6		NC	
7		NC	
8	I	CE	Chip enable input
9	I	$\overline{CE}$	Chip enable input
10		V_{SS}	Power supply pin
11	I/O	I/O4	Address and data I/O pin 4
12	I/O	I/O3	Address and data I/O pin 3
13	I/O	I/O2	Address and data I/O pin 2
14	I/O	I/O1	Address and data I/O pin 1
15	O	$\overline{BUSY}$	BUSY signal output pin
16	I	$\overline{CLK}$	Sync clock input pin

Electrical Characteristics 1

(T_a=−20 to +75°C, V_{CC}=5V ±10%, V_{SS}=0V)

Item	Symbol	Pin Name	Condition	Min.	Typ.	Max.	Unit
Supply current	I_{CC}	V_{CC}	*1		4	6	mA
Input pull-up current	I_{IU}	$\overline{CLK}$, CE, $\overline{CE}$		−45	−90	−180	μA
Input leakage current	I_{ILK}	All input pins				±20	μA
Output leakage current	I_{OLK}	All output pins				±20	μA
Output voltage high level 1	V_{OH1}	I/O1 to I/O4	I_{OH}=−0.5mA	V_{CC}−1.0			V
Output voltage low level 1	V_{OL1}	I/O1 to I/O4	I_{OL}=+0.5mA			+1.0	V
Output voltage high level 2	V_{OH2}	$\overline{BUSY}$	I_{OH}=−40μA	V_{CC}−1.0			V
Output voltage low level 2	V_{OL2}	$\overline{BUSY}$	I_{OL}=+40μA			+1.0	V
Input current 2 *2	I_{IN2}	OSC	V_{IN2}= V_{CC}−0.5V		1.0	1.5	mA

Note) *1 Includes the erasure and write times.
*2 t_{OSCH} See Timing Chart (3)

Electrical Characteristics 2

(T_a=−20 to +75°C, V_{CC}=5V ±10%, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	t_{WH}		10			μs
Clock pulse width	t_{WL}		10			μs
Data input setup time	t_{DS}		0			μs
Data input hold time	t_{DH}		0			μs
Rise/fall time	t_r, t_f				1	μs
Clock setup time	t_{CKS}		10			μs
Data delay time	t_{OD}				5	μs
Number of read	N_R	Refresh time	10^7	10^9		time
Write time	t_W	C=0.47μF, R=150 kΩ		30	60	ms
Erasure time	t_E	C=0.47μF, R=150 kΩ		30	60	ms
Memory retention time 1	t_{MH1}	After rewriting 10^4 times Store at Ta=85°C	10			year
Memory retention time 2	t_{MH2}	After rewriting 10^5 times Store at Ta=85°C	1			year

*__Note)__ It indicates the value during C=0.47 μF and R=150 kΩ, and for example, it become is tw (tz)=40 ms(typ.), 80 ms(max.) when during C=0.1 μF and R=82 kΩ (See Fig. 1).

Command Table

INI	CE	$\overline{CE}$	I/O1	I/O2	I/O3	I/O4	Operational command
L	H	L	L	L	H	L	DR: Memory read
L	H	L	H	L	H	L	DW: Memory write
L	H	L	X	X	L	L	No operation
L	H	L	X	X	L	H	No operation
L	H	L	X	X	H	H	No operation
L	L	L	X	X	X	X	No operation
L	L	H	X	X	X	X	No operation
L	H	H	X	X	X	X	No operation
H	X	X	X	X	X	X	No operation

Note) X denotes no relationship.

Description of Circuit Operations

Interactions between the memory and controller are performed by using two types of commands, the DR (Data Read) and DW (Data Write). The DW has two methods; namely, one method is to generate automatically by attaching CR to the OSC pin the erasure write-in time, and the other is by applying erasure write-in pulses to the OSC pin from the controller. Signals entered from the I/O bus are taken into the circuit at the fall time of $\overline{CLK}$, and the output signals from the memory are obtained at the rise time of the $\overline{CLK}$. The signals to be sent to the memory are switched while the $\overline{CLK}$ is in "H" level and they are fixed when the level is "L".

(1) DR: Data Read (Memory Read)

Entering the DR mode "L, L, H and L" from the I/O bus and entering the 5 bit address data at the next two clock cycles result in reading out the memory cell contents in the succeeding single clock cycle. Then, in the next four clock cycles, 16 bit data of D1 to D16 are output from the I/O bus, at every 4 bits time.

Now, a detailed description of the circuit operations will be given below.

- First the initialization is applied, then after 10 μs the first clock pulse is entered. The data read mode "L, L, H and L" which have been set to the I/O bus are taken into the circuit at the fall time of the first clock pulse. At the same time, the $\overline{BUSY}$ signal is output from the memory and goes into the BUSY state.
- At the fall time of the second clock and the third clock pulses, the address data "A0, A1, A2 A3" and "A4" are taken into the circuit, respectively.
- At the memory cell contents are read out internally at the fall time of the fourth clock pulse, the data "H, H, H and H" should be set to the I/O bus.
- At the rise time of the fourth clock pulse, the 4 bit data of "D1 to D4" are output to the I/O bus, in synchronization with the CLK. Likewise, at the rise time of the fifth clock pulse the data of "D5 to D8", at the rise time of the sixth clock pulse the data of "D9 to D12", and at the rise time of the seventh clock pulse the data of "D13 to D16" are output into I/O bus. That means a total of 16 bits are output during the four clock cycles.
- At the fall time of the ninth clock pulse, the data "H, H, H and H" are taken into the circuit, and the $\overline{BUSY}$ output is released.

Note) X denotes no relationship.

(2) DW1: Data Write 1 (Memory Write in OSC automatic transmission)

This paragraph describes when C-R (C=0.47 μF, R=150Ω typ.) is attached to the OSC pin.

Enter the DW mode "H, L, H and L" from the I/O bus and enter the 5 bit address data into the next two clock cycles. The data being written in after 1 clock is 4 bits, so with a total of 4 clocks 16 bits are input. In the after the data has set, the internal oscillation circuit automatically starts the operation and makes the clock timings of every 30 ms (typ.) for erasure and writing.

Whether the erasure/write operation has been completed can be datermined by observing the $\overline{BUSY}$ output signal.

A detailed description of the circuit operations for the data write will be given below.

- The initialization is applied first, and after 10 μs the first clock pulse is input. The data write mode "H, L, H and L" set in the I/O bus is taken into the circuit at the fall time of the first clock pulse. At the same time, the $\overline{BUSY}$ signal is output from the memory and memory becomes into the BUSY state.
- At the fall times of the second and third clock pulses, the address data "A0, A1, A2 A3" and "A4" are taken into the circuit, respectively.
- At the fall time of the fourth clock pulse, the data "H, H, H and H" are set in the I/O bus.
- At the fall time of the fifth clock pulse the data of "D1 to D4", at the fall time of the sixth clock pulse the data of "D5 to D8", at the fall time of the seventh clock pulse the data of "D9 to D12", and at the fall time of the eighth clock pulse the data "D13 to D16" are taken into the circuit, respectively, from the I/O bus, 4 bits at a time. The 16 bit data are set to the register within the circuit.
- At the rise time of the eighth clock pulse the OSC pin automatically starts oscillation. During the first oscillation cycle the erase operation and during the second oscillation cycle the write operation are automatically performed.

(3) DW2: Data Write 2 (Memory Write-in: Apply OSC external pulse)

Described hereafter is the case in which erasure write pulse is applied to the OSC pin from the controller.

Input DW mode "H, L, H, L" from I/O bus, enter address data 5 bits by the next 2 clocks, and, after 1 clock, input 16 bit write-in data (4 bit × 4 clock). Heretofore, it has been identical to "DW1". After the data has been set, enter erasure write in pulses (Respectively over 30 ms) to the OSC pin. Details of the operations are given below.

- As it is the same as "DW1" until data is set, the description is omitted.
- After the rising of No.8 clock, the low period t_E (30 ms), high period t_{OSCH} (5 to 50 μs), and low period tw (30 ms) pulses are input to the OSC pin. Operations of erase at the t_E time, write at the t_{OSCH} + tw time are carried out.
- "H, H, H, H" are fetched from the I/O bus at the falling of the No.9 clock, and reset is applied to the internal counter. When OSC pin is made high after the end of tw, the $\overline{BUSY}$ output is also released.

Notes on Application

(1) Power-on Reset Circuit

The power-on reset circuit is built-in the memory internal circuit. When the initialization is applied using the power-on reset circuit, the following items should be observed:

- The power supply should be smoothly raised and be noise free.
- The power supply rise time t_R should be $0.1 < t_R < 50$ (ms).
- At the power rise time, the input pin should not be lower than Vss and higher than Vcc.

(2) Initialization

When the power supply is turned on, the initialization should be applied externally whenever possible. In the normal operation when the memory is not being accessed, hold the initialization state so that erroneous changes of data by noises can be avoided.

When the initialization is applied, either the INI or $\overline{CE}$ is set to high, or the CE is set to low. Those pins perform the same function. Note that the initialization should not be made when the $\overline{BUSY}$ signal is being output (that is when the memory is in BUSY state). Otherwise, the access operation made immediately before is not guaranteed.

(3) Continuous Access

When the memory is continuously accessed, memory access should be started after 10 μs of the release of $\overline{BUSY}$ signal or release of the initialization by switching one of the signals of INI, $\overline{CE}$, CE, etc.

(4) Pull-up Resistor

Basically, the pull-up resistor is not necessary for the output pins (I/O1 to I/O4 and $\overline{BUSY}$). I/O1 to I/O4 are kept at high impedance in the input mode. Since $\overline{BUSY}$ outputs low during the memory operation and outputs high in the stand-by mode, it is recommended not to attach a pull-up resistor.

If the pull-up resistors are required for system stabilization, the following values should serve as a standard.

I/O1 to I/O4	Higher than 22 kΩ
$\overline{BUSY}$	Higher than 120 kΩ

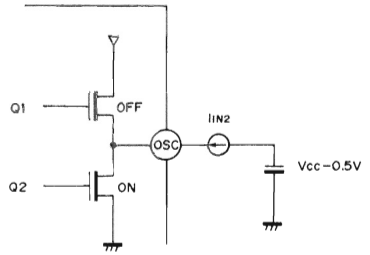
(5) E/W (Erase/Write) Oscillation

By attaching the CR externally to the OSC pin, the oscillation is automatically started from the rise time of the ninth clock pulse of the "DW" to generate the timings of the erasure and writing. The standard values of the CR are set as follows: C=0.47 μF and R=150 kΩ. At this time, the Erase/Write times become as follows: Erase=30 ms (typ.) and Write=30ms (typ.). When other constants are to be selected, determine the values in the recommended range by referring to Fig. 1. When it is out of the range, the memory retention time may not be guaranteed.

(6) Caution to be exercised when controlling the time of erasure and write-in from the exterior.

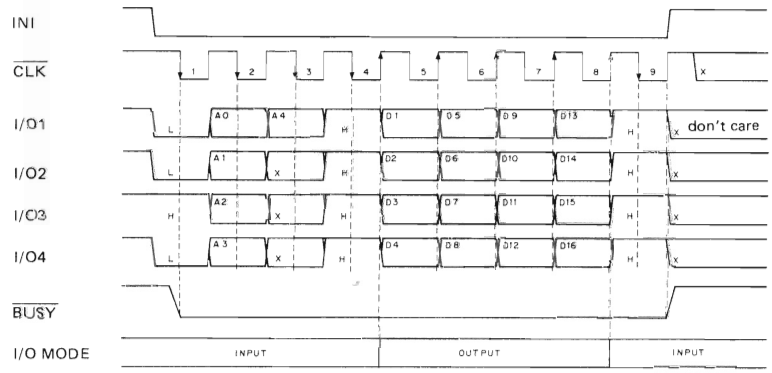
When it is considered to make the OSC pin over (V_{CC}—0.5V) during the t_{OSCH}, the Q2 in the figure below is turned ON and the current flows into the IC. Therefore the control IC must have the capability of the drive of over 1.5 mA.

Moreover, both Q1 and Q2, the OSC pin during the t_E and t_W is OFF and it is at high impedance. Except for Erase/Write, Q1 only is ON (Ron, typ. = 10 kΩ) and the OSC pin is pulled-up.

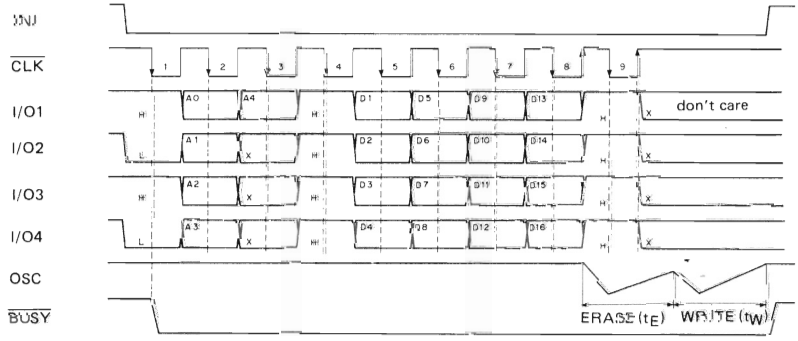


Timing Chart

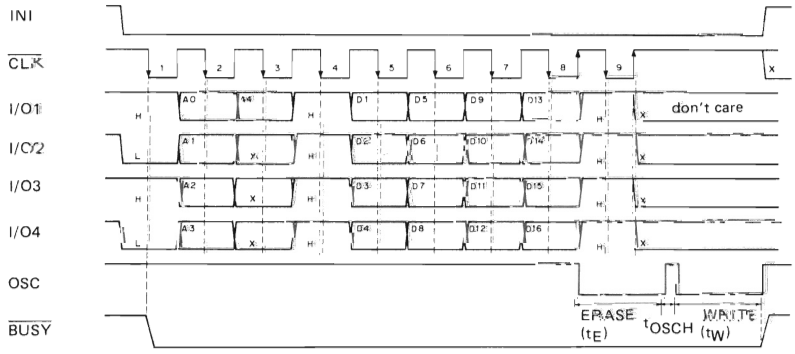
(1) DR: Data Read



(2) DW1: Data Write 1



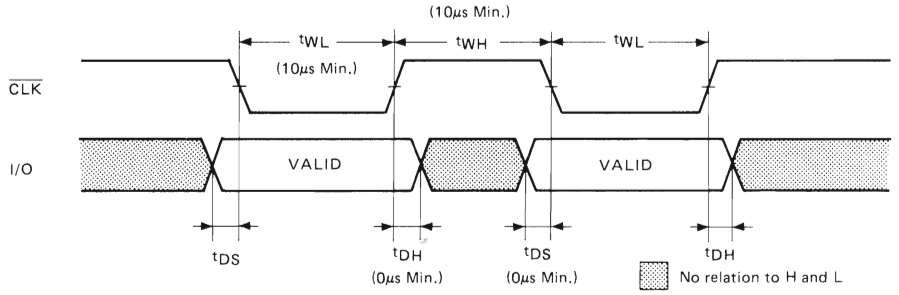
(3) DW2: Data Write 2



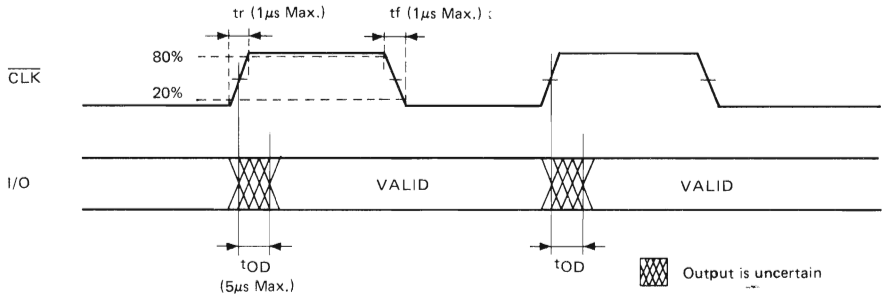
Item.	Min.	Max.
t_E	30msec	
t_W	30msec	
t_{OSCH}	5μsec	50μsec

I/O Timing Chart

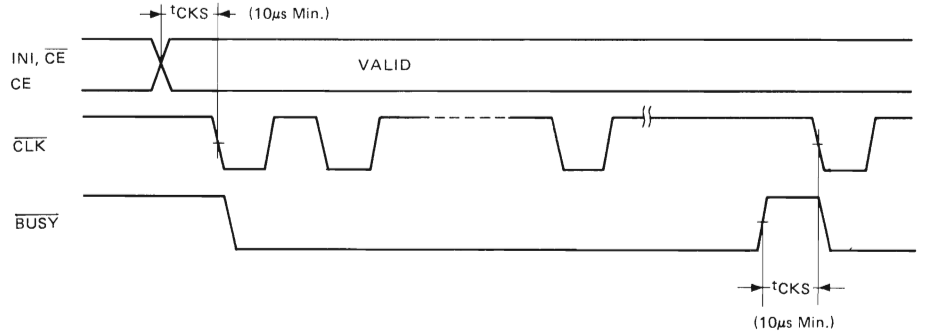
Input Mode



Output Mode



Access Mode



OSC Pin constant

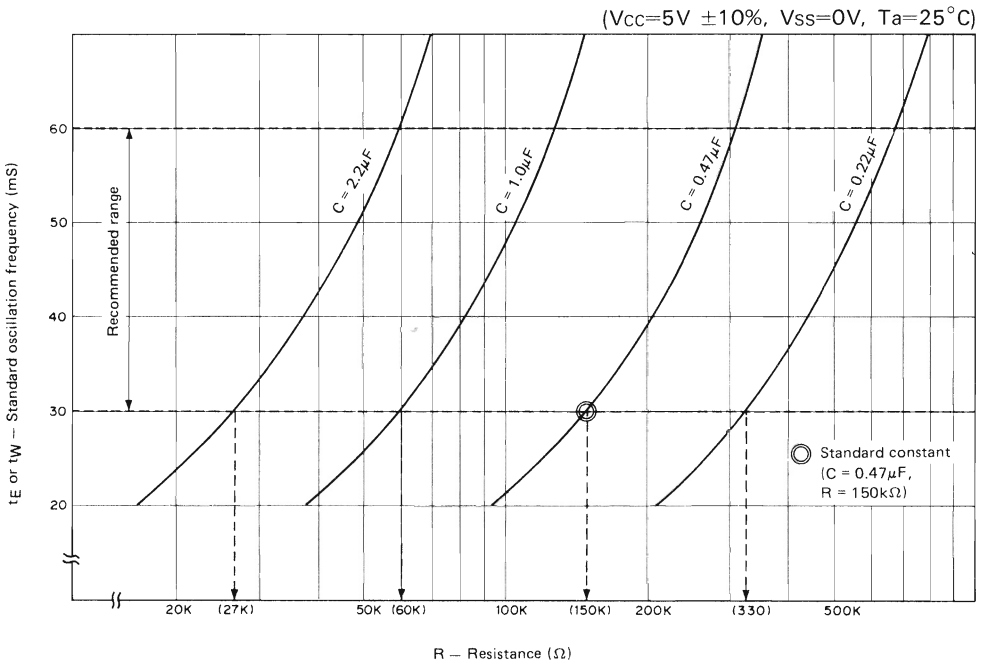
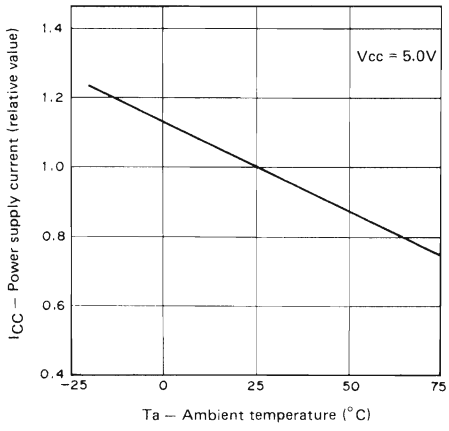
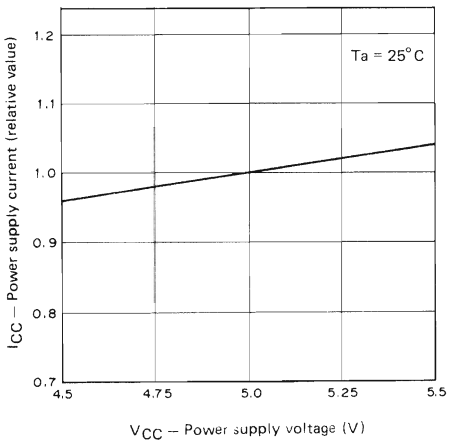


Fig. 1

Power supply current temperature characteristics

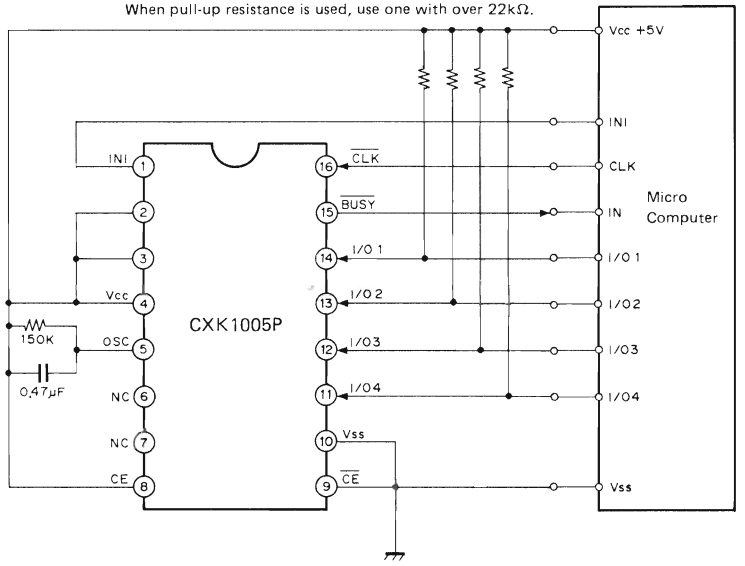


Power supply current vs. Power supply voltage characteristics

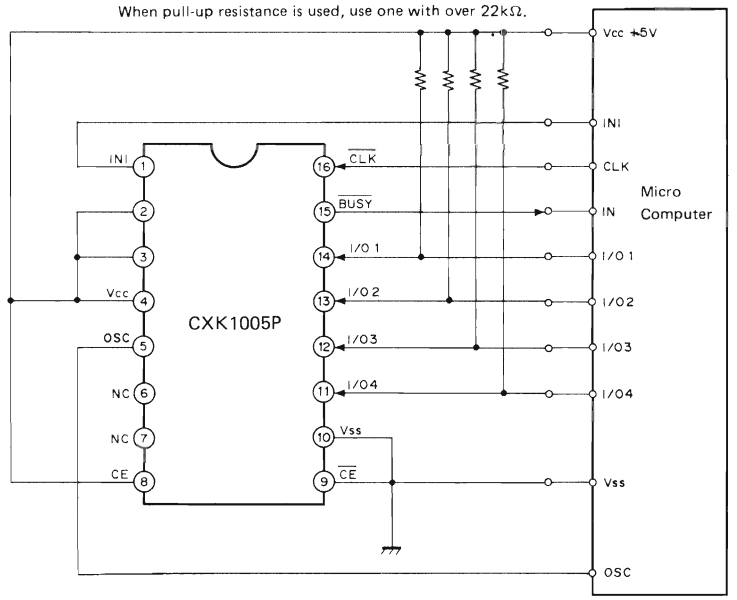


Application Circuit

1) When CR is oscillated



2) When controlled by exterior



1024-bit (64 word×16 bit) Non-Volatile Memory

Preliminary

Description

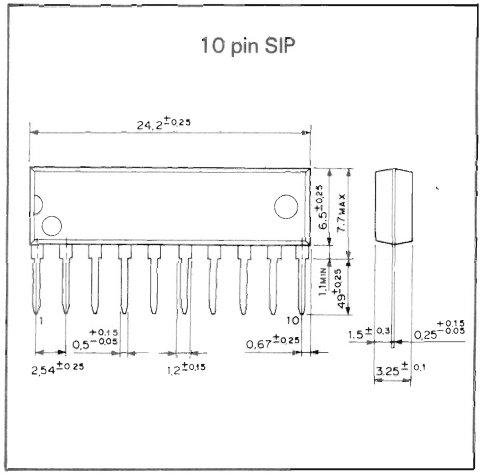
The CXK1006L is an electrically erasable and programmable 64 word × 16 bit E^2 PROM IC using MNOS non-volatile memory transistors.

The sequence controller is controlled with fewer program steps because it is incorporated in the IC and control signals for its operation are generated there.

The charge-pump circuit enables all operations to be executed with only a 5 V power supply. No high voltage is needed thereby enabling low-power consumption design (25 mW Typ.). The electronic tuner has a non-volatile channel memory and field making it ideal for a ROM system requiring several instant reloads.

Package Outline

Unit: mm



Features

- Single 5V power supply
- Full-decode 64 word × 16 bit structure
- Reloadable in one-word unit
- Memory holding more than 10 years with no power supply
- Erase and write more than 10^5 times
- Incorporated sequence controller
- Built-in timing circuit for write and erase
- 4-bit input/output control
- Low power consumption design (25 mW Typ.)

Structure

P-channel MNOS IC

Absolute Maximum Ratings (Ta = −20 to +75°C)

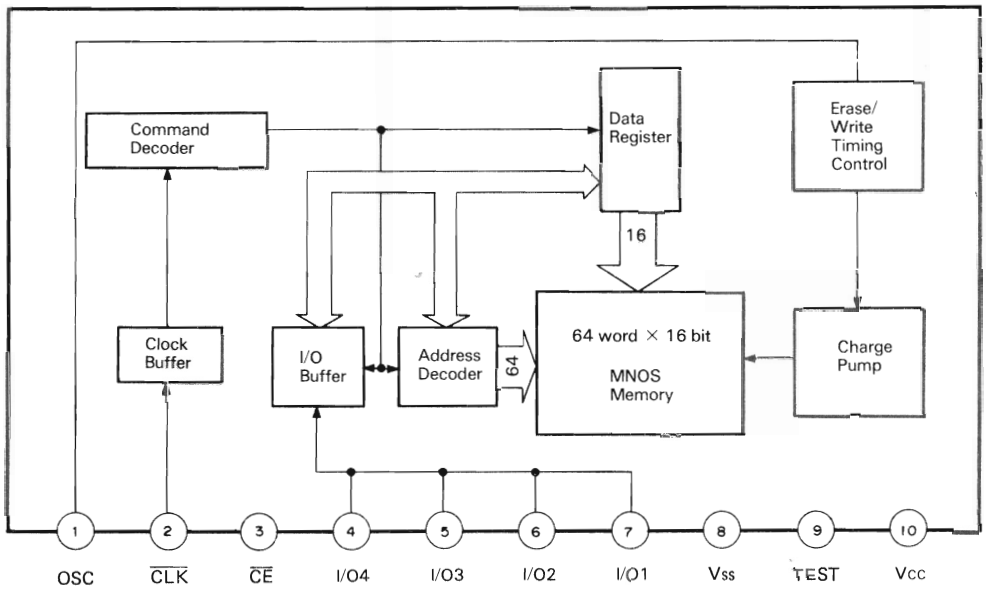
• Supply voltage	V_{CC}	−0.3 to 7.0	V
• Input voltage	V_{IN}	−0.3* to V_{CC} +0.3*	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

* Note) This value is for the steady state. In transit (20 to 30 ms), 0.5V is sufficient.

Recommended Operating Conditions (Ta = −20 to +75°C, Vss = 0V)

• Supply voltage	V_{CC}	4.5 to 5.5	V
• Clock frequency	f_{CLK}	DC to 50	kHz
• High-level input voltage	V_{INH1}	V_{CC} −1.5 to V_{CC}	V
• Low-level input voltage	V_{INL1}	0 to V_{CC} −3.5	V
High-level input voltage (OSC pin)	V_{INH2}	V_{CC} −0.5 to V_{CC}	V
Low-level input voltage (OSC pin)	V_{INL2}	0 to 1.5	V

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	I/O	Symbol	Description
1	I	OSC	Oscillation pin
2	I	$\overline{CLK}$	Sync clock input pin
3	I	$\overline{CE}$	Chip enable input
4	I/O	I/O4	Address and data input/output pin 4
5	I/O	I/O3	Address and data input/output pin 3
6	I/O	I/O2	Address and data input/output pin 2
7	I/O	I/O1	Address and data input/output pin 1
8		Vss	Power supply pin
9		TEST	Test input pin (Usually, connect to Vcc)
10		Vcc	Power supply pin

Electrical Characteristics 1

(Ta = −20 to +75°C, Vcc = 5.0V±10%, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{CC}	Vcc	*1		5	7	mA
Input pullup current	I_{IU}	$\overline{CLK}$, $\overline{CE}$		−45	−90	−180	μA
Input leakage current	I_{ILK}	All input pins				±20	μA
Output leakage current	I_{OLK}	All output pins				±20	μA
Output voltage "high-level" 1	V_{OH1}	I/O1 to I/O4	I_{OH} = −0.5mA	Vcc−1.0			V
Output voltage "low-level" 1	V_{OL1}	I/O1 to I/O4	I_{OL} = +0.5mA			1.0	V
Input current 2 *2	I_{IN2}	OSC	V_{IN2}=Vcc−0.5V		1.0	1.5	mA

Note) *1 Including during Erase and Write.
*2 Only tosch interval (See Timing Chart (3).)

Electrical Characteristics 2

(Ta = −20 to +75°C, Vcc = 5.0V±10%, Vss = 0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	t_{WH}		10			μs
Clock pulse width	t_{WL}		10			μs
Data input setup time	t_{DS}		0			μs
Data input hold time	t_{DH}		0			μs
Rise/Fall time	tr, tf				1	μs
Clock setup time	t_{CKS}		10			μs
Data delay time	t_{OD}				5	μs
Read time	N_R	During refresh	10^7	10^9		time
Write time	tw	C=0.47μF, R=150kΩ		30	60	ms
Erase time	t_E	C=0.47μF, R=150kΩ		30	60	ms
Memory hold time 1	t_{MH1}	Storing at Ta=85°C after reloads 10^4	10			year
Memory hold time 2	t_{MH2}	Storing at Ta=85°C after reloads 10^5	1			year

Instruction Length

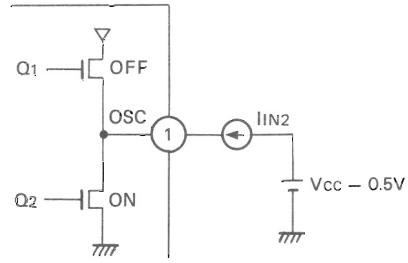
$\overline{CE}$	I/O1	I/O2	I/O3	I/O4	Operation instruction
L	L	L	H	L	DR: Memory read
L	H	L	H	L	DW: Memory write
L	X	X	L	L	No operation
L	X	X	L	H	No operation
L	X	X	H	H	No operation
H	X	X	X	X	No operation

Note) X denotes no relationship

Notes on Applications

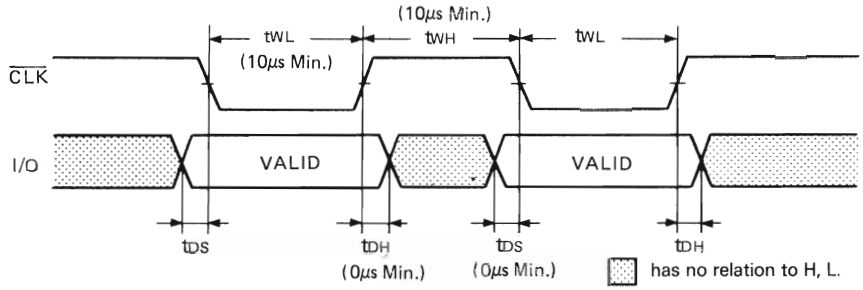
When the OSC pin is controlled externally without using the CR oscillation, Q_2 is switched on for the interval of t_{OSCH} and the current flows into IC. Therefore, IC control requires more than 1.5 mA of the drive capacity.

For t_E and tW intervals, both Q_1 and Q_2 are switched off and the OSC pin goes to high impedance. Except for Erase/Write, only Q_1 is switched on ($R_{ON,typ}$ = 10 kΩ), and the OSC pin is pulled up.

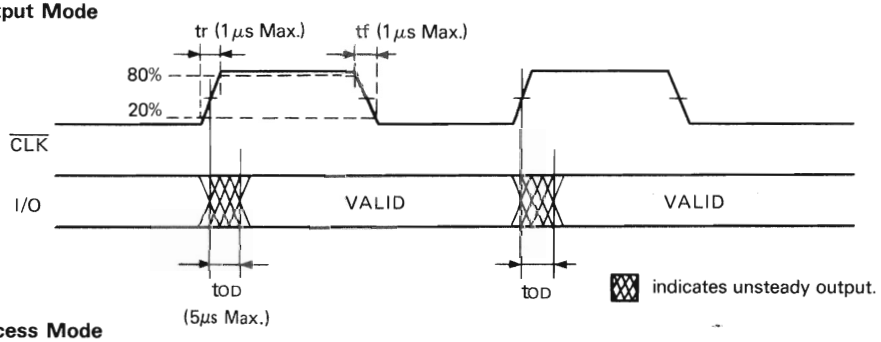


I/O Timing Chart

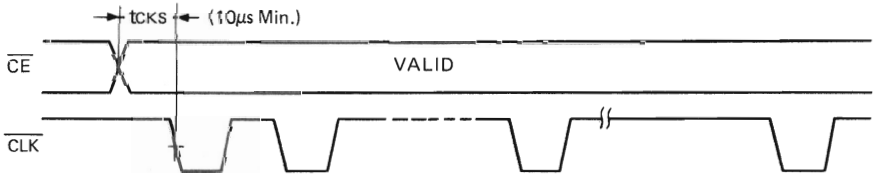
Input Mode



Output Mode

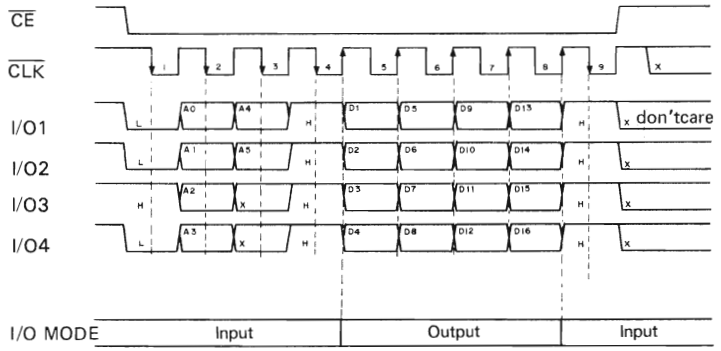


Access Mode

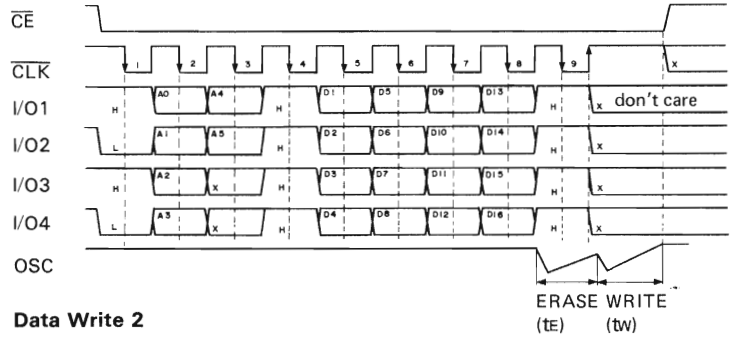


Timing Chart

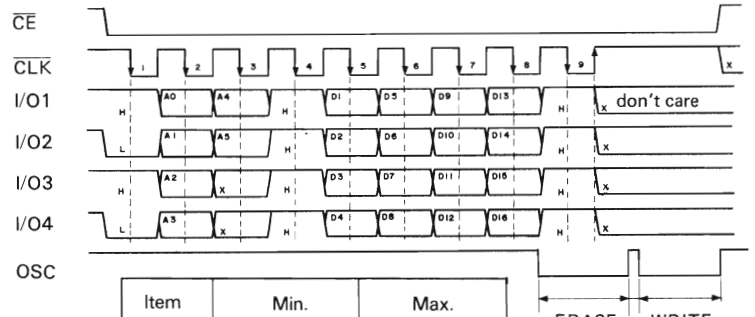
(1) DR: Data Read



(2) DW1: Data Write 1



(3) DW2: Data Write 2



Item	Min.	Max.
tE	30 msec	
tW	30 msec	
tOSCH	5 μsec	50 μsec

SONY

CXK1007P

1024-bit (64 word×16 bit) Non-Volatile Memory

Description

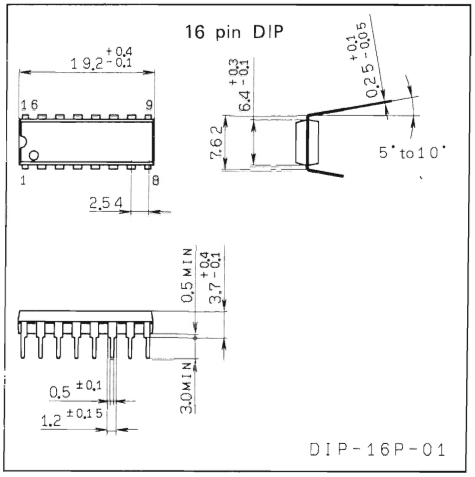
The CXK1007P is an electrically erasable and programmable E^2PROM of 64 word × 16 bit structure, employing the non-volatile memory transistors of the MNOS type.

As the sequence controller is built-in the IC and the control signals necessary for operations are generated within the IC, the chip can be controlled with fewer program steps.

The IC built-in a charge pump circuit and all the operations can be performed with only the 5V power supply. It requires no high voltage, and it is so designed as to require low power consumption (25 mW Typ.). It has a non-volatile channel memory for the electronic tuner and a most suitable read-only memory system that can be rewritten immediately any time when necessary in the field.

Package Outline

Unit: mm



Features

- Single 5V power supply
- 64 word × 16 bit structure of full decoding
- Rewritable in 1-word unit
- Memory retention time of more than 10 years with no power supply
- Number of erasures and writings of more than 10^5 times
- Built-in sequence controller
- Built-in timing circuit for erasure of writing
- 4-bit I/O control
- Low power consumption design (25 mW Typ.)

Structure

P-channel MNOS IC

Absolute Maximum Ratings (Ta=25°C)

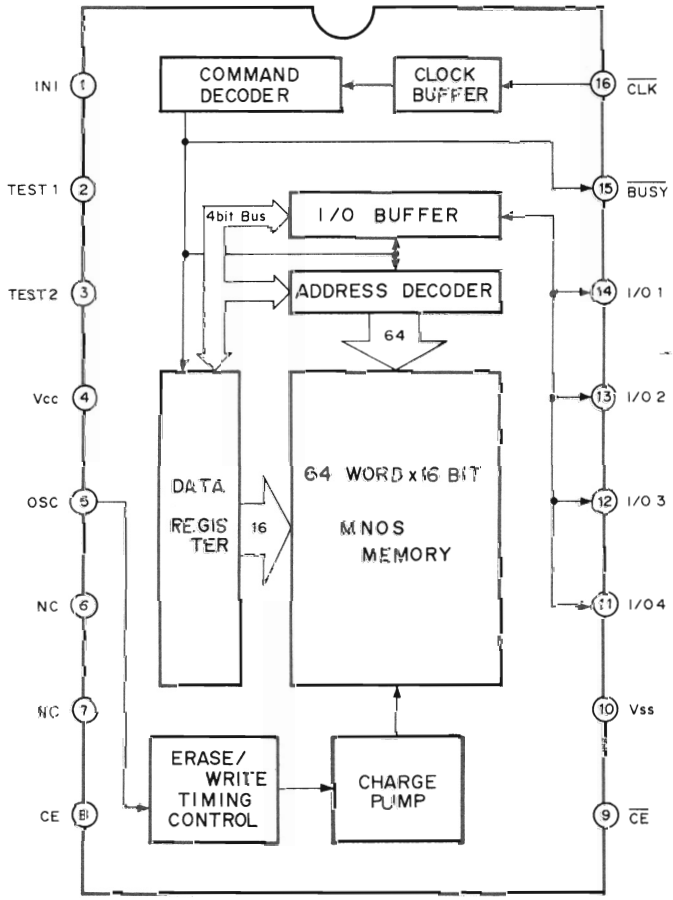
• Supply voltage	V_{CC}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3* to V_{CC}+0.3*	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

***Note)** This value is at normal condition; it may be 0.5V at the transient time (20 to 30 ms).

Recommended Operating Conditions (Ta=−20 to +75°C, Vss=0V)

• Supply voltage	V_{CC}	4.5 to 5.5	V
• Clock frequency	f_{CLK}	DC to 50	kHz
• High level input voltage	V_{INH}	V_{CC}−1.5 to V_{CC}	V
• Low level input voltage	V_{INL}	0 to V_{CC}−3.5	V
• High level input voltage (OSC pin)	V_{INH2}	V_{CC}−0.5 to V_{CC}	V
• Low level input voltage (OSC pin)	V_{INL2}	0 to 1.5	V

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	I/O	Symbol	Description
1	I	INI	Initialize input pin
2		TEST1	Test input pin (normally connected to Vcc)
3		TEST2	Test input pin (normally connected to Vcc)
4		Vcc	Power supply pin
5	I	OSC	Oscillation pin
6		NC	
7		NC	
8	I	CE	Chip enable input
9	I	$\overline{CE}$	Chip enable input
10		Vss	Power supply pin
11	I/O	I/O4	Address and data I/O pin 4
12	I/O	I/O3	Address and data I/O pin 3
13	I/O	I/O2	Address and data I/O pin 2
14	I/O	I/O1	Address and data I/O pin 1
15	O	$\overline{BUSY}$	BUSY signal output pin
16	I	$\overline{CLK}$	Sync clock input pin

Electrical Characteristics 1.

(Ta=−20 to +75°C, Vcc=5V ±10%, Vss=0V)

Item	Symbol	Pin Name	Condition	Min.	Typ.	Max.	Unit
Power supply current	Icc	Vcc	*1		5	7	mA
Input pull-up current	IIU	$\overline{CLK}$, CE, $\overline{CE}$		−45	−90	−180	μA
Input leakage current	IILK	All input pins				±20	μA
Output leakage current	IOLK	All output pins				±20	μA
Output voltage high level 1	VOH1	I/O1 to I/O4	IOH=−0.5mA	Vcc−1.0			V
Output voltage low level 1	VOL1	I/O1 to I/O4	IOL=+0.5mA			+1.0	V
Output voltage high level 2	VOH2	$\overline{BUSY}$	IOH=−40μA	Vcc−1.0			V
Output voltage low level 2	VOL2	$\overline{BUSY}$	IOL=+40μA			+1.0	V
Input current 2 *2	IIN2	OSC	VIN2= Vcc−0.5V		1.0	1.5	mA

Note) *1 Includes the erasure and write times.
*2 tOSCH See Timing Chart (3)

Electrical Characteristics 2.

(Ta=−20 to +75°C, V_{CC}=5V ±10%, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	t_{WH}		10			μs
Clock pulse width	t_{WL}		10			μs
Data input setup time	t_{DS}		0			μs
Data input hold time	t_{DH}		0			μs
Rise/fall time	t_r, t_f				1	μs
Clock setup time	t_{CKS}		10			μs
Data delay time	t_{OD}				5	μs
Number of read	N_R	Refresh time	10^7	10^9		time
Write time	t_W	C=0.47μF, R=150kΩ*		30	60	ms
Erasure time	t_E	C=0.47μF, R=150kΩ*		30	60	ms
Memory retention time 1	t_{MH1}	After rewriting 10^4 times Store at Ta=85°C	10			year
Memory retention time 2	t_{MH2}	After rewriting 10^5 times Store at Ta=85°C	1			year

***Note)** It indicates the value during C=0.47 μF and R=150 kΩ, and for example, it becomes tw (t_Z)=40 ms(typ.), 80 ms(max.) when during C=0.1 μF and R=82 kΩ (See Fig. 1).

Command Table

INI	CE	$\overline{CE}$	I/O1	I/O2	I/O3	I/O4	Operational command
L	H	L	L	L	H	L	DR: Memory read
L	H	L	H	L	H	L	DW: Memory write
L	H	L	X	X	L	L	No operation
L	H	L	X	X	L	H	No operation
L	H	L	X	X	H	H	No operation
L	L	L	X	X	X	X	No operation
L	L	H	X	X	X	X	No operation
L	H	H	X	X	X	X	No operation
H	X	X	X	X	X	X	No operation

Note) X denotes no relationship.

Description of Circuit Operations

Interactions between the memory and controller are performed by using two types of commands, the DR (Data Read) and DW (Data Write). The DW has two methods; namely, one method is to generate automatically by attaching CR to the OSC pin the erasure write-in time, and the other is by applying erasure write-in pulses to the OSC pin from the controller. Signals entered from the I/O bus are taken into the circuit at the fall time of $\overline{CLK}$, and the output signals from the memory are obtained at the rise time of the $\overline{CLK}$. The signals to be sent to the memory are switched while the $\overline{CLK}$ is in "H" level and they are fixed when the level is "L".

(1) DR: Data Read (Memory Read)

Entering the DR mode "L, L, H and L" from the I/O bus and entering the 6 bit address data at the next two clock cycles result in reading out the memory cell contents in the succeeding single clock cycle. Then, in the next four clock cycles, 16 bit data of D1 to D16 are output from the I/O bus, at every 4 bits time.

Now, a detailed description of the circuit operations will be given below.

- First the initialization is applied, then after 10 μs the first clock pulse is entered. The data read mode "L, L, H and L" which have been set to the I/O bus are taken into the circuit at the fall time of the first clock pulse. At the same time, the $\overline{BUSY}$ signal is output from the memory and goes into the BUSY state.
- At the fall time of the second clock and the third clock pulses, the address data "A0, A1, A2 A3" and "A4, A5" are taken into the circuit, respectively.
- At the memory cell contents are read out internally at the fall time of the fourth clock pulse, the data "H, H, H and H" should be set to the I/O bus.
- At the rise time of the fourth clock pulse, the 4 bit data of "D1 to D4" are output to the I/O bus, in synchronization with the CLK. Likewise, at the rise time of the fifth clock pulse the data of "D5 to D8", at the rise time of the sixth clock pulse the data of "D9 to D12", and at the rise time of the seventh clock pulse the data of "D13 to D16" are output into I/O bus. That means a total of 16 bits are output during the four clock cycles.
- At the fall time of the ninth clock pulse, the data "H, H, H and H" are taken into the circuit, and the $\overline{BUSY}$ output is released.

Note) X denotes no relationship.

(2) DW1: Data Write 1 (Memory Write in OSC automatic transmission)

This paragraph describes when C-R (C=0.47 μF, R=150Ω typ.) is attached to the OSC pin.

Enter the DW mode "H, L, H and L" from the I/O bus and enter the 6 bit address data into the next two clock cycles. The data being written in after 1 clock is 4 bits, so with a total of 4 clocks 16 bits are input. In the after the data has set, the internal oscillation circuit automatically starts the operation and makes the clock timings of every 30 ms (typ.) for erasure and writing.

Whether the erasure/write operation has been completed can be determined by observing the $\overline{BUSY}$ output signal.

A detailed description of the circuit operations for the data write will be given below.

- The initialization is applied first, and after 10 μs the first clock pulse is input. The data write mode "H, L, H and L" set in the I/O bus is taken into the circuit at the fall time of the first clock pulse. At the same time, the $\overline{BUSY}$ signal is output from the memory and memory becomes into the BUSY state.
- At the fall times of the second and third clock pulses, the address data "A0, A1, A2, A3" and "A4, A5" are taken into the circuit, respectively.
- At the fall time of the fourth clock pulse, the data "H, H, H and H" are set in the I/O bus.
- At the fall time of the fifth clock pulse the data of "D1 to D4", at the fall time of the sixth clock pulse the data of "D5 to D8", at the fall time of the seventh clock pulse the data of "D9 to D12", and at the fall time of the eighth clock pulse the data "D13 to D16" are taken into the circuit, respectively, from the I/O bus, 4 bits at a time. The 16 bit data are set to the register within the circuit.
- At the rise time of the eighth clock pulse the OSC pin automatically starts oscillation. During the first oscillation cycle the erase operation and during the second oscillation cycle the write operation are automatically performed.

(3) DW2: Data Write 2 (Memory Write-in: Apply OSC external pulse)

Described hereafter is the case in which erasure write pulse is applied to the OSC pin from the controller.

Input DW mode "H, L, H, L" from I/O bus, enter address data 6 bits by the next 2 clocks, and, after 1 clock, input 16 bit write-in data (4 bit × 4 clock). Heretofore, it has been identical to "DW1". After the data has been set, enter erasure write in pulses (Respectively over 30 ms) to the OSC pin. Details of the operations are given below.

- As it is the same as "DW1" until data is set, the description is omitted.
- After the rising of No.8 clock, the low period t_E (30 ms), high period t_{OSCH} (5 to 50 μs), and low period tw (30 ms) pulses are input to the OSC pin. Operations of erase at the t_E time, write at the t_{OSCH} + tw time are carried out.
- "H, H, H, H" are fetched from the I/O bus at the falling of the No.9 clock, and reset is applied to the internal counter. When OSC pin is made high after the end of tw, the $\overline{BUSY}$ output is also released.

Notes on Application

(1) Power-On Reset Circuit

The power-on reset circuit is built-in the memory internal circuit. When the initialization is applied using the power-on reset circuit, the following items should be observed:

- The power supply should be smoothly raised and be noise free.
- The power supply rise time t_R should be $0.1 < t_R < 50$ (ms).
- At the power rise time, the input pin should not be lower than Vss and higher than Vcc.

(2) Initialization

When the power supply is turned on, the initialization should be applied externally whenever possible. In the normal operation when the memory is not being accessed, hold the initialization state so that erroneous changes of data by noises can be avoided.

When the initialization is applied, either the INI or $\overline{CE}$ is set to high, or the CE is set to low. Those pins perform the same function. Note that the initialization should not be made when the $\overline{BUSY}$ signal is being output (that is when the memory is in BUSY state). Otherwise, the access operation made immediately before is not guaranteed.

(3) Continuous Access

When the memory is continuously accessed, memory access should be started after 10 μs of the release of $\overline{BUSY}$ signal or release of the initialization by switching one of the signals of INI, $\overline{CE}$, CE, etc.

(4) Pull-up Resistor

Basically, the pull-up resistor is not necessary for the output pins (I/O1 to I/O4 and $\overline{BUSY}$). I/O1 to I/O4 are kept at high impedance in the input mode. Since $\overline{BUSY}$ outputs low during the memory operation and outputs high in the stand-by mode, it is recommended not to attach a pull-up resistor.

If the pull-up resistors are required for system stabilization, the following values should serve as a standard.

I/O1 to I/O4	Higher than 22 kΩ
$\overline{BUSY}$	Higher than 120 kΩ

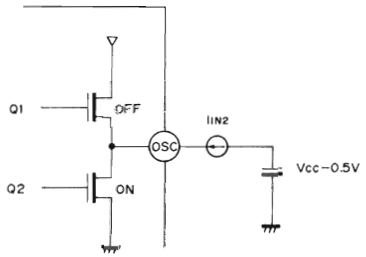
(5) E/W (Erase/Write) Oscillation

By attaching the CR externally to the OSC pin, the oscillation is automatically started from the rise time of the ninth clock pulse of the "DW" to generate the timings of the erasure and writing. The standard values of the CR are set as follows: C=0.47 μF and R=150 kΩ. At this time, the Erase/Write times become as follows: Erase=30 ms (typ.) and Write=30ms (typ.). When other constants are to be selected, determine the values in the recommended range by referring to Fig. 1. When it is out of the range, the memory retention time may not be guaranteed.

(6) Caution to be exercised when controlling the time of erasure and write-in from the exterior.

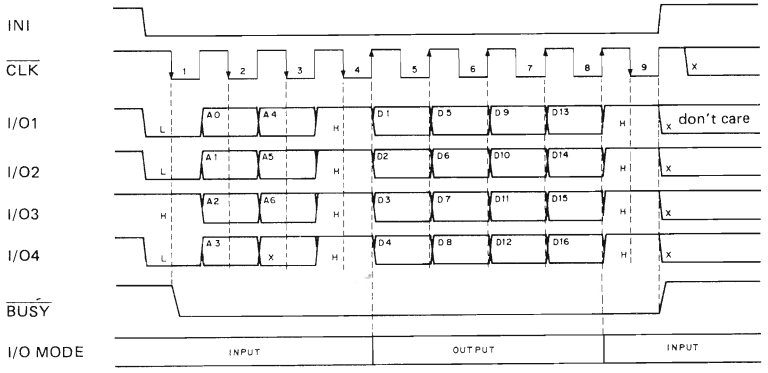
When it is considered to make the OSC pin over (V_{CC}—0.5V) during the t_{OSCH}, the Q2 in the figure below is turned ON and the current flows into the IC. Therefore the control IC must have the capability of the drive of over 1.5 mA.

Moreover, both Q1 and Q2, the OSC pin during the t_E and t_W is OFF and it is at high impedance. Except for Erase/Write, Q1 only is ON (Ron typ. = 10 kΩ) and the OSC pin is pulled-up.

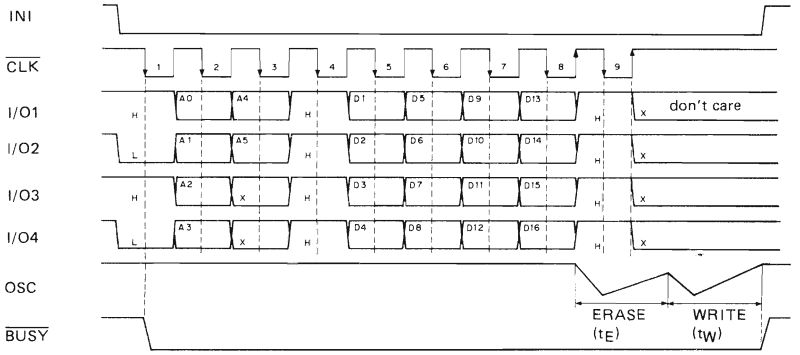


Timing Chart

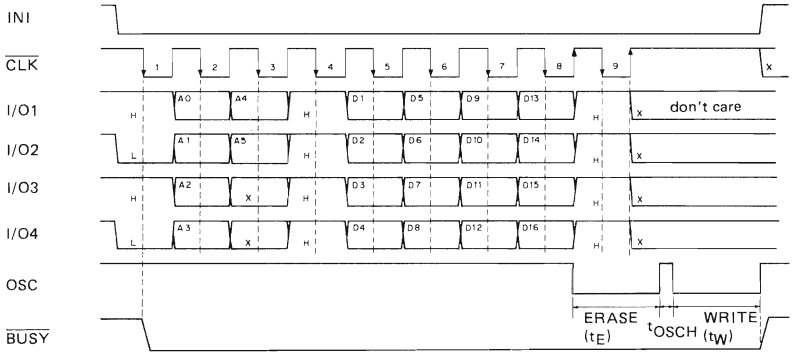
(1) DR: Data Read



(2) DW1: Data Write 1



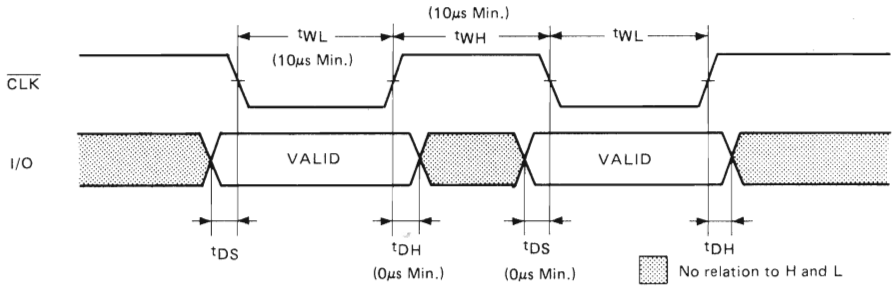
(3) DW2: Data Write 2



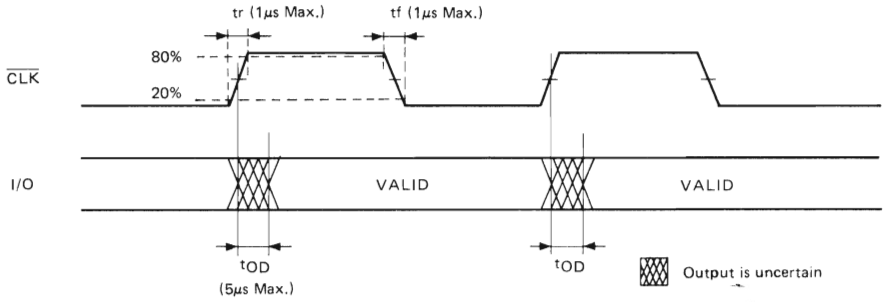
Item.	Min.	Max.
t_E	30msec	
t_W	30msec	
t_{OSCH}	5μsec	50μsec

I/O Timing Chart

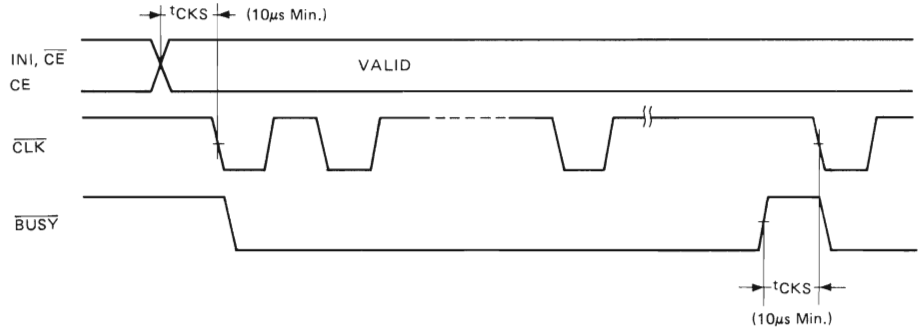
Input Mode



Output Mode



Access Mode



OSC Pin constant

(V_{CC}=5V ±10%, V_{SS}=0V, Ta=25°C)

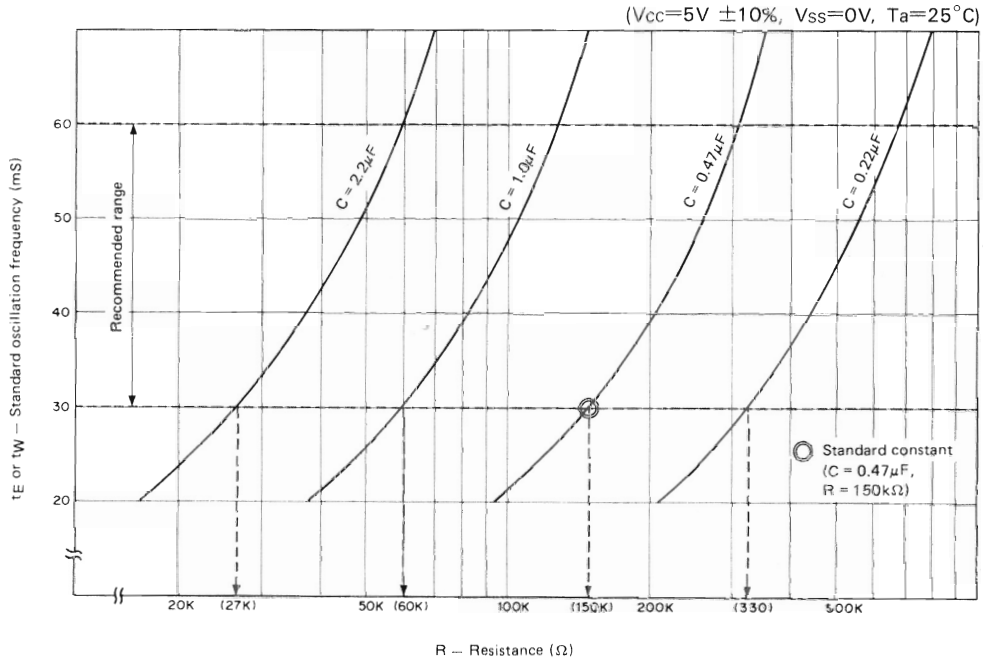
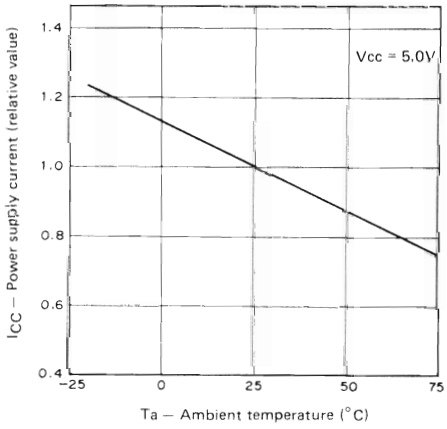
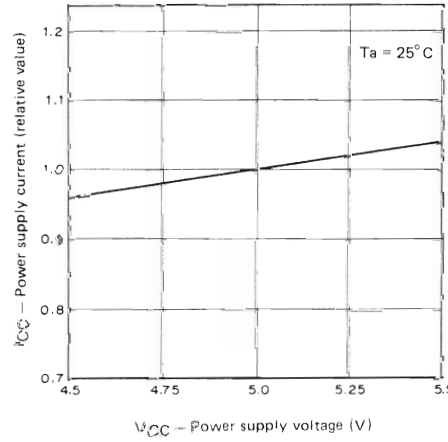


Fig. 1

Power supply current temperature characteristics

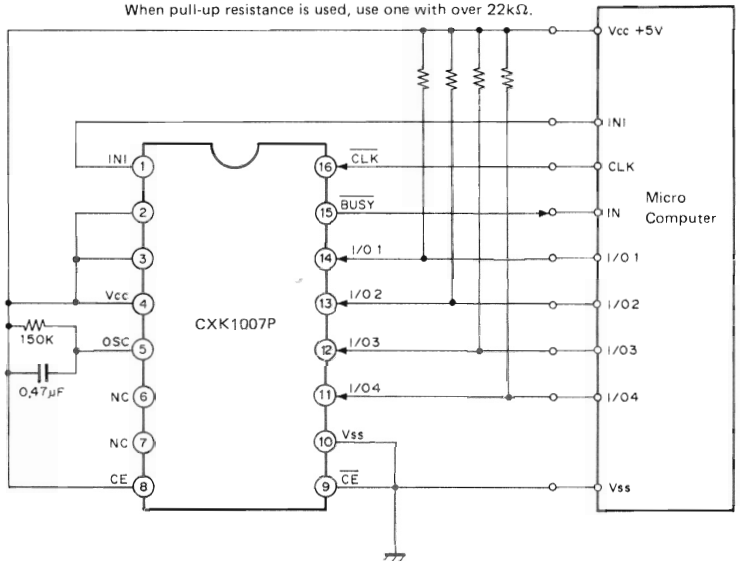


Power supply current vs. Power supply voltage characteristics

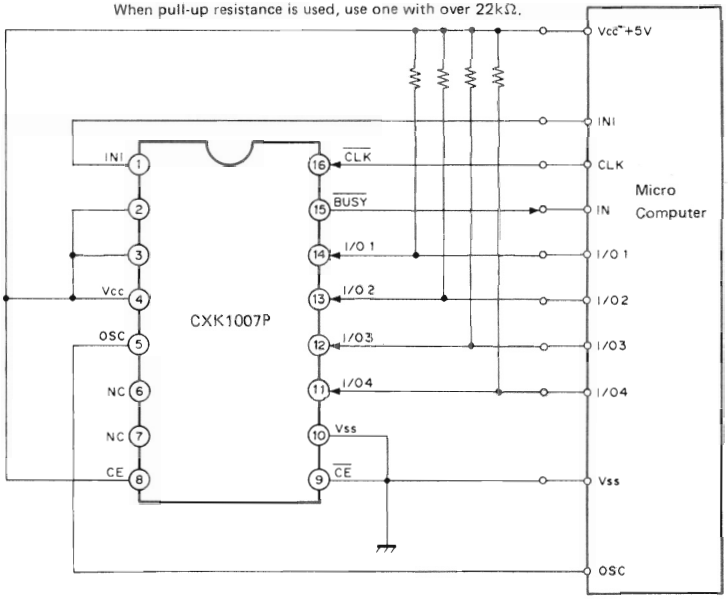


Application Circuits

1) When CR is oscillated



2) When controlled by exterior



2048-bit (128 word×16 bit) Non-Volatile Memory

Preliminary

Description

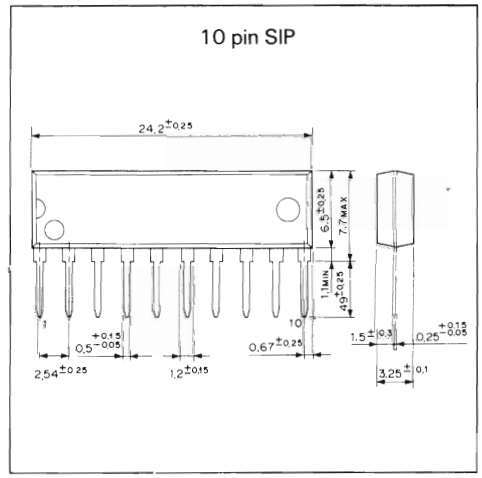
The CXK1008L is an electrically erasable and programmable 128 word×16 bit E^2 PROM IC using MNOS non-volatile memory transistors.

The sequence controller is controlled with fewer program steps because it is incorporated in the IC and control signals for its operation are generated there.

The charge-pump circuit enables all operations to be executed with only a 5 V power supply. No high voltage is needed thereby enabling low-power consumption design (30 mW Typ.). The electronic tuner has a non-volatile channel memory and field making it ideal for a ROM system requiring several instant reloads.

Package Outline

Unit: mm



Features

- Single 5V power supply
- Full-decode 128 word × 16 bit structure
- Reloadable in one-word unit
- Memory holding more than 10 years with no power supply
- Erase and write more than 10^5 times
- Incorporated sequence controller
- Built-in timing circuit for write and erase
- 4-bit input/output control
- Low power consumption design (30 mW Typ.)

Structure

P-channel MNOS IC

Absolute Maximum Ratings (Ta = −20 to +75°C)

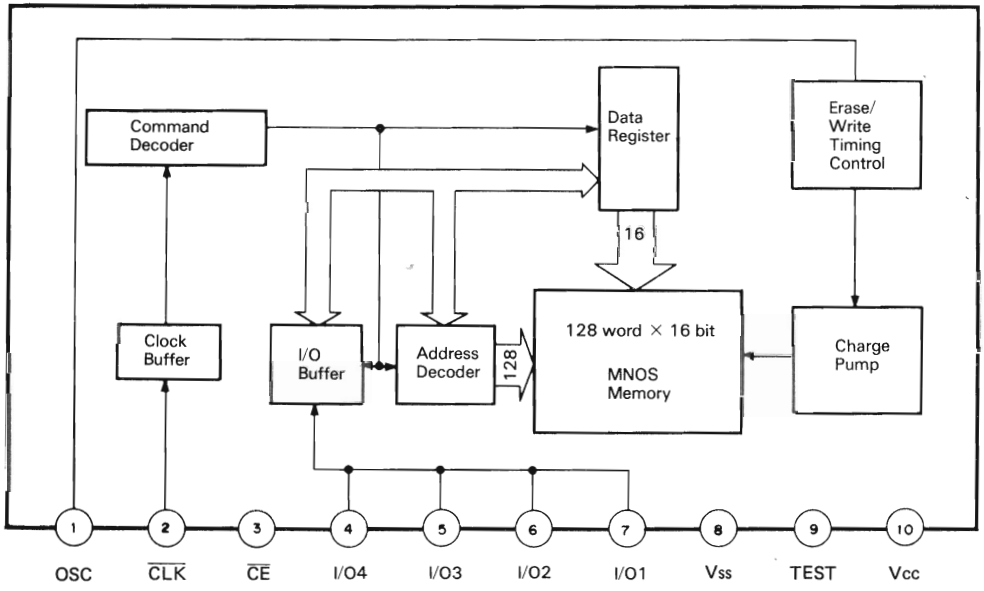
• Supply voltage	V_{CC}	−0.3 to 7.0	V
• Input voltage	V_{IN}	−0.3* to V_{CC} +0.3*	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

* Note) This value is for the steady state. In transit (20 to 30 ms), 0.5V is sufficient.

Recommended Operating Conditions (Ta = −20 to +75°C, Vss = 0V)

• Supply voltage	V_{CC}	4.5 to 5.5	V
• Clock frequency	f_{CLK}	DC to 50	kHz
• High-level input voltage	V_{INH1}	V_{CC} − 1.5 to V_{CC}	V
• Low-level input voltage	V_{INL1}	0 to V_{CC} − 3.5	V
High-level input voltage (OSC pin)	V_{INH2}	V_{CC} − 0.5 to V_{CC}	V
Low-level input voltage (OSC pin)	V_{INL2}	0 to 1.5	V

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	I/O	Symbol	Description
1	I	OSC	Oscillation pin
2	I	$\overline{CLK}$	Sync clock input pin
3	I	$\overline{CE}$	Chip enable input
4	I/O	I/O4	Address and data input/output pin 4
5	I/O	I/O3	Address and data input/output pin 3
6	I/O	I/O2	Address and data input/output pin 2
7	I/O	I/O1	Address and data input/output pin 1
8		Vss	Power supply pin
9		TEST	Test input pin (Usually, connect to Vcc)
10		Vcc	Power supply pin

Electrical Characteristics 1

(Ta = −20 to +75°C, Vcc = 5.0V±10%, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{CC}	Vcc	*1		6	9	mA
Input pullup current	I_{IU}	$\overline{CLK}$, $\overline{CE}$		−45	−90	−180	μA
Input leakage current	I_{ILK}	All input pins				±20	μA
Output leakage current	I_{OLK}	All output pins				±20	μA
Output voltage "high-level" 1	V_{OH1}	I/O1 to I/O4	I_{OH} = −0.5mA	Vcc−1.0			V
Output voltage "low-level" 1	V_{OL1}	I/O1 to I/O4	I_{OL} = +0.5mA			1.0	V
Input current 2 *2	I_{IN2}	OSC	V_{IN2}=Vcc−0.5V		1.0	1.5	mA

Note) *1 Including during Erase and Write.

*2 Only tosch interval (See Timing Chart (3).)

Electrical Characteristics 2

(Ta = −20 to +75°C, Vcc = 5.0V±10%, Vss = 0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	t_{WH}		10			μs
Clock pulse width	t_{WL}		10			μs
Data input setup time	t_{DS}		0			μs
Data input hold time	t_{DH}		0			μs
Rise/Fall time	tr, tf				1	μs
Clock setup time	t_{CKS}		10			μs
Data delay time	t_{OD}				5	μs
Read time	N_R	During refresh	10^7	10^9		time
Write time	t_W	C=0.47μF, R=150kΩ		30	60	ms
Erase time	t_E	C=0.47μF, R=150kΩ		30	60	ms
Memory hold time 1	t_{MH1}	Storing at Ta=85°C after reloads 10^4	10			year
Memory hold time 2	t_{MH2}	Storing at Ta=85°C after reloads 10^5	1			year

Instruction Length

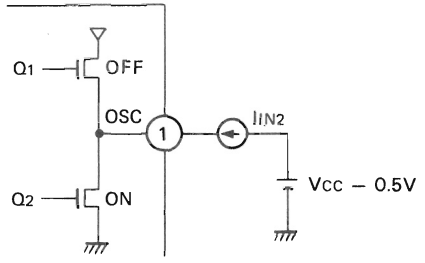
$\overline{CE}$	I/01	I/02	I/03	I/04	Operation instruction
L	L	L	H	L	DR: Memory read
L	H	L	H	L	DW: Memory write
L	X	X	L	L	No operation
L	X	X	L	H	No operation
L	X	X	H	H	No operation
H	X	X	X	X	No operation

Note) X denotes no relationship

Notes on Applications

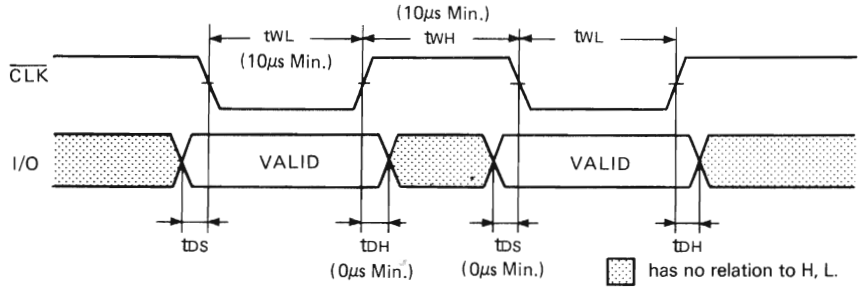
When the OSC pin is controlled externally without using the CR oscillation, Q_2 is switched on for the interval of t_{OSCH} and the current flows into IC. Therefore, IC control requires more than 1.5 mA of the drive capacity.

For t_E and t_W intervals, both Q_1 and Q_2 are switched off and the OSC pin goes to high impedance. Except for Erase/Write, only Q_1 is switched on ($R_{ON,typ}$ = 10 kΩ), and the OSC pin is pulled up.

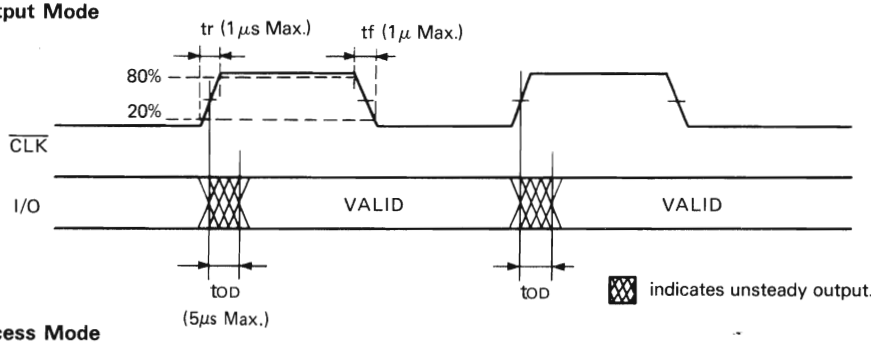


I/O Timing Chart

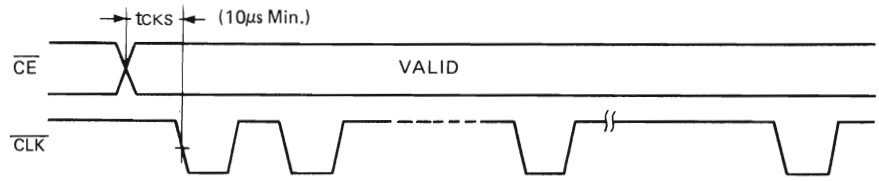
Input Mode



Output Mode

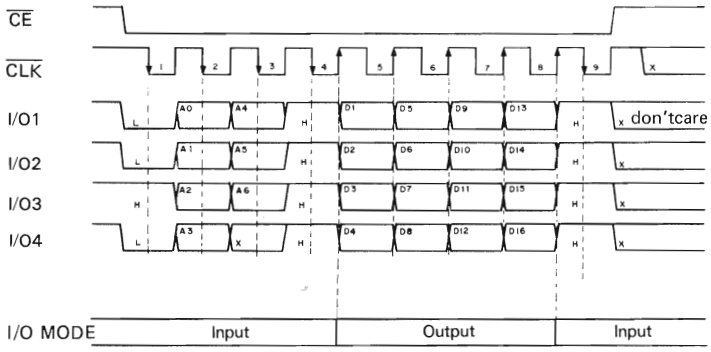


Access Mode

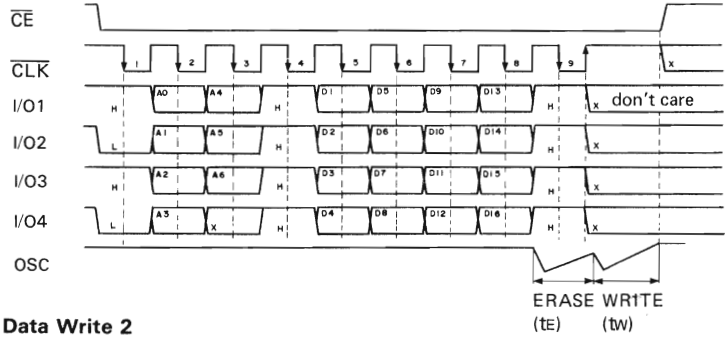


Timing Chart

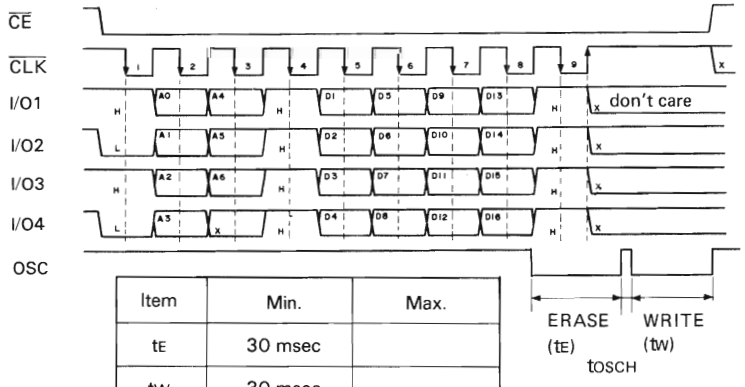
(1) DR: Data Read



(2) DW1: Data Write 1



(3) DW2: Data Write 2



Item	Min.	Max.
tE	30 msec	
tW	30 msec	
tOSCH	5 μsec	50 μsec

SONY

CXK1009P

2048-bit (128 word×16 bit) Non-Volatile Memory

Description

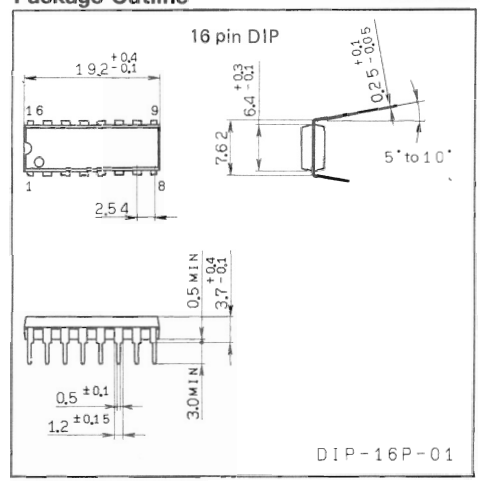
The CXK1009P is an electrically erasable and programmable E^2PROM of 128 word × 16 bit structure, employing the non-volatile memory transistors of the MNOS type.

As the sequence controller is built-in the IC and the control signals necessary for operations are generated within the IC, the chip can be controlled with fewer program steps.

The IC built-in a charge pump circuit and all the operations can be performed with only the 5V power supply. It requires no high voltage, and it is so designed as to require low power consumption (30 mW Typ.). It has a non-volatile channel memory for the electronic tuner and a most suitable read-only memory system that can be rewritten immediately any time when necessary in the field.

Package Outline

Unit: mm



Features

- Single 5V power supply
- 128 word × 16 bit structure of full decoding
- Rewritable in 1-word unit
- Memory retention time of more than 10 years with no power supply
- Number of erasures and writings of more than 10^5 times
- Built-in sequence controller
- Built-in timing circuit for erasure of writing
- 4-bit I/O control
- Low power consumption design (30 mW Typ.)

Structure

P-channel MNOS IC

Absolute Maximum Ratings (Ta=25°C)

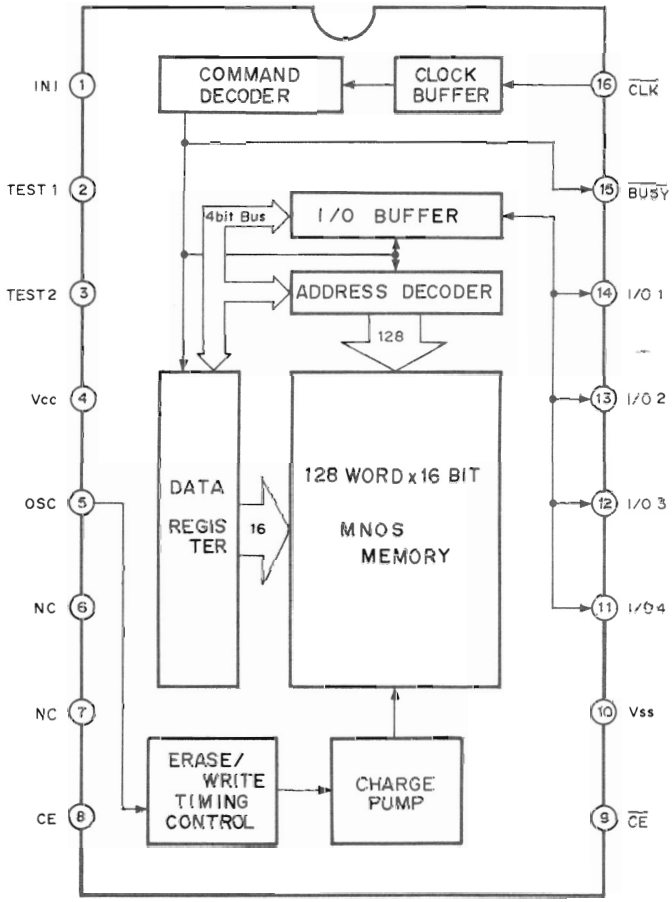
• Supply voltage	V_{CC}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3* to V_{CC}+0.3*	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C

*Note) This value is at normal condition; it may be 0.5V at the transient time (20 to 30 ms).

Recommended Operating Conditions (Ta=−20 to +75°C, Vss=0V)

• Supply voltage	V_{CC}	4.5 to 5.5	V
• Clock frequency	f_{CLK}	DC to 50	kHz
• High level input voltage	V_{INH}	V_{CC}−1.5 to V_{CC}	V
• Low level input voltage	V_{INL}	0 to V_{CC}−3.5	V
• High level input voltage (OSC pin)	V_{INH2}	V_{CC}−0.5 to V_{CC}	V
• Low level input voltage (OSC pin)	V_{INL2}	0 to 1.5	V

Block Diagram and Pin Configuration (Top View)



Pin Description

No.	I/O	Symbol	Description
1	I	INI	Initialize input pin
2		TEST1	Test input pin (normally connected to V_{CC})
3		TEST2	Test input pin (normally connected to V_{CC})
4		V_{CC}	Power supply pin
5	I	OSC	Oscillation pin
6		NC	
7		NC	
8	I	CE	Chip enable input
9	I	$\overline{CE}$	Chip enable input
10		V_{SS}	Power supply pin
11	I/O	I/O4	Address and data I/O pin 4
12	I/O	I/O3	Address and data I/O pin 3
13	I/O	I/O2	Address and data I/O pin 2
14	I/O	I/O1	Address and data I/O pin 1
15	O	$\overline{BUSY}$	BUSY signal output pin
16	I	$\overline{CLK}$	Sync clock input pin

Electrical Characteristics 1.

($Ta=-20$ to $+75°C$, $V_{CC}=5V \pm 10\%$, $V_{SS}=0V$)

Item	Symbol	Pin Name	Condition	Min.	Typ.	Max.	Unit
Power supply current	I_{CC}	V_{CC}	*1		6	9	mA
Input pull-up current	I_{IU}	$\overline{CLK}$, CE, $\overline{CE}$		−45	−90	−180	μA
Input leakage current	I_{ILK}	All input pins				±20	μA
Output leakage current	I_{OLK}	All output pins				±20	μA
Output voltage high level 1	V_{OH1}	I/O1 to I/O4	$I_{OH}=-0.5mA$	$V_{CC}-1.0$			V
Output voltage low level 1	V_{OL1}	I/O1 to I/O4	$I_{OL}=+0.5mA$			+1.0	V
Output voltage high level 2	V_{OH2}	$\overline{BUSY}$	$I_{OH}=-40\mu A$	$V_{CC}-1.0$			V
Output voltage low level 2	V_{OL2}	$\overline{BUSY}$	$I_{OL}=+40\mu A$			+1.0	V
Input current 2 *2	I_{IN2}	OSC	$V_{IN2}=V_{CC}-0.5V$		1.0	1.5	mA

Note) *1 Includes the erasure and write times.
*2 t_{OSCH} See Timing Chart (3)

Electrical Characteristics 2.

(Ta=−20 to +75°C, V_{CC}=5V ±10%, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	t_{WH}		10			μs
Clock pulse width	t_{WL}		10			μs
Data input setup time	t_{DS}		0			μs
Data input hold time	t_{DH}		0			μs
Rise/fall time	t_r, t_f				1	μs
Clock setup time	t_{CKS}		10			μs
Data delay time	t_{OD}				5	μs
Number of read	N_R	Refresh time	10^7	10^9		time
Write time	t_W	C=0.47μF, R=150 kΩ		30	60	ms
Erasure time	t_E	C=0.47μF, R=150 kΩ		30	60	ms
Memory retention time 1	t_{MH1}	After rewriting 10^4 times Store at Ta=85°C	10			year
Memory retention time 2	t_{MH2}	After rewriting 10^5 times Store at Ta=85°C	1			year

***Note)** It indicates the value during C=0.47 μF and R=150 kΩ, and for example, it becomes tw (tz)=40 ms(typ.), 80 ms(max.) when during C=0.1 μF and R=82 kΩ (See Fig. 1).

Command Table

INI	CE	$\overline{CE}$	I/O1	I/O2	I/O3	I/O4	Operational command
L	H	L	L	L	H	L	DR: Memory read
L	H	L	H	L	H	L	DW: Memory write
L	H	L	X	X	L	L	No operation
L	H	L	X	X	L	H	No operation
L	H	L	X	X	H	H	No operation
L	L	L	X	X	X	X	No operation
L	L	H	X	X	X	X	No operation
L	H	H	X	X	X	X	No operation
H	X	X	X	X	X	X	No operation

Note) X denotes no relationship.

Description of Circuit Operations

Interactions between the memory and controller are performed by using two types of commands, the DR (Data Read) and DW (Data Write). The DW has two methods; namely, one method is to generate automatically by attaching CR to the OSC pin the erasure write-in time, and the other is by applying erasure write-in pulses to the OSC pin from the controller. Signals entered from the I/O bus are taken into the circuit at the fall time of $\overline{CLK}$, and the output signals from the memory are obtained at the rise time of the $\overline{CLK}$. The signals to be sent to the memory are switched while the $\overline{CLK}$ is in "H" level and they are fixed when the level is "L".

(1) DR: Data Read (Memory Read)

Entering the DR mode "L, L, H and L" from the I/O bus and entering the 7 bit address data at the next two clock cycles result in reading out the memory cell contents in the succeeding single clock cycle. Then, in the next four clock cycles, 16 bit data of D1 to D16 are output from the I/O bus, at every 4 bits time.

Now, a detailed description of the circuit operations will be given below.

- First the initialization is applied, then after 10 μs the first clock pulse is entered. The data read mode "L, L, H and L" which have been set to the I/O bus are taken into the circuit at the fall time of the first clock pulse. At the same time, the $\overline{BUSY}$ signal is output from the memory and goes into the BUSY state.
- At the fall time of the second clock and the third clock pulses, the address data "A0, A1, A2 A3" and "A4, A5, A6" are taken into the circuit, respectively.
- At the memory cell contents are read out internally at the fall time of the fourth clock pulse, the data "H, H, H and H" should be set to the I/O bus.
- At the rise time of the fourth clock pulse, the 4 bit data of "D1 to D4" are output to the I/O bus, in synchronization with the CLK. Likewise, at the rise time of the fifth clock pulse the data of "D5 to D8", at the rise time of the sixth clock pulse the data of "D9 to D12", and at the rise time of the seventh clock pulse the data of "D13 to D16" are output into I/O bus. That means a total of 16 bits are output during the four clock cycles.
- At the fall time of the ninth clock pulse, the data "H, H, H and H" are taken into the circuit, and the $\overline{BUSY}$ output is released.

Note) X denotes no relationship.

(2) DW1: Data Write 1 (Memory Write in OSC automatic transmission)

This paragraph describes when C-R (C=0.47 μF, R=150Ω typ.) is atttached to the OSC pin.

Enter the DW mode "H, L, H and L" from the I/O bus and enter the 7 bit address data into the next two clock cycles. The data being written in after 1 clock is 4 bits, so with a total of 4 clocks 16 bits are input. In the after the data has set, the internal oscillation circuit automatically starts the operation and makes the clock timings of every 30 ms (typ.) for erasure and writing.

Whether the erasure/write operation has been completed can be determined by observing the $\overline{BUSY}$ output signal.

A detailed description of the circuit operations for the data write will be given below.

- The initialization is applied first, and after 10 μs the first clock pulse is input. The data write mode "H, L, H and L" set in the I/O bus is taken into the circuit at the fall time of the first clock pulse. At the same time, the $\overline{BUSY}$ signal is output from the memory and memory becomes into the BUSY state.
- At the fall times of the second and third clock pulses, the address data "A0, A1, A2, A3" and "A4, A5, A6" are taken into the circuit, respectively.
- At the fall time of the fourth clock pulse, the data "H, H, H and H" are set in the I/O bus.
- At the fall time of the fifth clock pulse the data of "D1 to D4", at the fall time of the sixth clock pulse the data of "D5 to D8", at the fall time of the seventh clock pulse the data of "D9 to D12", and at the fall time of the eighth clock pulse the data "D13 to D16" are taken into the circuit, respectively, from the I/O bus, 4 bits at a time. The 16 bit data are set to the register within the circuit.
- At the rise time of the eighth clock pulse the OSC pin automatically starts oscillation. During the first oscillation cycle the erase operation and during the second oscillation cycle the write operation are automatically performed.

(3) DW2: Data Write 2 (Memory Write-in: Apply OSC external pulse)
Described hereafter is the case in which erasure write pulse is applied to the OSC pin from the controller.
Input DW mode "H, L, H, L" from I/O bus, enter address data 6 bits by the next 2 clocks, and, after 1 clock, input 16 bit write-in data (4 bit × 4 clock). Heretofore, it has been identical to "DW1". After the data has been set, enter erasure write in pulses (Respectively over 30 ms) to the OSC pin. Details of the operations are given below.
- As it is the same as "DW1" until data is set, the description is omitted.
- After the rising of No.8 clock, the low period t_E (30 ms), high period t_{OSCH} (5 to 50 μs), and low period tw (30 ms) pulses are input to the OSC pin. Operations of erase at the t_E time, write at the t_{OSCH} + tw time are carried out.
- "H, H, H, H" are fetched from the I/O bus at the falling of the No.9 clock, and reset is applied to the internal counter. When OSC pin is made high after the end of tw, the $\overline{BUSY}$ output is also released.

Notes on Application

(1) Power-On Reset Circuit
The power-on reset circuit is built-in the memory internal circuit. When the initialization is applied using the power-on reset circuit, the following items should be observed:
- The power supply should be smoothly raised and be noise free.
- The power supply rise time t_R should be $0.1 < t_R < 50$ (ms).
- At the power rise time, the input pin should not be lower than Vss and higher than Vcc.

(2) Initialization
When the power supply is turned on, the initialization should be applied externally whenever possible. In the normal operation when the memory is not being accessed, hold the initialization state so that erroneous changes of data by noises can be avoided.
When the initialization is applied, either the INI or $\overline{CE}$ is set to high, or the CE is set to low. Those pins perform the same function. Note that the initialization should not be made when the $\overline{BUSY}$ signal is being output (that is when the memory is in BUSY state). Otherwise, the access operation made immediately before is not guaranteed.

(3) Continuous Access
When the memory is continuously accessed, memory access should be started after 10 μs of the release of $\overline{BUSY}$ signal or release of the initialization by switching one of the signals of INI, $\overline{CE}$, CE, etc.

(4) Pull-up Resistor
Basically, the pull-up resistor is not necessary for the output pins (I/O1 to I/O4 and $\overline{BUSY}$). I/O1 to I/O4 are kept at high impedance in the input mode. Since $\overline{BUSY}$ outputs low during the memory operation and outputs high in the stand-by mode, it is recommended not to attach a pull-up resistor.
If the pull-up resistors are required for system stabilization, the following values should serve as a standard.

I/O1 to I/O4	Higher than 22 kΩ
$\overline{BUSY}$	Higher than 120 kΩ

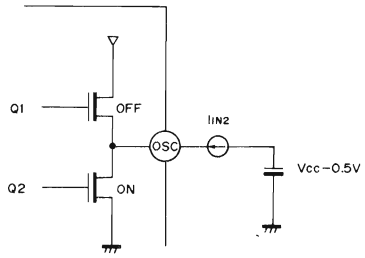
(5) E/W (Erase/Write) Oscillation

By attaching the CR externally to the OSC pin, the oscillation is automatically started from the rise time of the ninth clock pulse of the "DW" to generate the timings of the erasure and writing. The standard values of the CR are set as follows: C=0.47 μF and R=150 kΩ. At this time, the Erase/Write times become as follows: Erase=30 ms (typ.) and Write=30ms (typ.). When other constants are to be selected, determine the values in the recommended range by referring to Fig. 1. When it is out of the range, the memory retention time may not be guaranteed.

(6) Caution to be exercised when controlling the time of erasure and write-in from the exterior.

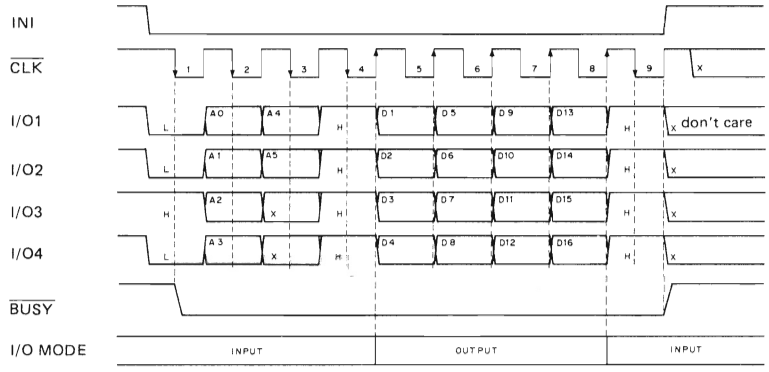
When it is considered to make the OSC pin over (V_{CC}—0.5V) during the t_{OSCH}, the Q2 in the figure below is turned ON and the current flows into the IC. Therefore the control IC must have the capability of the drive of over 1.5 mA.

Moreover, both Q1 and Q2, the OSC pin during the t_E and t_W is OFF and it is at high impedance. Except for Erase/Write, Q1 only is ON (Ron, typ. = 10 kΩ) and the OSC pin is pulled-up.

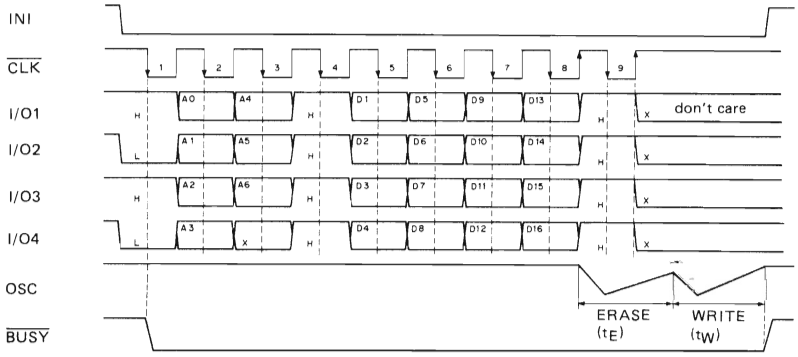


Timing Chart

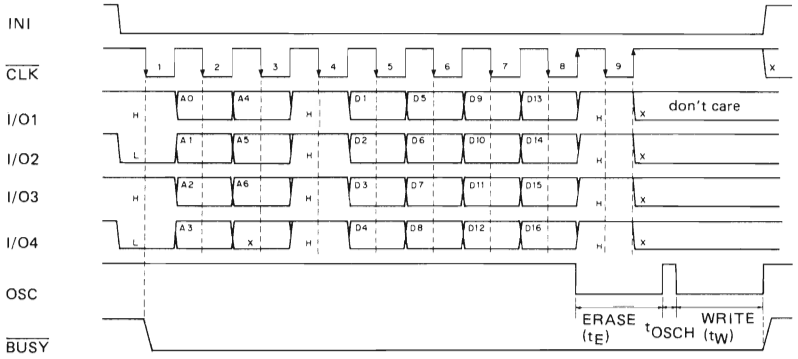
(1) DR: Data Read



(2) DW1: Data Write 1



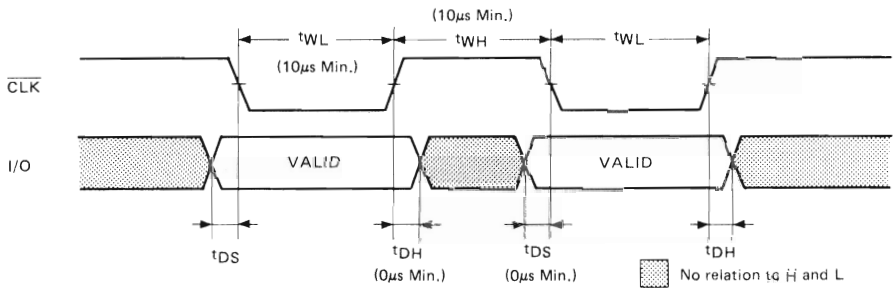
(3) DW2: Data Write 2



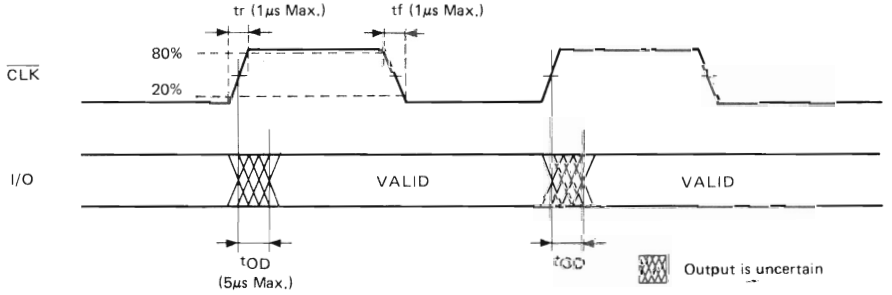
Item	Min.	Max.
t_E	30msec	
t_W	30msec	
t_{OSCH}	5μsec	50μsec

I/O Timing Chart

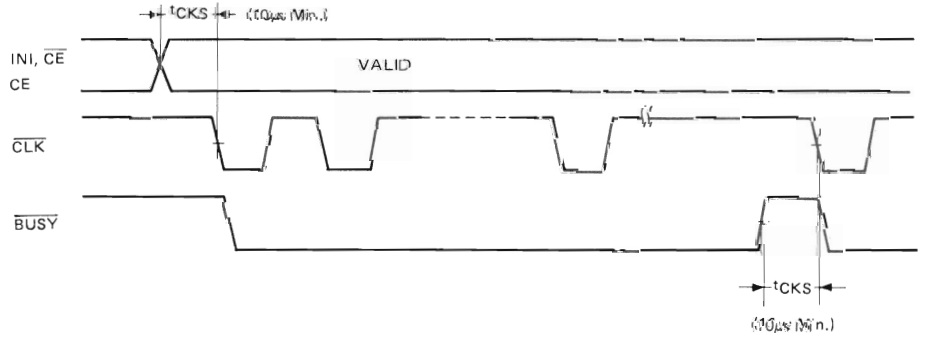
Input Mode



Output Mode



Access Mode



OSC Pin constant

(V_{CC}=5V ±10%, V_{SS}=0V, Ta=25°C)

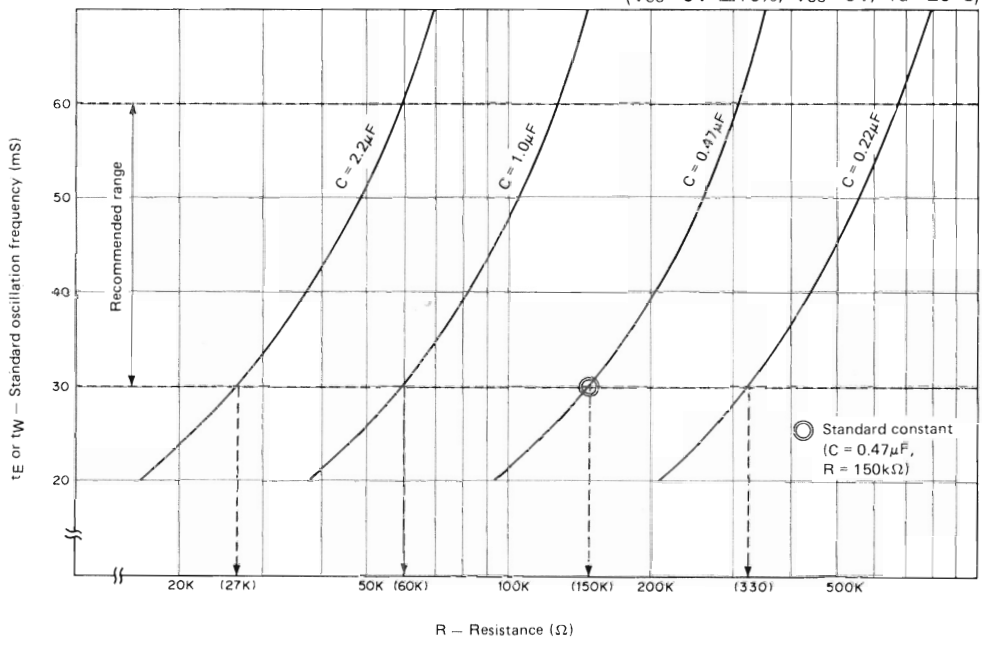
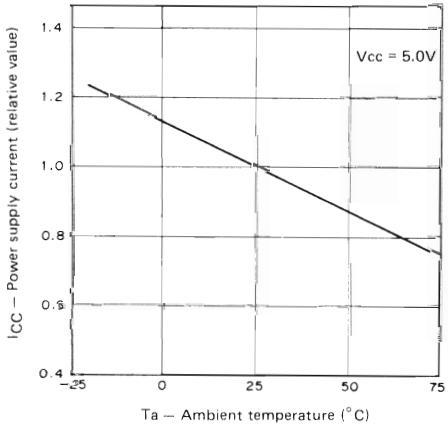
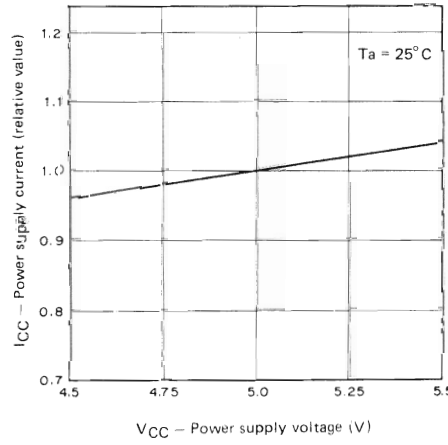


Fig. 1

Power supply current temperature characteristics

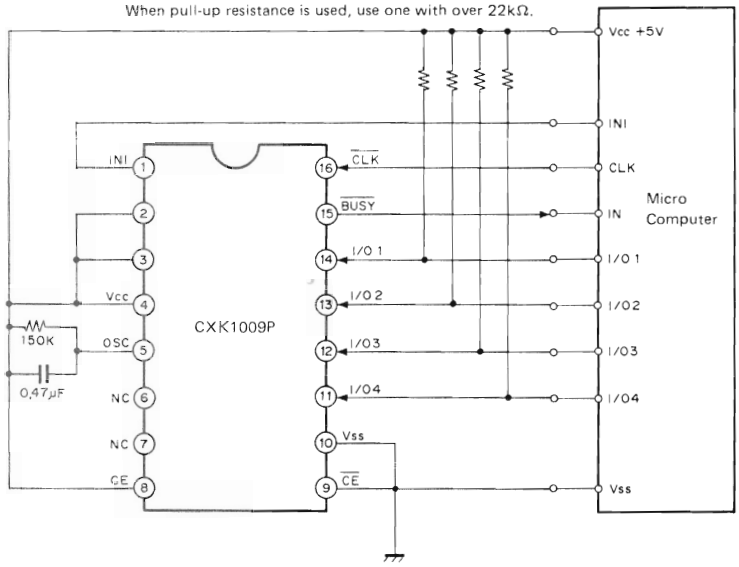


Power supply current vs. Power supply voltage characteristics

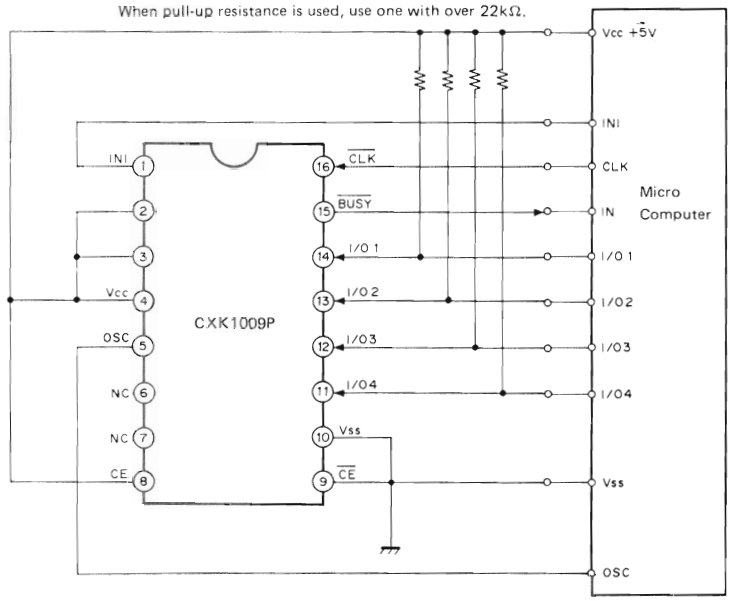


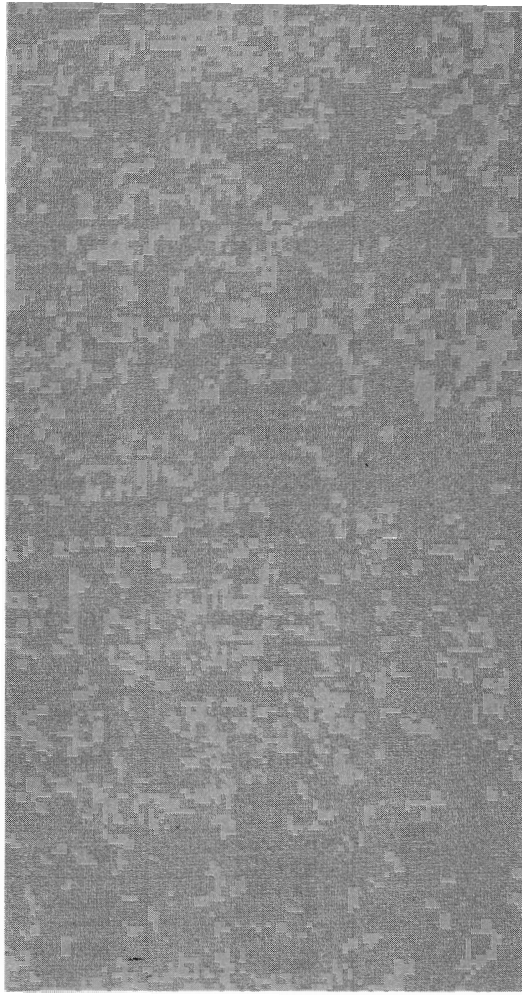
Application Circuits

1) When CR is oscillated

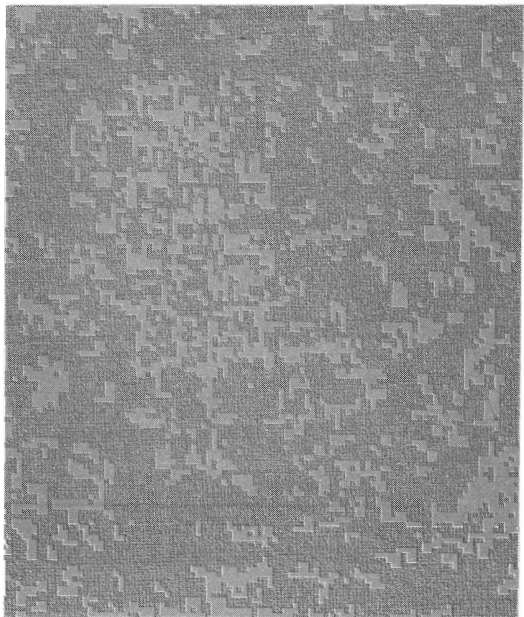


2) When controlled by exterior





Supplementary Function



3) Supplementary Function

Type	Function	Page
CX-7948	Hatch Signal Generator for TV	191
CX-7958	TV Screen Display (CRT Display)	201
CX20100	RGB Interface for CTV	219
CX20106A	Preamplifier for Remote Control Use	248
CX20112	US Audio Multiplexing Decoder	255
CX20125	Dynamic Picture	276
CX20159	Power Supply IC for TV	283
CXA1011P/M	dbx-TV Noise Reduction IC	290
CXA1024S	RGB Interface Automatic White Balance	306
CXA1044P	RGB Interface for Ultra-High Resolution Display	328
CXD1053S	Picture-in-Picture Memory Control IC for TV	340
CXD1054S	Picture-in-Picture Data Control IC for TV	353
CXK1201P	Double Scan Converter (P)	364
※BX-1330 BX-1396	Infrared Ray Remote Control Receiver	376
※BX-1387 BX-1407	Infrared Remote Control Receiver	382
※BX-1393 BX-1408	Infrared Remote Control Receiver	389
※BX-1398 BX-1409	Infrared Remote Control Receiver	395
※BX-1435	US Multiplexing Sound Decoder Module	402
※BX-1436	US Multiplexing Sound Decoder Module	410

※ Hybrid ICs (P) : Preliminary

Hatch Signal Generator for TV

Description

The CX-7948 is an IC to generate a composite sink signal and three kinds of hatch signals in non-interlace by connecting a 3.58 MHz crystal oscillator, which is best for adjusting registrations such as monitors and projects.

Function

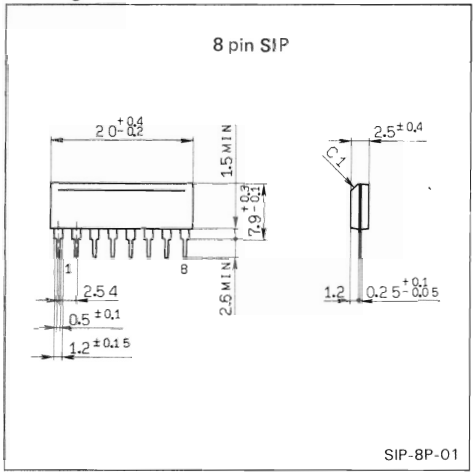
- Hatch Signal Generator

Structure

Silicon Gate CMOS IC

Package Outline

Unit: mm



Absolute Maximum Ratings (Vss = 0V, Topr = −15°C to +70°C)

• Supply voltage	V_{DD}	0.3 to 7	V
• Input voltage	V_{IN}	−0.3 to V_{DD} +0.3	V
• Output voltage	V_{OUT}	−0.3 to V_{DD} +0.3	V
• Output pin maximum current	|Imax|	10	mA
• Storage temperature	Tstg	−50 to +125	°C
• Operating temperature	Topr	−15 to +70	°C
• Allowable power dissipation	PD	100	mW

Recommended Operating Condition

• Supply voltage	V_{DD}	4.5 to 5.5	V

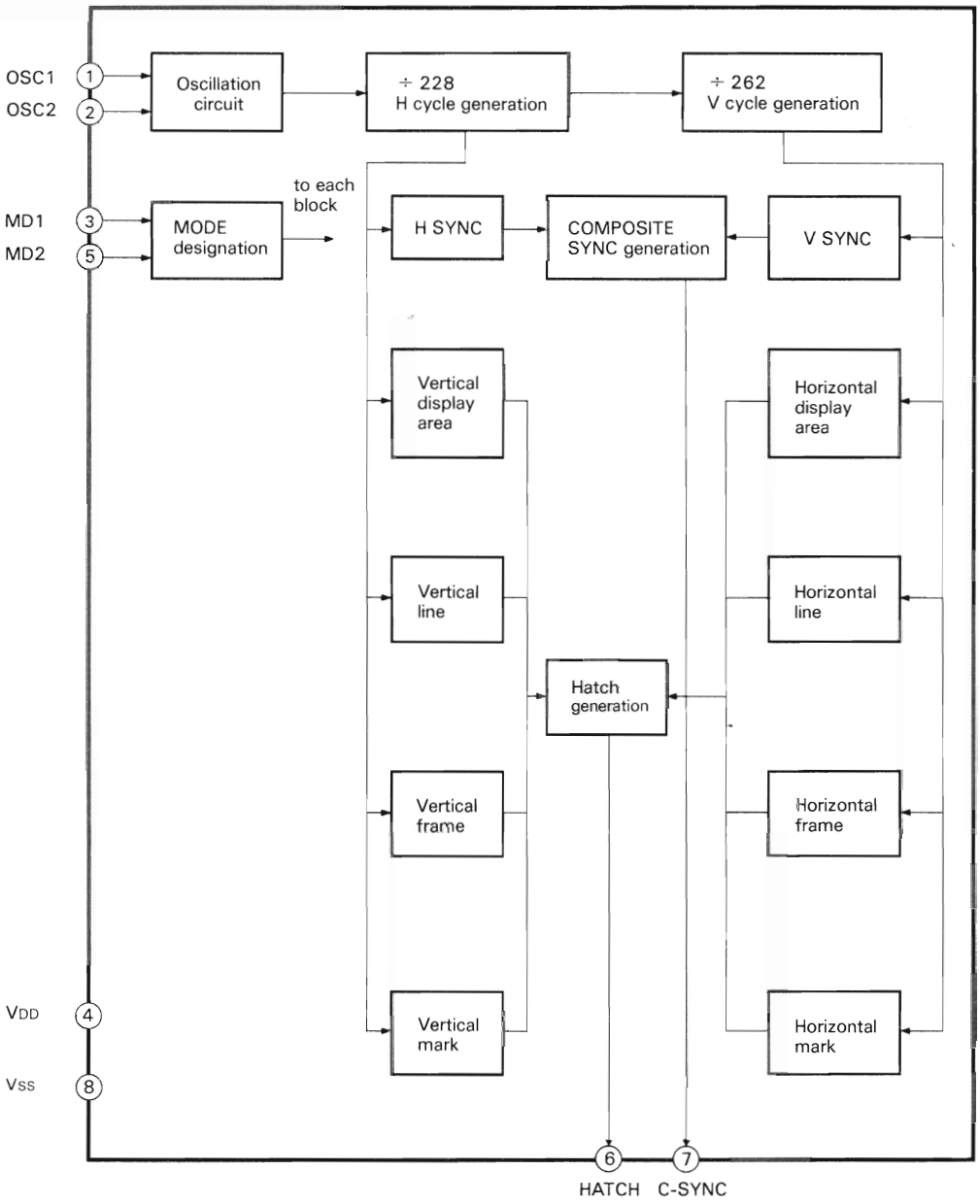
Electrical Characteristics

(Ta = −15°C to +70°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V)

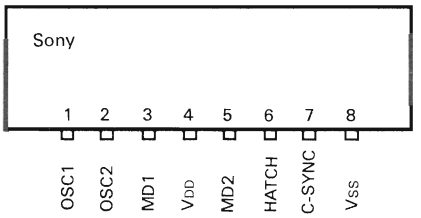
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input voltage (1)	$V_{IH(1)}$		0.8V_{DD}		V_{DD}	V	Apply to the respective 3, 5 pins.
	$V_{IL(1)}$		0		0.2V_{DD}	V	
Input voltage (2)	$V_{IH(2)}$		0.8V_{DD}		V_{DD} +1.0	V	Apply to the respective 2 pin.
	$V_{IL(2)}$		−1.0		0.2V_{DD}	V	
Input current	I_{IH}	V_{IN} = V_{DD}			10	μA	
	$-I_{IL}$	V_{IN} = 0V			10	μA	
Output current	$-I_{OH}$	$V_{DD}-V_{OUT}$ = 0.5V	1.0			mA	
	I_{OL}	V_{OUT} = 0.5V	1.0			mA	
Consumption current	I_{DD}	No load			7	mA	*
Operating frequency	f			3.58		MHz	*

* **Note)** Connecting a 3.58 MHz crystal oscillator and capacitor to Pins 1, 2. (See the Application Circuit)

Block Diagram

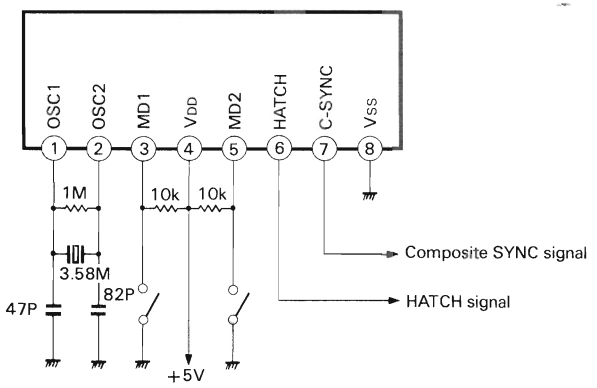


Pin Configuration



No.	Symbol	I/O	Function
1	OSC1	O	For self-oscillation (3.58 MHz crystal oscillator)
2	OSC2	I	
3	MD1	I	Hatch pattern select input
4	V_{DD}		+5V power supply
5	MD2	I	Hatch pattern select input
6	HATCH	O	Hatch signal output
7	C-SYNC	O	Composite sink signal output
8	V_{SS}		Ground

Application Circuit



Note) For capacitor, use the ceramic capacitor used for temperature compensation whose allowable deviation is ±5%.

Description of Function

CX-7948 is a self-oscillator connected to the 3.58 MHz crystal oscillator. Besides dividing its oscillation frequency by a counter and generating the composite sink (non-interlace), it generates three types of hatch patterns.

1) MODE designation

MD2	MD1	Hatch pattern
L	L	Consumer Cross
L	H	Consumer Mesh
H	L	Instruction Mesh
H	H	Oscillation stop

Note 1) After changing the MODE designation input, term output signal (HATCH, C-SYNC) of approx. 20 ms is undefined.
2) Chatter killer circuit is not attached to the MODE designation input.

2) HATCH output

Three types of hatch patterns below are by the above MODE designation input.

Consumer Cross See Fig. 1
Consumer Mesh See Fig. 2
Instruction Mesh See Fig. 3

Black lines in the figures indicate output of +5V. In other cases, output is 0V.

3) C-SYNC output

The wave form of C-SYNC is shown in Fig. 4.

Consumer Cross (Black lines represent white parts on the display. Others are black.)

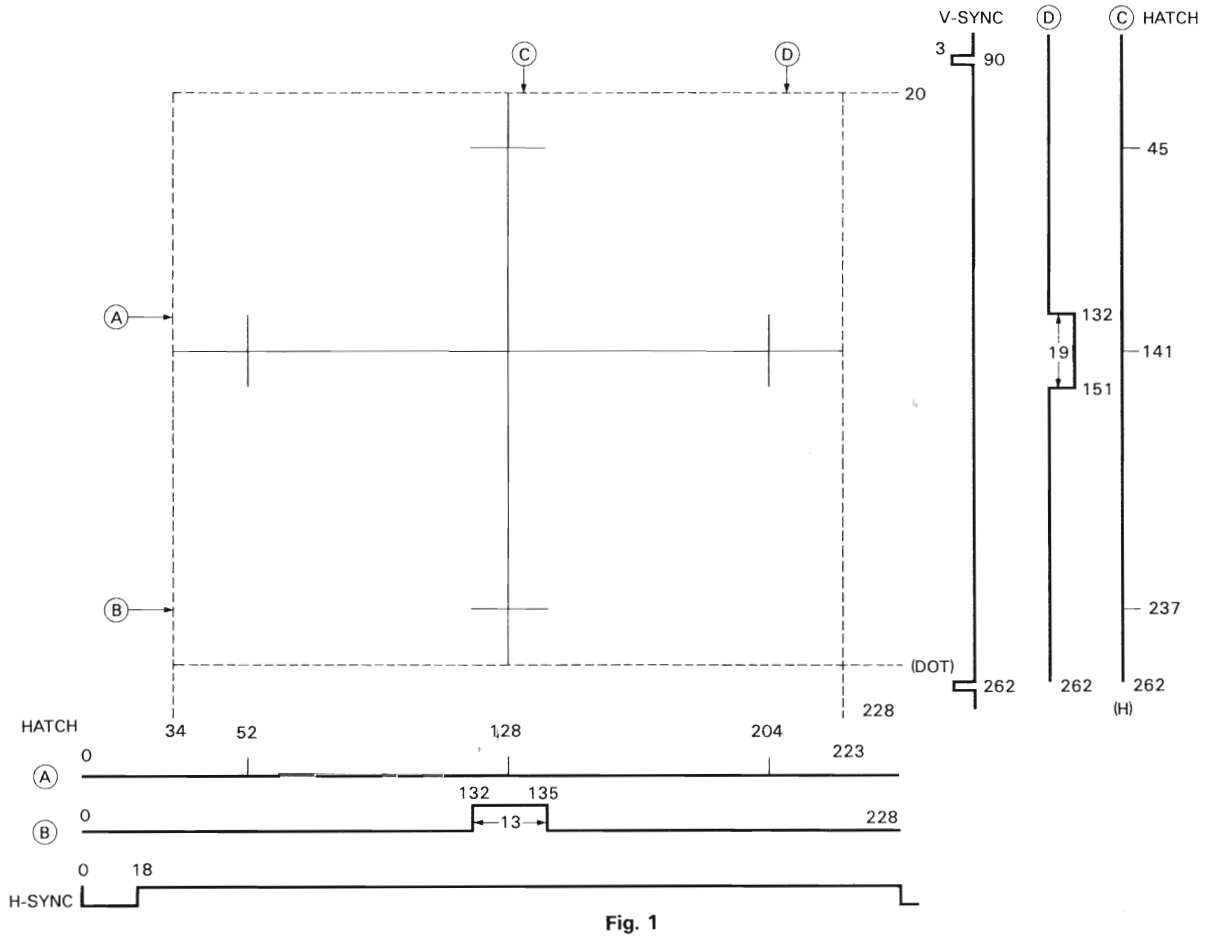


Fig. 1

Note) Dot is the 3.58 MHz clock. H is the horizontal interval.

Consumer Mesh (Black lines represent white parts on the display. Others are black.)

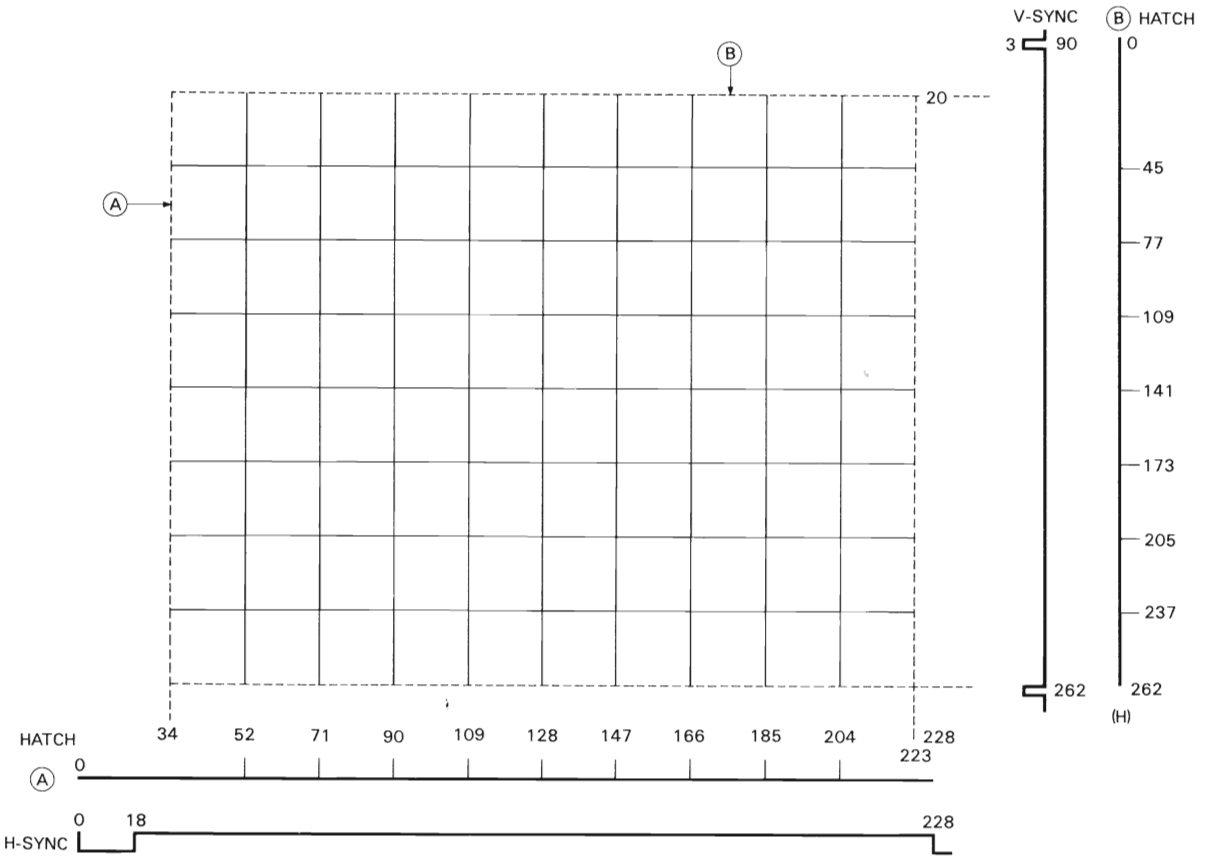


Fig. 2

Note) Dot is the 3.58 MHz clock. H is the horizontal interval.

SONY

Instruction Mesh (Black lines represent white parts on the display. Others are black.)

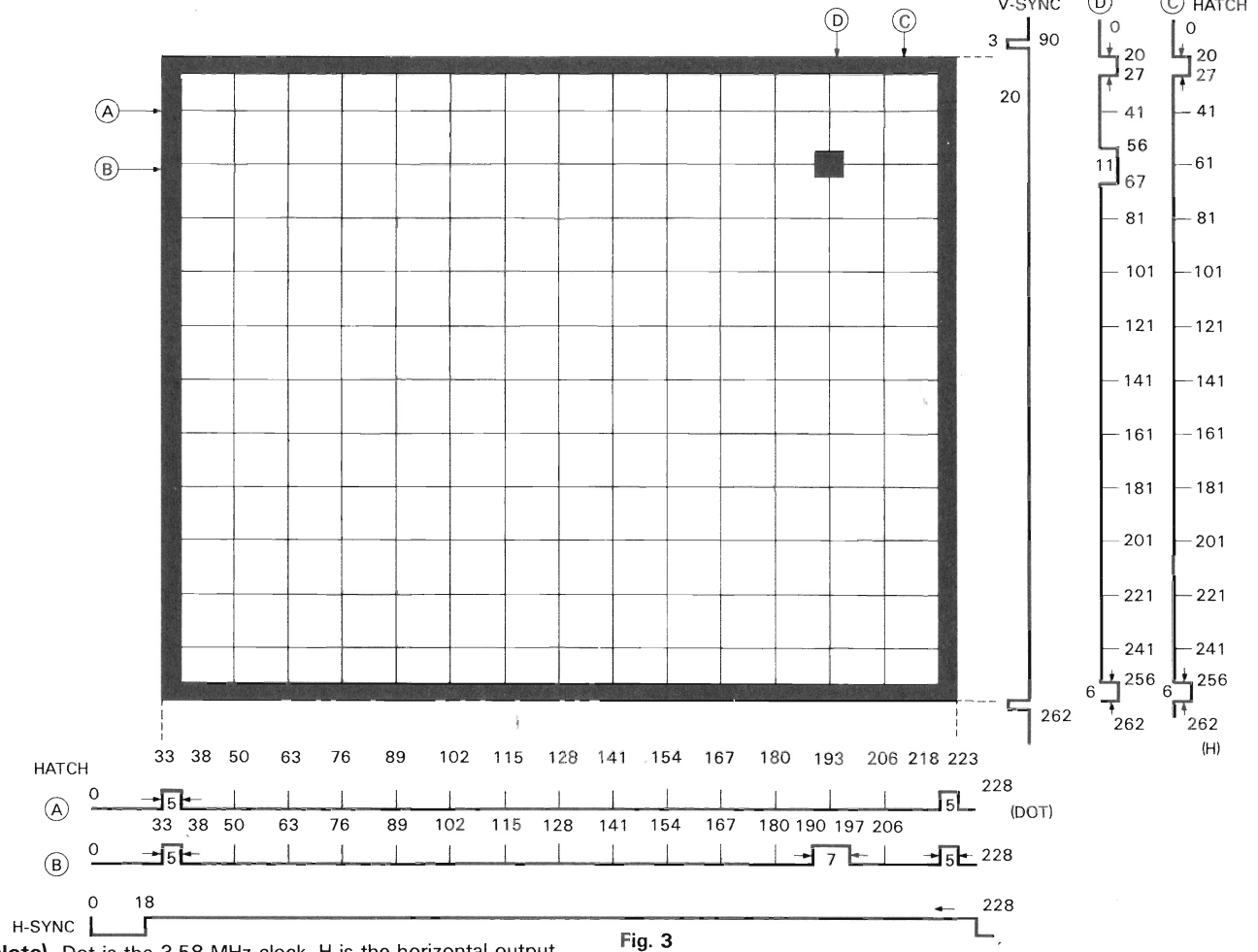


Fig. 3

Note) Dot is the 3.58 MHz clock. H is the horizontal output.

SONY

C-SYNC Output

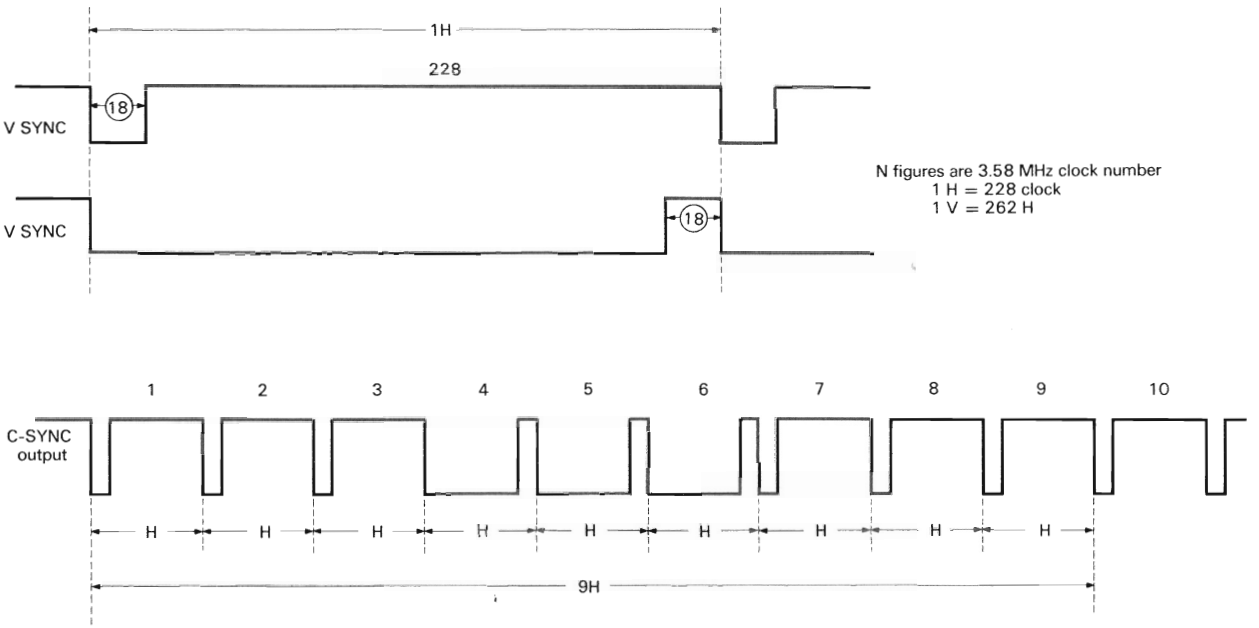
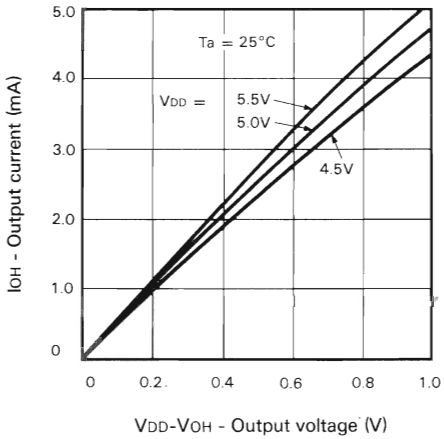
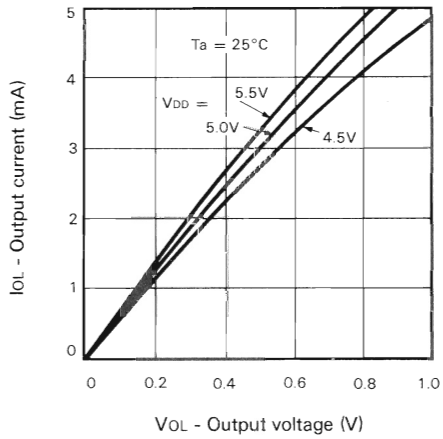


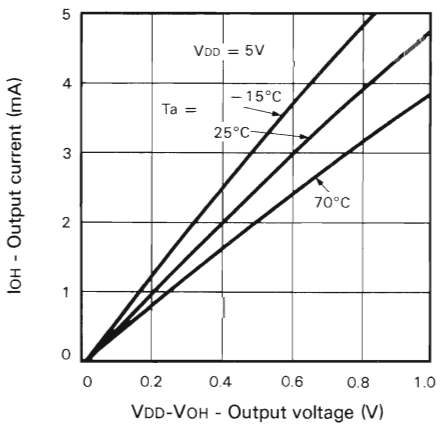
Fig. 4

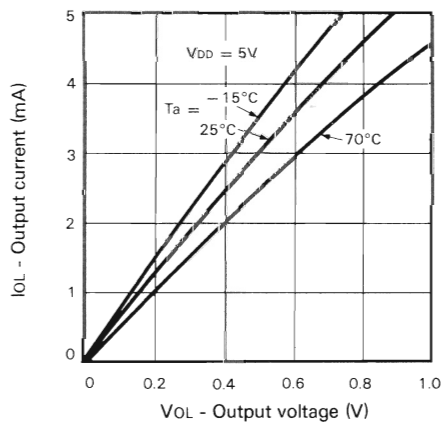
Output characteristics of VDD (HATCH, C-SYNC)





Output characteristics of temperature (HATCH, C-SYNC)





TV Screen Display (CRT Display)

Description

The CX-7958 is a display controller CMOS IC which can be used to display 55 kinds of alphanumeric characters and graphics with 8 colors on the TV screen.

Features

- 7 characters × 3 digits of alphanumeric characters and graphics display
- Display with 64 bars
- Provided with double character rounding function with character structure of 5×7 dots
- Predetermined time length display by incorporated monostable multivibrator
- Display location adjustment by incorporated monostable multivibrator
- Jitter elimination with the vertical synchronizing signal
- CPU interface by serial bus

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{DD}	V_{SS}−0.3 to +7	V
• Input voltage	V_I	V_{SS}−0.3 to V_{DD}+0.3*	V
• Output voltage	V_O	V_{SS}−0.3 to V_{DD}+0.3	V
• Operating temperature	Topr	−10 to +65	°C
• Storage temperature	Tstg	−55 to +150	°C

* Only pins 1 and 12 are specified as V_I=−2.0 to V_{DD}+2.0V (Ta=25°C).

Recommended Operating Conditions

• Supply voltage	V_{DD}	4.5 to 5.5 (Typ.5V)	V
• Operating temperature	Topr	−10 to +65	°C

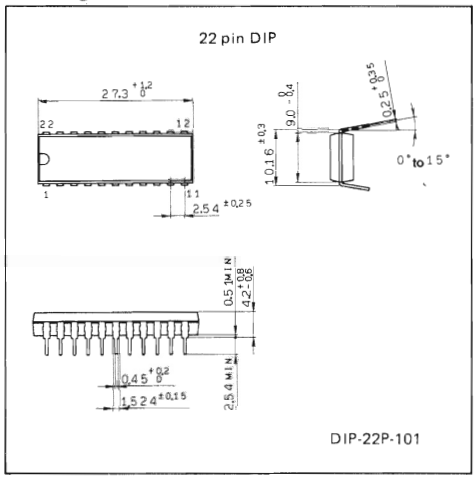
Input/output capacity

• Input pin	C_I	10	pF
• Output pin	C_O	10	pF
• I/O pin	$C_{I/O}$	10	pF

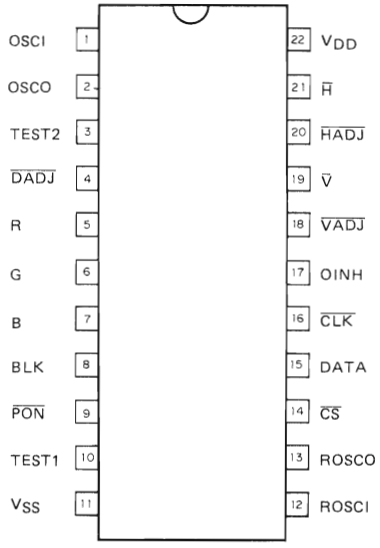
Condition V_{DD}=V_I=0V, f_M=1 MHz

Package Outline

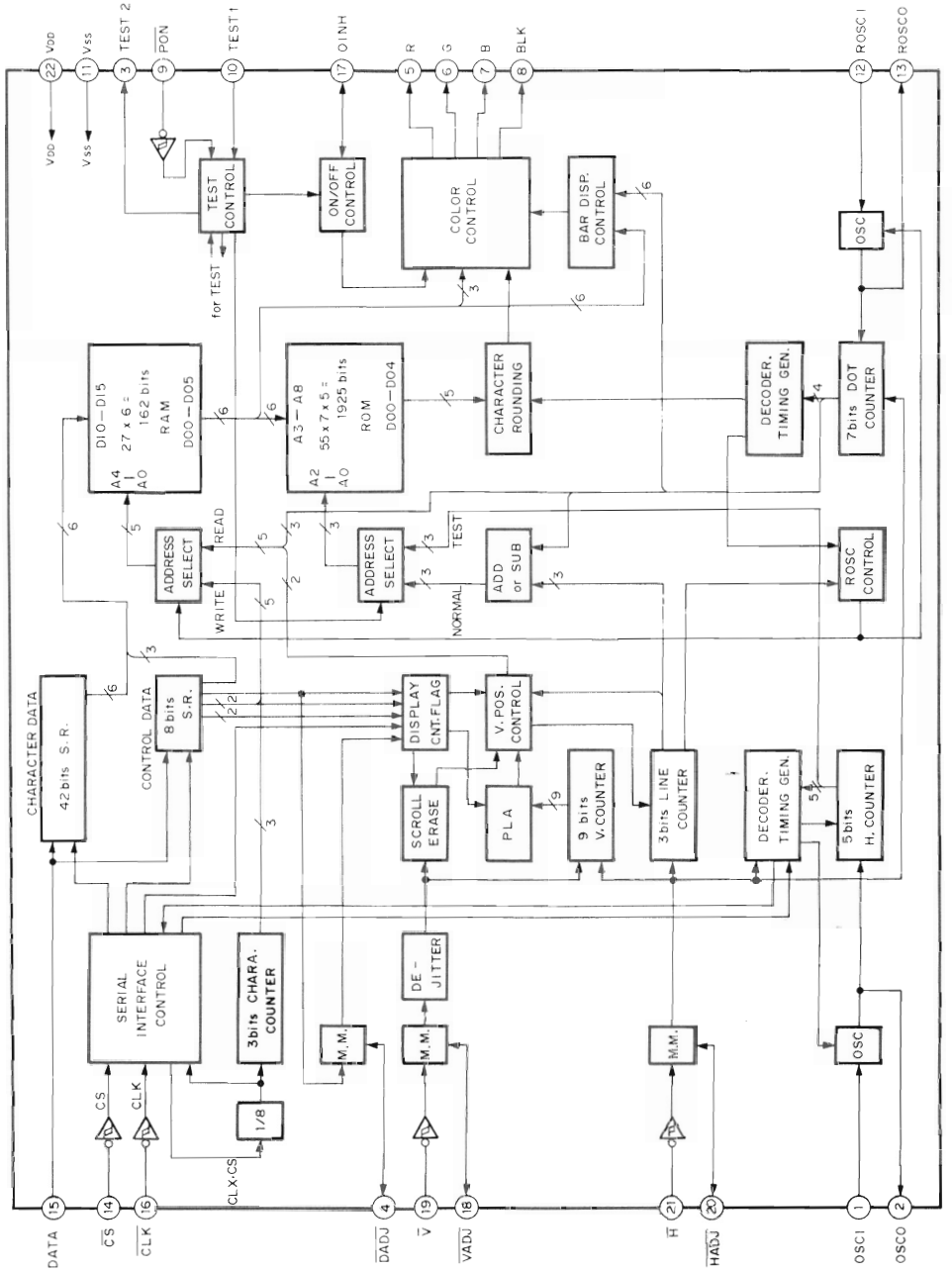
Unit: mm



Pin Configuration



Block Diagram



Pin Description

No.	Name	I/O	Description
1	OSCI	I	An oscillation circuit input pin of oscillating frequency of 500 kHz.
2	OSCO	O	An oscillation circuit output pin of oscillating frequency of 500 kHz.
3	TEST2	O	An output pin of the incorporated monostable multivibrator. It outputs EXCLUSIVE OR for the horizontal display location setting monostable multivibrator, vertical display location setting monostable multivibrator and display time setting monostable multivibrator.
4	$\overline{\text{DADJ}}$	I/O	A CR externally attached pin of display time setting monostable multivibrator.
5	R	O	A data output pin for Red display. The polarity is positive logic.
6	G	O	A data output pin for Green display. The polarity is positive logic.
7	B	O	A data output pin for Blue display. The polarity is positive logic.
8	BLK	O	A dot data output pin provided for blanking the main signal (For example, the signal sent by ON AIR). OR of the R, G and B pins and the polarity is positive logic. In case of bargraph display, the BLK pin can be set at "L" by selecting trasparent color due to setting of the control flag.
9	$\overline{\text{PON}}$	I	A reset pulse input pin. The polarity is negative logic. Possible to be reset when applying the power supply by only attaching the CR externally, as a Schmitt circuit is being incorporated. By resetting, the internal register is cleared and the display is also erased. However, the content of the internal RAM is unchanged.
10	TEST1	I	A test mode setting input pin. Normally, it is fixed at "L".
11	Vss	Power supply	0V
12	ROSCI	I	An oscillation circuit input pin of oscillating frequency of 5 MHz.
13	ROSCO	O	An oscillation circuit output pin of oscillating frequency of 5 MHz.
14	$\overline{\text{CS}}$	I	A control signal input pin of the serial interface. The polarity is positive logic. Incorporates a Schmitt circuit. Writing into the internal RAM is commenced by transferring the data after changing the CS pin to "L" from "H" and set at "H" after transfer has been completed.
15	DATA	I	A data input pin of the serial interface. The polarity is positive logic.
16	$\overline{\text{CLK}}$	I	A clock input pin of the serial interface. Incorporates a Schmitt circuit. It fetches the data at the rising of the negative polarity of clock.

No.	Name	I/O	Description
17	OINH	I/O	An output inhibiting input pin of R, G, B and BLK pins. It is in normal operation when the OINH pin is at "L", and when at "H" all the R, G, B and BLK pins become "L". The internal state is output from the OINH pin when turning it into the test mode by setting the TEST1 pin at "H".
18	$\overline{\text{VADJ}}$	I/O	A CR externally attached pin of the vertical display location setting monostable multivibrator. The monostable multivibrator starts to operate at the falling of the vertical synchronizing signal input from the $\overline{\text{V}}$ pin. It is possible to input the negative polarity pulse from the $\overline{\text{VADJ}}$ pin by connecting the $\overline{\text{V}}$ pin to the V_{DD} or V_{SS} pin. In this case, eliminate the externally attached CR.
19	$\overline{\text{V}}$	I	A trigger input pin of the vertical display location setting monostable multivibrator. The polarity is negative logic. Incorporates a Schmitt circuit.
20	$\overline{\text{HADJ}}$	I/O	A CR externally attached pin of the horizontal display location setting monostable multivibrator. The monostable multivibrator starts to operate at the falling of the horizontal synchronizing signal input from the $\overline{\text{H}}$ pin. It is possible to input the negative polarity pulse from the $\overline{\text{HADJ}}$ pin by connecting the $\overline{\text{H}}$ pin to the V_{DD} or V_{SS} pin. In this case, eliminate the externally attached CR.
21	$\overline{\text{H}}$	I	A trigger input pin of the horizontal display location setting monostable multivibrator. The polarity is negative logic. Incorporates a Schmitt circuit.
22	V_{DD}	Power supply	+5V

Electrical Characteristics

DC Characteristics

Ta=−10°C to +65°C, V_{DD}=+5V±10%, V_{SS}=0V

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Input voltage 1	"H" level	V_{IH1}		0.8V_{DD}		V_{DD}	V	Note 1
	"L" level	V_{IL1}		V_{SS}		0.2V_{DD}	V	
Input voltage 2	"H" level	V_{IH2}		0.8V_{DD}		V_{DD}	V	Note 2
	"L" level	V_{IL2}		V_{SS}		0.2V_{DD}	V	
	Hysteresis voltage	V_H			0.5		V	
Input pin leakage current		I_{LI}	V_I=0 to V_{DD}			±2	μA	Note 3
I/O pin leakage current		I_{LZ}	V_I=0 to V_{DD}			±10	μA	Note 4
Output current	"H" level	I_{OL}	V_{OH}=2.5V	−1			mA	Note 5
	"L" level	I_{OL}	V_{OL}=0.4V	2.5			mA	
Current consumption		I_{DD}	OSC=500kHz ROSC=5MHz		3	10	mA	Non-loaded

Note) 1. Apply to the respective TEST1, OSCI, ROSCI, DATA and $\overline{\text{OINH}}$ pins.
2. Apply to the respective $\overline{\text{PON}}$, $\overline{\text{H}}$, $\overline{\text{V}}$, $\overline{\text{HADJ}}$, $\overline{\text{VADJ}}$, $\overline{\text{DADJ}}$, $\overline{\text{CS}}$, and $\overline{\text{CLK}}$ pins.
3. Apply to the respective TEST1, $\overline{\text{PON}}$ OSCI, ROSCI, $\overline{\text{HADJ}}$, $\overline{\text{VADJ}}$, $\overline{\text{DADJ}}$, $\overline{\text{H}}$ and $\overline{\text{V}}$ pins.
4. Apply to the respective $\overline{\text{HADJ}}$, $\overline{\text{VADJ}}$, $\overline{\text{DADJ}}$, and OINH pins.
5. Apply to the respective R, G, B and BLK pins.

Operating Frequency

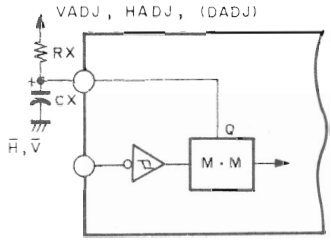
V_{DD}=5V±10%, Ta=−10°C to +65°C

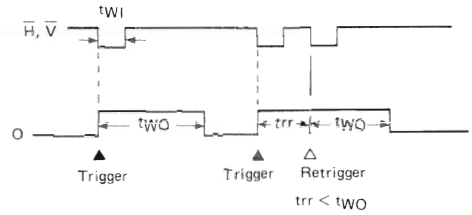
Item	Symbol	Min.	Typ.	Max.	Unit
Oscillating frequency (1)	f_{OSC}		0.5	0.6	MHz
Oscillating frequency (2)	f_{ROSC}		5.0	5.5	MHz

(1) OSCI pin and OSCO pin, (2) ROSCI pin and ROSCO pin

Monostable Multivibrator Characteristics (V_{DD}=+5V, Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Trigger width	t_{WI}	500			ns
Retrigger time	trr	0			ns
Output pulse width	two			±50	%
Externally attached resistor	RX	5		1000	kΩ
Externally attached capacitor	CX	No limits			μF

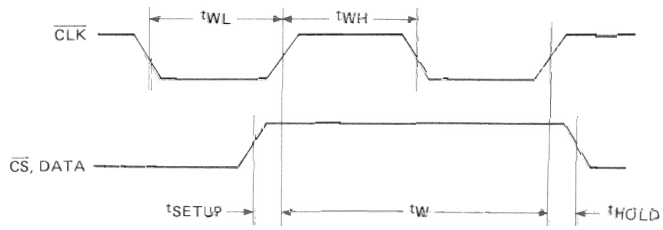




T_{WO} = 0.65 CXRX

Switching Characteristics (V_{DD}=5V±10% Ta=−10 to +65°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock cycle	tW	1000			ns
Clock pulse width	tWL, tWH	200			ns
Data setup time $\overline{CS}$ DATA→$\overline{CLK}$	tSETUP	100			ns
Data hold time $\overline{CS}$ DATA→$\overline{CLK}$	tHOLD	100			ns



Description of Function

Display function

1. Screen structure

   There are four display sections such as the 1st to 4th on the screen as shown in Fig. 1. Maximum 7 characters display is possible to the respective 1st to 3rd dispaly sections, and 64 vertical slits display is possible to the 4th display section.

   The horizontal display locations of the respective display sections are as shown in Fig. 2, and the vertical display locations of the respective display sections are as shown in Fig. 3.

2. Character structure

   It can display 55 kinds of characters each of which is structured with 5×7 bit provided by the incorporated character generator. The shapes and codes of the individual characters are as shown in Fig. 4. The tilting lines of the respective characters are compensated by the double rounding function.

   There are three kinds of the character sizes; namely, small, medium and large characters as shown in Fig. 5. However, the medium and large characters cannot be displayed other than in the 1st display section.

   There are spaces of 1 dot between the characters.

   The sizes of the bar displays which are structured with 64 vertical slits are as shown in Fig. 5.

3. Display color

   Display in one color among the 8 colors such as transparent, blue, green, cyanic, red, magenta, yellow and white can be set in the 1st to 3rd display sections.

   Display in two colors, that is, one color among the 7 colors such as blue, green, cyanic, red, magenta, yellow and white and either one color of transparent or black can be set in the 4th display section. With these two colors, the bar display of color separation on the left and right sides can be carried out.

4. Display and erasure

   Respective continuous display, a constant time length display, and erasure of display can be set in the 1st to 3rd display sections.

   The display on the 4th display section is controlled by the 3rd display section.

   The display time of the constant time length display is determined by the externally attached CR which is being connected to the $\overline{\text{DADJ}}$ pin. Its time length is about 0.65CR.

   If it is reset with a shorter period of time than the time constant, the display time is lengthened by the retrigger function of the incorporated monostable multivibrator.

   By setting the erasure, the displays on the 2nd to 4th display sections are instantaneously erased, but scroll erasure is carried out only in the 1st display section. The erasure is performed from the lower section by each 1/2 dot at every 2V.

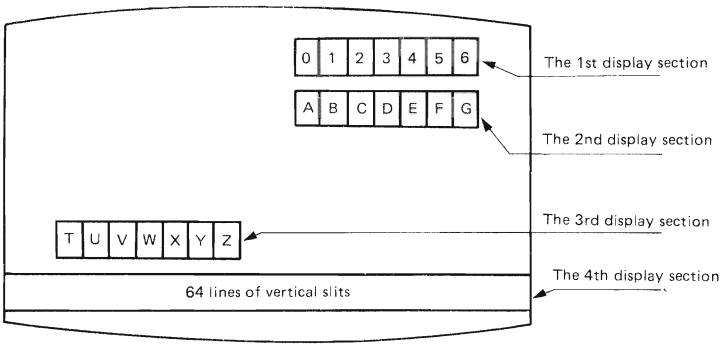
5. Display location adjustment

   Owing to the incorporated horizontal display location setting and vertical display location setting monostable multivibrators, the display location of the horizontal and vertical directions can be adjusted by the externally attached CR which is being connected to the $\overline{\text{HADJ}}$ and $\overline{\text{VADJ}}$ pins.

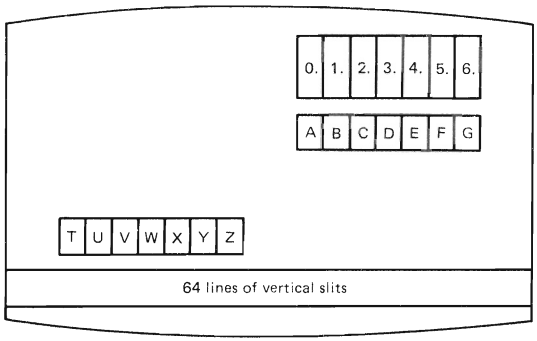
6. Jitter elimination function

   If the range of the jitter of the vertical synchronizing signal is within 12μs, it eliminates the jitter irrespective of the phase of the horizontal synchronizing signal, and thus prevents the character fluctuations of up and down.

(a) When the 1st display section displays with the small size characters


0 1 2 3 4 5 6
A B C D E F G
T U V W X Y Z
The 1st display section
The 2nd display section
The 3rd display section
The 4th display section
64 lines of vertical slits

(b) When the 1st display section displays with the medium size characters



(c) When the 1st display section displays with the large size characters

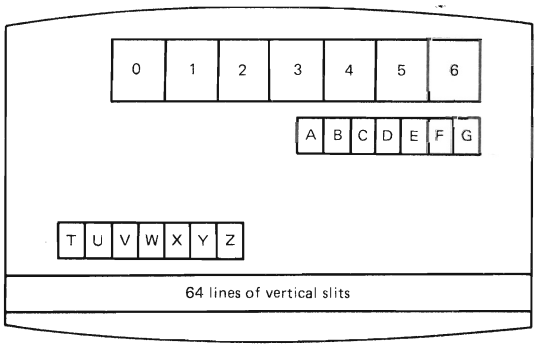
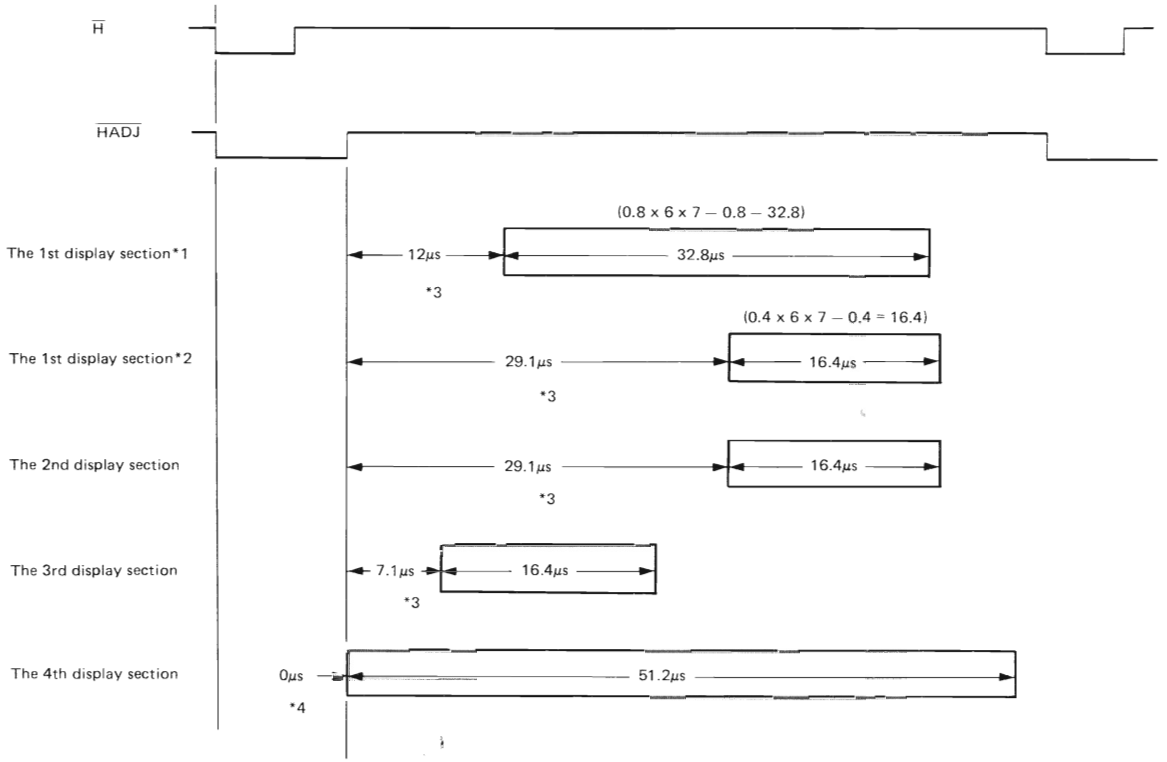


Fig. 1 Screen Structure



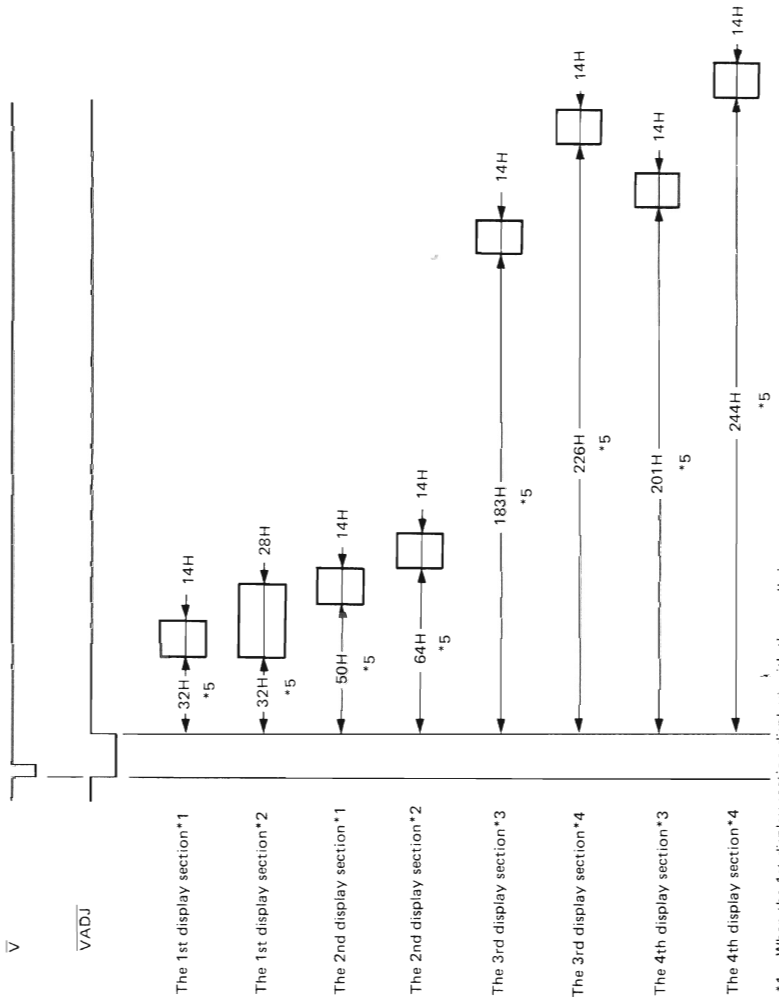
*1 When the 1st display section displays with the large characters

*2 When the 1st display section displays with the small and medium sizes of characters

*3 It becomes about 0.5μs longer due to delay of the oscillation commencement of the 500kHz oscillation circuit

*4 It becomes about 0.1μs longer due to delay of the oscillation commencement of the 5 MHz oscillation circuit

Fig. 2 Horizontal Display Location



*1 When the 1st display section displays with the small size characters

*2 When the 1st display section displays with the medium and large sizes of characters

*3 When it is set to NTSC

*4 When it is set to PAL

*5 It becomes 0.5 to 1H longer due to delay of the jitter elimination circuit.

Fig. 3 Vertical Display Location

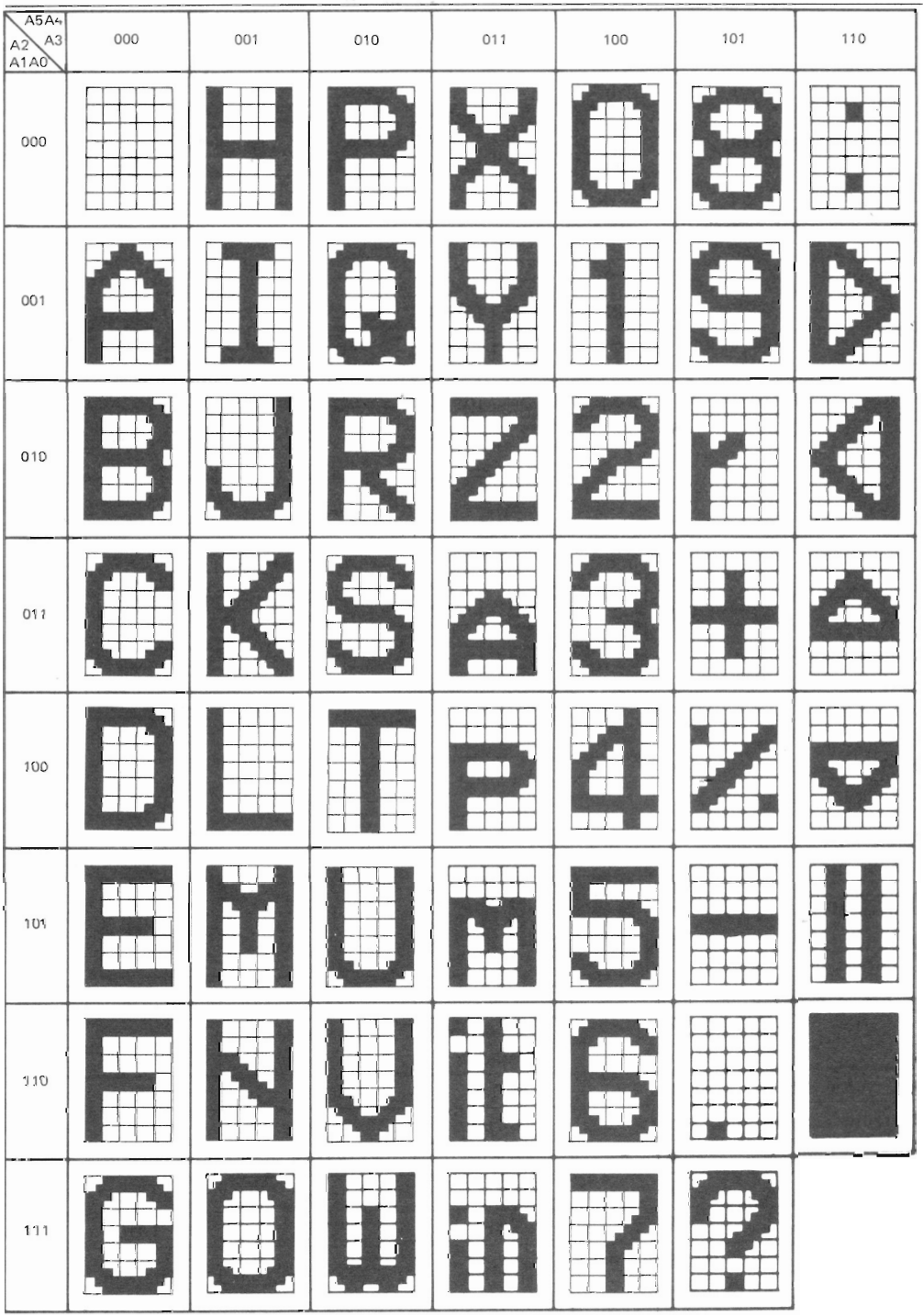
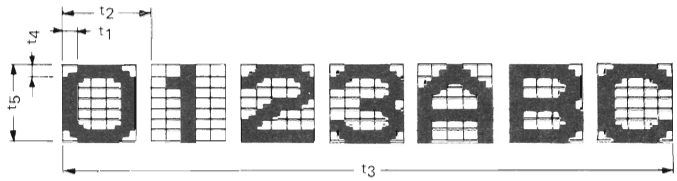
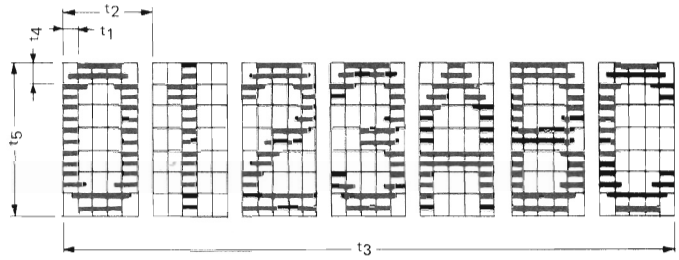


Fig. 4 Character Shapes and Codes

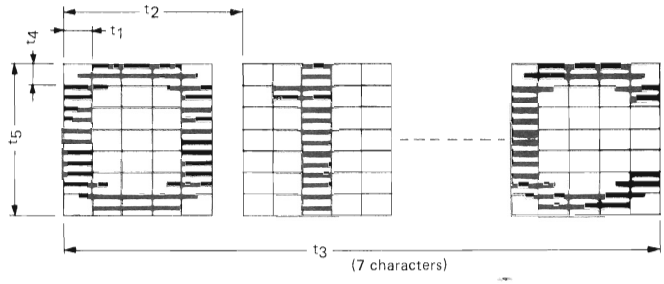
(a) Small characters



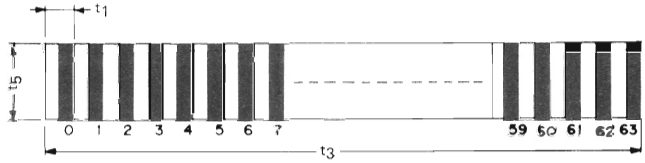
(b) Medium characters



(c) Large characters



(d) Bar display



	(a) Small character	(b) Medium character	(c) Large character	(d) Bar display
t1 (Dot width)	400ns	400ns	800ns	800ns
t2 (Character width)	2.4 μs	2.4 μs	4.8 μs	—
t3 (Block width)	16.4 μs	16.4 μs	32.8 μs	51.2 μs
t4 (Dot height)	2H	4H	4H	—
t5 (Block height)	14H	28H	28H	14H
Display section	The 1st, The 2nd, The 3rd,	The 1st	The 1st	The 4th

Fig. 5 Sizes of the Characters and Bars

Interface Function

The data transfer to CX-7958 from the microcomputer, etc. is carried out by serial transfer using 3 pins; namely, the DATA, $\overline{CLK}$ and $\overline{CS}$ pins.

The data transfer format and an example of the data transfer to the respective display sections are as shown in Figs. 6 and 7 respectively.

1. The data transfer to the 1st to 3rd display sections
   (1) Standard type
   After setting the $\overline{CS}$ pin at "L", input the 8-bit control code and character code of 7 characters × 8 bit from the DATA pin, and simultaneously input the 64-clock signal, which is synchronous with the data, from the $\overline{CLK}$ pin. After completion of the input, set the $\overline{CS}$ pin at "H".
   (2) Simplified type . . . When displaying n ($1 \leqq n \leqq 6$) characters
   After setting the $\overline{CS}$ pin at "L", input the 8-bit control code and the character code of n character × 8 bit from the DATA pin, and simultaneously input the n×8-clock signal, which is synchronous with the data, from the $\overline{CLK}$ pin. After the completion of input, set the $\overline{CS}$ pin at "H".
   When using the 1st and 2nd display sections, the inputted characters (including blanks) are displayed from the right end and when using the 3rd display section, they are displayed from the left end.

2. The data transfer to the 4th display section
   (1) Standard type
   After setting the $\overline{CS}$ pin at "L", input the 8-bit control code, 8-bit color 2 data, 8 bit of number of steps and 5×8 bit of data (Don't Care) from the DATA pin, and simultaneously input 64-clock signal which is synchronous with the data from the $\overline{CLK}$ pin. After completion of the input, set the $\overline{CS}$ pin at "H".
   (2) Simplified type
   After setting the $\overline{CS}$ pin at "L", input the 8-bit control code, 8-bit color 2 data, and 8 bit of number of steps from the DATA pin, and simultaneously input the 24-clock signal, which is synchronous with the data from the $\overline{CLK}$ pin.
   After the completion of the input, set the $\overline{CS}$ pin at "H".

3. Transfer of only the control code
   After setting the $\overline{CS}$ pin at "L", input the 8-bit control code from the DATA pin and simultaneously input the 8-clock signal, which is synchronous with the data, from the $\overline{CLK}$ pin. After the completion of the input, set the $\overline{CS}$ pin at "H". At this point, the part to be set into the control code is only varied and is displayed.
   The character code, color 2 of bar display, and number of steps are not changed.

4. Control code

The control code consists of the following 4 blocks.

(a) ID : Set the data transferring destination (either one among the 1st to 4th display sections)

(b) Display 1: Setting of the contact display/constant time display.

(c) Display 2: Respective setting of display/erasure, small/medium/large characters, NTSC/PAL, and black/transparent.

(d) Color 1 : Color setting of character or the left side of bar display.
When the number of steps in n in the bar display, the left side of the vertical slits of n+1 is set with color 1 and the rest is set with color 2.

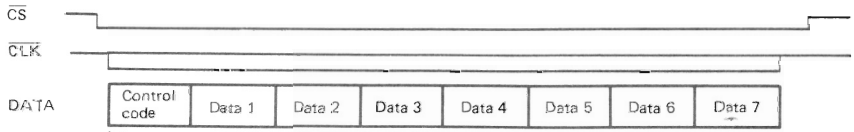
The control code in detail is as shown in Fig. 6.

5. Transfer inhibiting period

The CX-7958 operates having the priority in writing over the other functions and therefore it does not fetch new data until the writing has been completed.

To write the data into the internal RAM, 10H of time is required after the data has been transferred (after ↓ of the $\overline{CS}$). In addition, it holds the writing for the period of 14H of the bar display.

Accordingly, it inhibits the data transfer for 25H after completion of the data transfer. (H: the horizontal scanning period) Moreover, it inhibits rising of the $\overline{CS}$ prior to 25H of the 3rd display section up to the beginning of the 4th display section.



(The respective blocks are structured with 8 bits and transferred from the control code side.)

• **Control Code**

Color 1			Display 1	Display 2		ID	
B	G	R	CR	DP_0	DP_1	ID_0	ID_1
LSB 1		2	3	4	5	6	MSB (Transfers from the LSB side)

	ID_1	0	0	1	1
	ID_0	0	1	0	1
DP_0	DP_1	The 1st display section	The 2nd display section	The 3rd display section	The 4th display section
0	0	Erasure	Erasure	Erasure	Transparent
1	0	Small character	Small character	NTSC Small character	Transparent
0	1	Medium character	Small character	PAL Small character	Black
1	1	Large character	Small character	PAL Small character	Black

Color 1, Color 2			
Color	B	G	R
Black/Transparent	0	0	0
Blue	1	0	0
Green	0	1	0
Cyanic	1	1	0
Red	0	0	1
Magenta	1	0	1
Yellow	0	1	1
White	1	1	1

CR	Display time
0	Continuous
1	Constant time length

The color of RGB=000 is possible to select in black or transparent at the 4th display section.

• **Data 1 to 7**(X denotes "Don't Care", and is transferred from the LSB side.)

In the case of the 1st to 3rd display sections

Data 1 to 7: Character code

In the case of the 4th display sections

Data 1 : Color 2

Data 2 : The number of steps

Data 3 : Don't Care

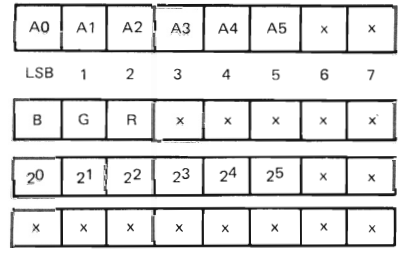


Fig. 6 Data Transfer Format

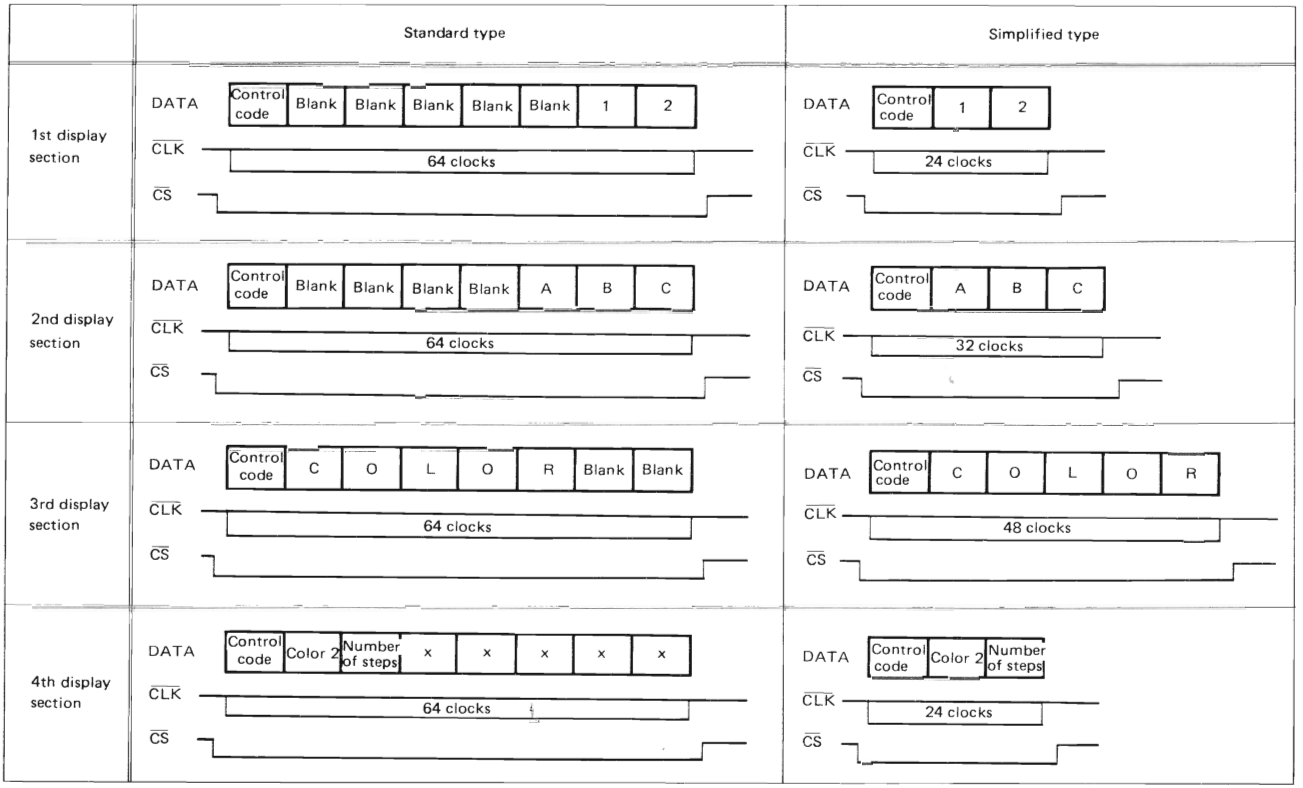
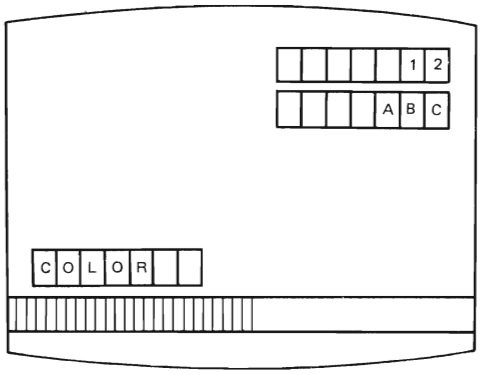


Fig. 7 (a) The Data Transfer

Note 2

	LSB 1	2	3	4	5	6	MSB	
Control code (See the item of control code):	Color 2		Display 1	Display 2		ID		
Character code (Blanks 1, 2, A, B, C, L, O, R, etc. in the figures):	A0	A1	A2	A3	A4	A5	x	x	Note 1
Color 2 (The right side color of the bar display, the left side is color 1):	B	G	R	x	x	x	x	x	Note 1
The number of steps (The vertical slits numbers displayed by color 1):	2^0	2^1	2^2	2^3	2^4	2^5	x	x	Note 1

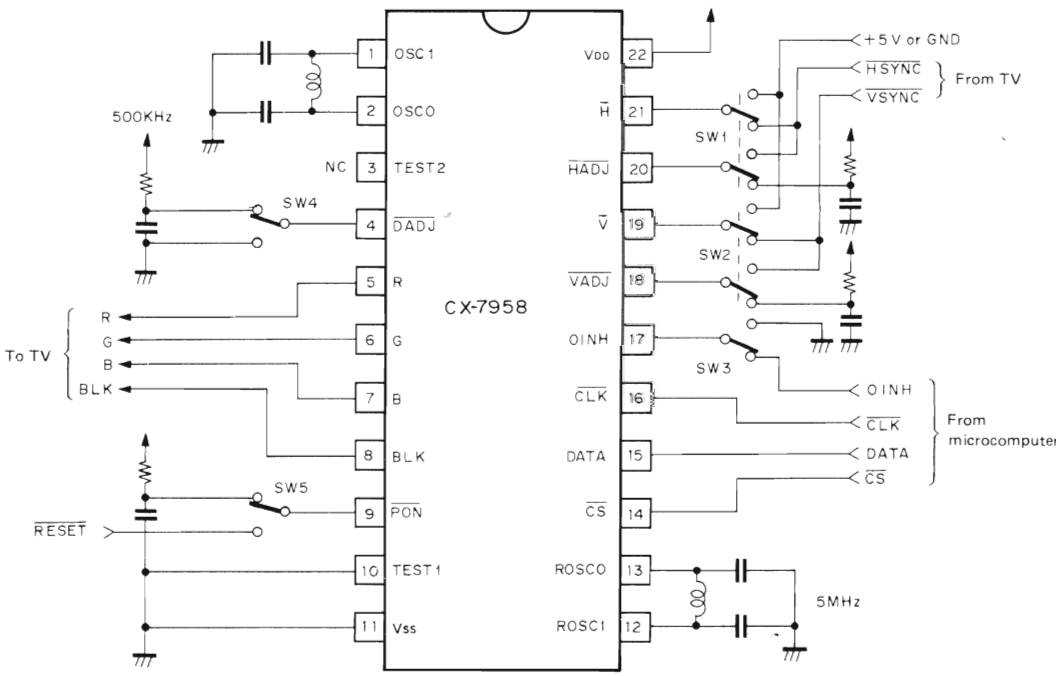
Note) 1. X denotes "Don't Care".
2. Transfer from the LSB side.



The data transfer example, when it is as shown in the left diagram, is indicated by separating into the standard type and simplified type.

Fig. 7 (b) The Data Transfer

Application Circuit



Note 1) Marked with ↑ represents +5V

2) Selection of the SW1 to SW5 should be made in accordance with the using condition.

RGB Interface for CTV

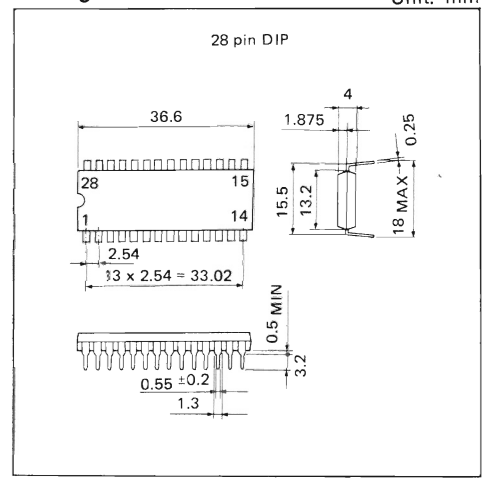
Description

The CX20100 is a bipolar IC which switches and processes signals of 2 systems, and outputs them. It enables to use digital signal by converting it into 0.7 Vp-p signal.

One of the 2 systems input pins is for RGB signal which is obtained by composite signal such as TV signal (Hereafter, it is abbreviated as RGB TV signal.), and the other one is for RGB signal of microcomputer and the like (Hereafter, it is abbreviated as RGB EXT signal.). Three switches; namely, TV/EXT, YM, YS are incorporated within this IC, and in combination with these switches, RGB TV signal only, RGB EXT signal only or RGB TV signal (approximately 6 dB lowered), etc. can be output. As to the standard combinations of these switches, etc. they are based on EIAJ standards.

Package Outline

Unit: mm



Features

- 12V single power source operation
- Based on EIAJ standards
- YS and YM are high-speed switches
- Either positive or negative polarity is applicable to the control voltages of PIX and BRT.

Structure

Bipolar silicon monolithic IC

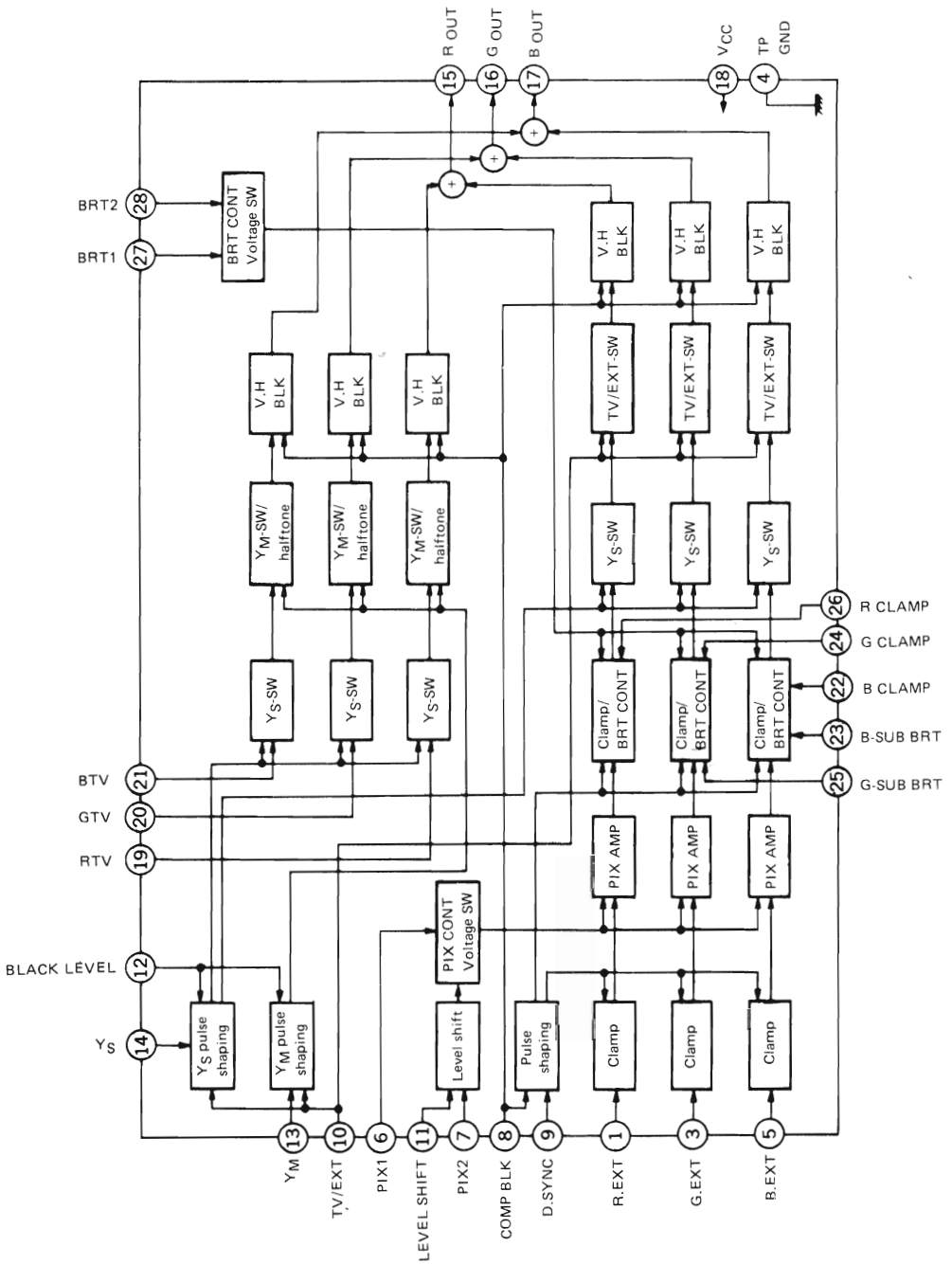
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	17	V
• RGB EXT input pin		0 to 5	V
• Input pins other than the above-mentioned		0 to V_{CC}	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	1160	mW

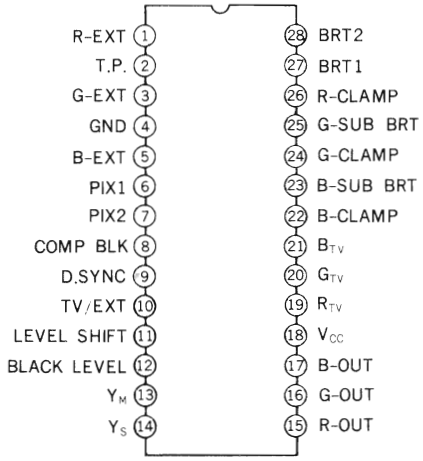
Recommended Operating Condition

• Supply voltage	V_{CC}	12 ± 1	V

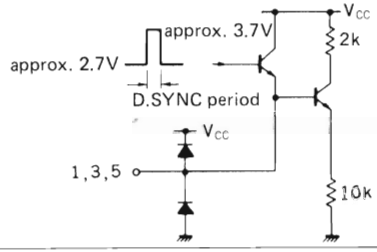
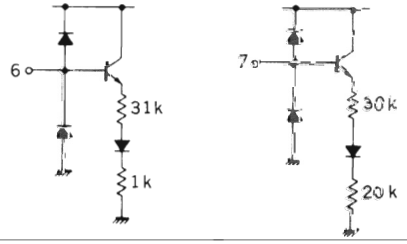
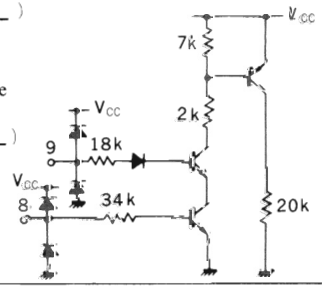
Block Diagram

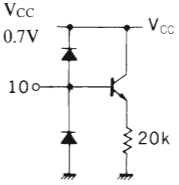
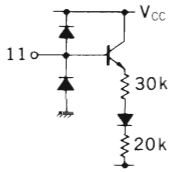
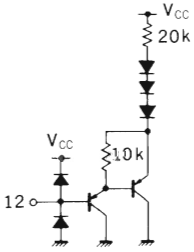
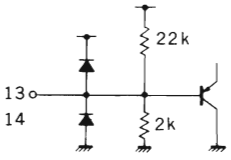


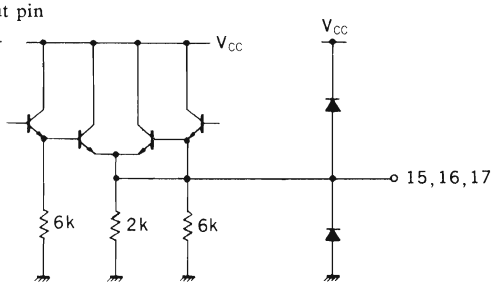
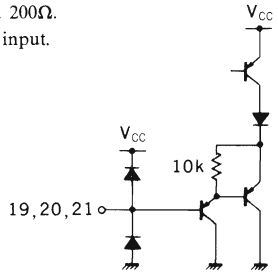
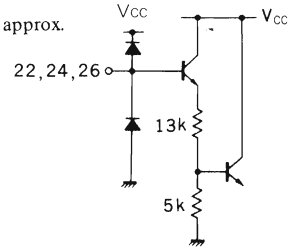
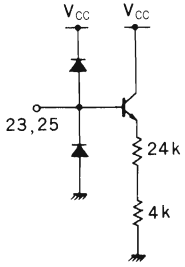
Pin Configuration (Top View)



Pin Description

No.	Symbol	Pin function	DC potential
1 3 5	R-EXT G-EXT B-EXT	① RGB EXT signal input pin ② Input with capacitor cut (approx. 10μ) ③ Input signal level When synchronizing pulse is not existent — less than 0.7 Vp-p When synchronizing pulse is existent — less than 1.0 Vp-p (including SYNC pulse) 	
2	T. P.	Ground the test pin	
4	GND	Ground	
6 7	PIX1 PIX2	① Picture amplifier gain controlling pin ② PIX 1: When voltage increases, gain of the picture amplifier becomes up. PIX 2: When voltage increases, gain of the picture amplifier becomes down. ③ Use either PIX 1 or PIX 2. When PIX 1 is used, connect PIX 2 to GND. When PIX 2 is used, connect PIX 1 to Vcc. 	
8 9	COMP BLK D. SYNC	① COMP BLK blanking pulse input pin Input pulse polarity: Positive (⎍) Low level 0V to 0.4V High level 3V to Vcc ② D. SYNC delayed synchronizing pulse input pin Input pulse polarity: Positive (⎍) Low level 0V to 0.7V High level 3V to Vcc 	

No.	Symbol	Pin function	DC potential
10	TV/EXT	① RGB TV signal and RGB EXT signal changing switch controlling pin (See Table 1 Truth table) ② { Logic 1 3V to V_{CC} Logic 0 0V to 0.7V 	
11	LEVEL SHIFT	① The voltage applied to this pin is superimposed to the voltage applied to pin 7 (PIX 2) and it controls the gain of picture amplifier. (See pins 6 and 7) ② Use only when pin 7 (PIX 2) used. 	
12	BLACK LEVEL	① Black level voltage input pin ② It becomes the reference voltage of black level of Y_M (RGB TV signal is 6 dB lowered). 	
13 14	Y_M Y_S	① { Pin 13: Y_M switch controlling pin Pin 14: Y_S switch controlling pin (See Table 1 Truth table) ② { Logic 1 1.0V to 3.0V Logic 0 0V to 0.4V ③ It drives with the signal source of output impedance 75Ω. 	1.0 V

No.	Symbol	Pin function	DC potential
15 16 17	R-OUT G-OUT B-OUT	① R, G and B output pin ② Receive with buffer. 	
18	V_{CC}	V_{CC}	12 V
19 20 21	R_{TV} G_{TV} B_{TV}	① RGB TV signal input pin ② Input a signal via resistance of approx. 200Ω. ③ Connect it to GND when no signal is input. 	
22 24 26	B-CLAMP G-CLAMP R-CLAMP	① RGB clamp filter pin ② Connect to ground with a capacitor of approx. 0.22 to 0.47μ. 	
23 25	B-SUB BRT G-SUB BRT	① G and B sub-bright controlling pin ② Use this pin with BRT 1 or BRT 2 to adjust the pedestal level. 	

No.	Symbol	Pin function	DC potential
27	BRT_1	① Bright control pins 1 and 2 ② { BRT_1: When the voltage increases, the pedestal level becomes up. BRT_2: When the voltage increases. the pedestal level becomes down. ③ Use either BRT_1 or BRT_2. { When BRT_1 is used, connect BRT_2 to GND. When BRT_2 is used, connect BRT_1 to V_{CC}.	
28	BRT_2		

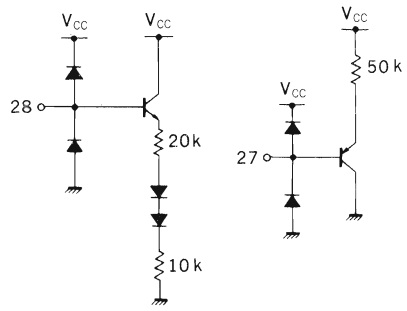


Table 1 Truth Table

TV/EXT	1	0		
Y_M	X	0	1	X
Y_S	X	0	0	1
Input pin / Output mode	TV	TV	RGB TV signal 6 dB down	EXT

Electrical Characteristics (Ta=25°)

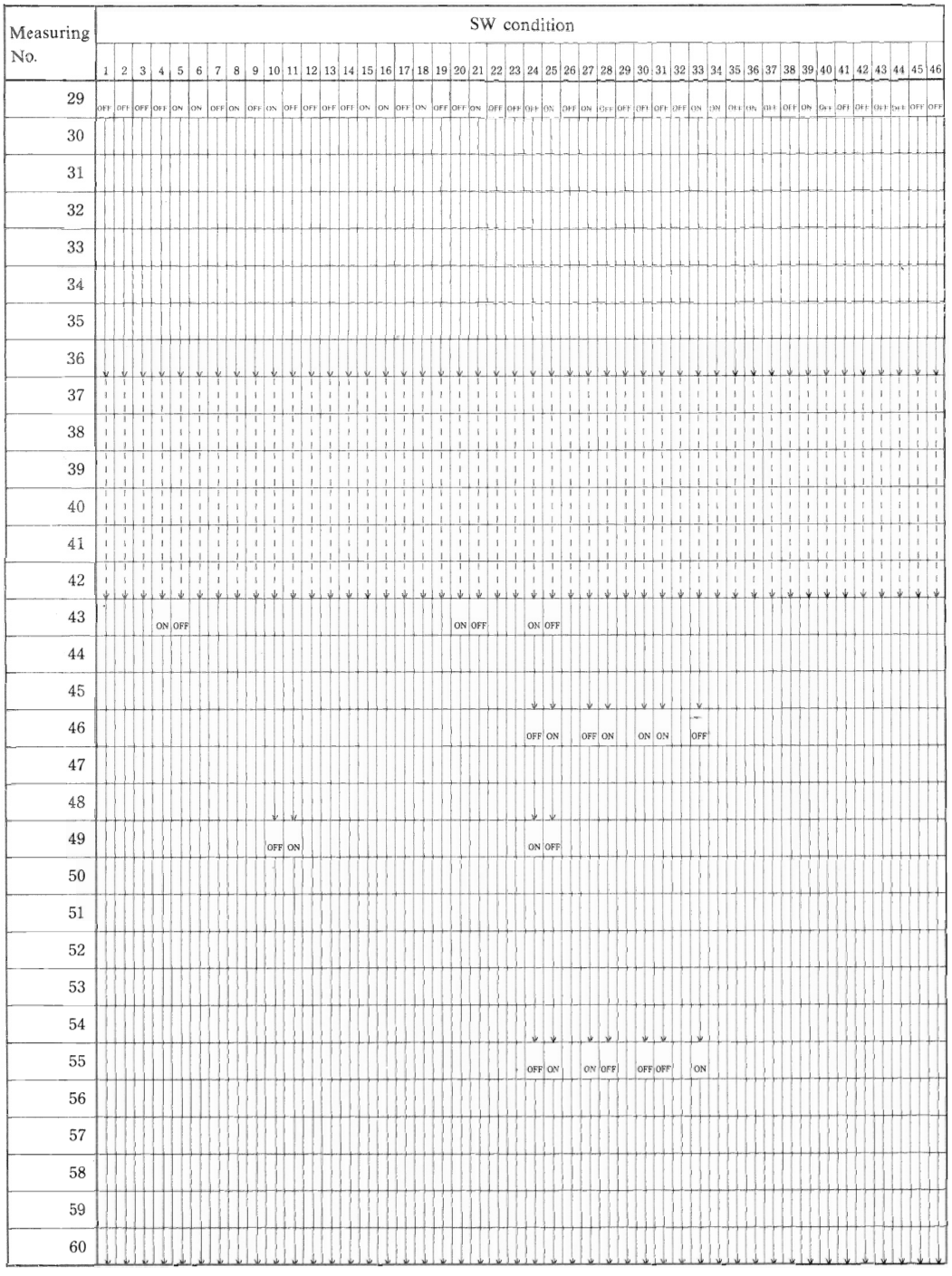
Measuring No.	Measuring item	Symbol	Bias applying point and voltage E_1	E_2	E_3	E_4	E_5	*	Output waveform and description of measuring method	Min.	Typ.	Max.	Unit
1	Current value	I_1	㉚ 3V	㊳ 1.5V	㊺ 6V	㊶ 1V	⑱ 12V	⑱		42	61	78	mA
2	〃	I_2	㉚㉟ 3V					⑱		42	61	78	mA
3	EXT output voltage	R_E	㉚ 3V					㉓	DC measurement (Unit: mV)	3.19	3.5	4.62	V
4		G_E						⑯		3.19	3.5	4.62	V
5		B_E						⑰		3.19	3.5	4.62	V
6	TV output voltage	$R_{TV'MAX}$						⑮		5.69	5.9	6.11	V
7	(MIX mode)	$G_{TV'MAX}$						⑯		5.69	5.9	6.11	V
8		$B_{TV'MAX}$						⑰		5.69	5.9	6.11	V
9	TV output voltage (V_{CC}=13V)	$R_{TV'MAX1}$					⑱ 13V	⑮		5.69	5.9	6.11	V
10	TV output voltage (V_{CC}=11V)	$R_{TV'MAX2}$					⑱ 11V	⑮		5.69	5.9	6.11	V
11	TV output voltage	$R_{TV\ MAX}$	㉚㉟ 3V			㊶ 1V	⑱ 12V	⑮		5.69	5.9	6.11	V
12		$G_{TV\ MAX}$						⑯		5.69	5.9	6.11	V
13		$B_{TV\ MAX}$						⑰		5.69	5.9	6.11	V
14		$R_{TV\ MIN}$		㊳㊻ 1.5V				⑮		1.3	1.5	1.7	V
15		$G_{TV\ MIN}$						⑯		1.3	1.5	1.7	V
16		$B_{TV\ MIN}$						⑰		1.3	1.5	1.7	V
17	EXT output voltage correlation	ΔV_E							$\Delta V_E = G_E - R_E$	−310	0	310	mV
18									$\Delta V_E = B_E - R_E$	−310	0	310	mV
19									$\Delta V_E = B_E - G_E$	−310	0	310	mV
20	TV output voltage correlation	$\Delta V_{TV'MAX}$							$\Delta V_{TV'MAX} = G_{TV'MAX} - R_{TV'MAX}$	−52	0	52	mV
21									$\Delta V_{TV'MAX} = B_{TV'MAX} - R_{TV'MAX}$	−52	0	52	mV
22									$\Delta V_{TV'MAX} = B_{TV'MAX} - G_{TV'MAX}$	−52	0	52	mV
23	TV output voltage correlation	$\Delta V_{TV\ MAX}$							$\Delta V_{TV\ MAX} = G_{TV\ MAX} - R_{TV\ MAX}$	−52	0	52	mV
24									$\Delta V_{TV\ MAX} = B_{TV\ MAX} - R_{TV\ MAX}$	−52	0	52	mV
25									$\Delta V_{TV\ MAX} = B_{TV\ MAX} - G_{TV\ MAX}$	−52	0	52	mV
26		$\Delta V_{TV\ MIN}$							$\Delta V_{TV\ MIN} = G_{TV\ MIN} - R_{TV\ MIN}$	−52	0	52	mV
27									$\Delta V_{TV\ MIN} = B_{TV\ MIN} - R_{TV\ MIN}$	−52	0	52	mV
28									$\Delta V_{TV\ MIN} = B_{TV\ MIN} - G_{TV\ MIN}$	−52	0	52	mV

* Measuring point

| Measuring No. | SW condition | | |

Measuring No.	Measuring item	Symbol	Bias applying point and voltage E_1	E_2	E_3	E_4	E_5	*	Output waveform and description of measuring method	Min.	Typ.	Max.	Unit
29	Y_M output voltage	$R_{YM\ MIN}$				㊴ 1V		⑮	DC measurement (Unit: mV order)	1.38	1.45	1.52	V
30		$G_{YM\ MIN}$						⑯		1.38	1.45	1.52	V
31		$B_{YM\ MIN}$						⑰		1.38	1.45	1.52	V
32		$R_{YM\ MAX}$		㊳ 1.5V	㊻ 6V			⑮		3.35	3.7	4.05	V
33		$G_{YM\ MAX}$						⑯		3.35	3.7	4.05	V
34		$B_{YM\ MAX}$						⑰		3.35	3.7	4.05	V
35	Y_M output voltage (Vcc=13V)	$R_{YM\ MAX1}$					⑱ 13V	⑮		3.35	3.7	4.05	V
36	Y_M output voltage (Vcc=10V)	$R_{YM\ MAX2}$					⑱ 11V	⑮		3.35	3.7	4.05	V
37	Y_M output voltage correlation	$\Delta Y_{M\ MIN}$							$\Delta Y_{M\ MIN} = G_{YM\ MIN} - R_{YM\ MIN}$	−51.5	0	51.5	mV
38									$\Delta Y_{M\ MIN} = B_{YM\ MIN} - R_{YM\ MIN}$	−51.5	0	51.5	mV
39									$\Delta Y_{M\ MIN} = B_{YM\ MIN} - G_{YM\ MIN}$	−51.5	0	51.5	mV
40		$\Delta Y_{M\ MAX}$							$\Delta Y_{M\ MAX} = G_{YM\ MIN} - R_{YM\ MIN}$	−51.5	0	51.5	mV
41									$\Delta Y_{M\ MAX} = B_{YM\ MAX} - R_{YM\ MAX}$	−51.5	0	51.5	mV
42									$\Delta Y_{M\ MAX} = B_{YM\ MAX} - G_{YM\ MAX}$	−51.5	0	51.5	mV
43	Ys output voltage (EXT side)	R_{YSE}	㉚ 3V			㊶ 1V	⑱ 12V	⑮	DC measurement (Unit: mV order)	0.75	0.95	1.15	V
44		G_{YSE}						⑯		0.75	0.95	1.15	V
45		B_{YSE}						⑰		0.75	0.95	1.15	V
46	Ys output voltage (TV side)	R_{YST}						⑮	DC measurement (Unit: mV order)	0.75	0.95	1.15	V
47		G_{YST}						⑯		0.75	0.95	1.15	V
48		B_{YST}						⑰		0.75	0.95	1.15	V
49	BLK threshold (Low side EXT)	R_{BLE}			㊶ 1V	㊳ 0.4V		⑮		3.0	3.6	4.7	V
50		G_{BLE}						⑯		3.0	3.6	4.7	V
51		B_{BLE}						⑰		3.0	3.6	4.7	V
52	BLK threshold (High side EXT)	R_{BHE}	㉚㉝ 3V					⑮				0.525	V
53		G_{BHE}						⑯				0.525	V
54		B_{BHE}						⑰				0.525	V
55	BLK threshold (High side TV)	R_{BHT}			㊻ 6V			⑮				0.525	V
56		G_{BHT}						⑯				0.525	V
57		B_{BHT}						⑰				0.525	V
58	BLK threshold (Low side TV)	R_{BLT}	㉚ 3V			㉝ 0.4V		⑮		5.4	5.9	6.4	V
59		G_{BLT}						⑯		5.4	5.9	6.4	V
60		B_{BLT}						⑰		5.4	5.9	6.4	V

* Measuring point


Measuring No.
SW condition
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46
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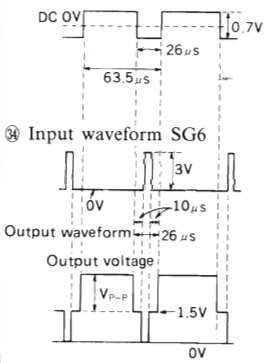
ON OFF
ON OFF
ON OFF
OFF ON
OFF ON
ON ON
OFF
OFF ON
ON OFF
OFF ON
ON OFF
OFF OFF
ON

Measuring No.	Measuring item	Symbol	Bias applying point and voltage E_1	E_2	E_3	E_4	E_5	*	Output waveform and description of measuring method	Min.	Typ.	Max.	Unit
61	TV/EXT threshold (Low side)	R_{SL}				㊱ 0.7V		⑮	Bias condition →E_6 ㊶ 1V	3.0	3.85	4.7	V
62		G_{SL}						⑯		3.0	3.85	4.7	V
63		B_{SL}						⑰		3.0	3.85	4.7	V
64	Ys threshold (Low side)	R_{YSL}				㊶ 0.4V		⑮		5.4	5.9	6.4	V
65		G_{YSL}						⑯		5.4	5.9	6.4	V
66		B_{YSL}						⑰		5.4	5.9	6.4	V
67	YM threshold (Low side)	R_{YML}				㊴ 0.4V		⑮		5.4	5.9	6.4	V
68		G_{YML}						⑯		5.4	5.9	6.4	V
69		B_{YML}						⑰		5.4	5.9	6.4	V
70	D. SYNC threshold	R_{DL}	㉝ 3V			㉟ 0.7V		①	DC measurement (Unit: mV order)	1.8	2.1	2.3	V
71		G_{DL}						③		1.8	2.1	2.3	V
72		B_{DL}						⑤		1.8	2.1	2.3	V
73		R_{DH}	㉝㉟ 3V					①		2.55	3.0	3.25	V
74		G_{DH}						③		2.55	3.0	3.25	V
75		B_{DH}						⑤		2.55	3.0	3.25	V
76	P_{IX} AMP GAIN (MAX)	R_{PMAX}	㊾ 58V		㊶ 1V			⑮	㉙ Input waveform SG1	2.25	2.9	3.45	V_{P-P}
77		$G_{P\ MAX}$						⑯		2.25	2.9	3.45	V_{P-P}
78		$B_{P\ MAX}$						⑰		2.25	2.9	3.45	V_{P-P}
79	P_{IX} AMP GAIN (MAX V_{CC}=13V)	$R_{P\ MAX1}$					⑱ 13V	⑮		2.25	2.9	3.45	V_{P-P}
80	P_{IX} AMP GAIN (MAX V_{CC}=11V)	$R_{P\ MAX2}$					⑱ 11V	⑮	㉞ Input waveform SG6	2.25	2.9	3.45	V_{P-P}
81	P_{IX1} AMP GAIN (CENT)	R_{P1CENT}				㉛ 6V	⑱ 12V	⑮		0.9	1.15	1.40	V_{P-P}
82		G_{P1CENT}						⑯		0.9	1.15	1.40	V_{P-P}
83		B_{P1CENT}						⑰		0.9	1.15	1.40	V_{P-P}
84	P_{IX1} AMP GAIN (MIN)	$R_{P1\ MIN}$				㉛ 0V		⑮		0.34	0.37	0.48	V_{P-P}
85		$G_{P1\ MIN}$						⑯		0.34	0.37	0.48	V_{P-P}
86		$B_{P1\ MIN}$						⑰		0.34	0.37	0.48	V_{P-P}
87	P_{IX2} AMP GAIN (CENT)	R_{P2CENT}				㉜ 3V		⑮		1.24	1.45	1.66	V_{P-P}
88		$G_{P2\ CENT}$						⑯		1.24	1.45	1.66	V_{P-P}
89		B_{P2CENT}						⑰		1.24	1.45	1.66	V_{P-P}
90	P_{IX2} AMP GAIN (MIN)	$R_{P2\ MIN}$				㉜ 6V		⑮		0.43	0.5	0.61	V_{P-P}
91		$G_{P2\ MIN}$						⑯		0.43	0.5	0.61	V_{P-P}
92		$B_{P2\ MIN}$						⑰		0.43	0.5	0.61	V_{P-P}



(Measuring items: 76 ~ 95)
Measuring unit: 10 mV order

* Measuring point

| Measuring No. | SW condition | | |

Measuring No.	Measuring item	Symbol	Bias applying point and voltage E_1	E_2	E_3	E_4	E_5	*	Output waveform and description of measuring method	Min.	Typ.	Max.	Unit
93	Level shift	R_L				㉜㉛ 3V		⑮		0.66	0.8	0.94	V_{P-P}
94		G_L						⑯		0.66	0.8	0.94	V_{P-P}
95		B_L						⑰		0.66	0.8	0.94	V_{P-P}
96	PIX AMP GAIN correlation	ΔP_{MAX}							$\Delta P_{MAX}=G_{PMAX}/R_{PMAX}$	0.85	1.0	1.15	
97									$\Delta P_{MAX}=B_{PMAX}/R_{PMAX}$	0.85	1.0	1.15	
98									$\Delta P_{MAX}=B_{PMAX}/G_{PMAX}$	0.85	1.0	1.15	
99	PIX 1 AMP GAIN correlation (CENT)	ΔP_{1CENT}							$\Delta P_{1CENT}=G_{P1CENT}/R_{P1CENT}$	0.85	1.0	1.15	
100									$\Delta P_{1CENT}=B_{P1CENT}/R_{P1CENT}$	0.85	1.0	1.15	
101									$\Delta P_{1CENT}=B_{P1CENT}/G_{P1CENT}$	0.85	1.0	1.15	
102	PIX 1 AMP GAIN correlation (MIN)	ΔP_{1MIN}							$\Delta P_{1MIN}=G_{P1MIN}/R_{P1MIN}$	0.85	1.0	1.15	
103									$\Delta P_{1MIN}=B_{P1MIN}/R_{P1MIN}$	0.85	1.0	1.15	
104									$\Delta P_{1MIN}=B_{P1MIN}/G_{P1MIN}$	0.85	1.0	1.15	
105	PIX 2 AMP GAIN correlation (CENT)	ΔP_{2CENT}							$\Delta P_{2CENT}=G_{P2CENT}/R_{P2CENT}$	0.85	1.0	1.15	
106									$\Delta P_{2CENT}=B_{P2CENT}/R_{P2CENT}$	0.85	1.0	1.15	
107									$\Delta P_{2CENT}=B_{P2CENT}/G_{P2CENT}$	0.85	1.0	1.15	
108	PIX 2 AMP GAIN correlation (MIN)	ΔP_{2MIN}							$\Delta P_{2MIN}=G_{P2MIN}/R_{P2MIN}$	0.85	1.0	1.15	
109									$\Delta P_{2MIN}=B_{P2MIN}/R_{P2MIN}$	0.85	1.0	1.15	
110									$\Delta P_{2MIN}=B_{P2MIN}/G_{P2MIN}$	0.85	1.0	1.15	
111	Level shift correlation	ΔL							$\Delta L=G_L/R_L$	0.85	1.0	1.15	
112									$\Delta L=B_L/R_L$	0.85	1.0	1.15	
113									$\Delta L=B_L/G_L$	0.85	1.0	1.15	
114	Black level	R_{PD}						⑮	Input signal Output waveform (items 114 ~122) ㉙ SG1 ㉞ SG6 approx. 2.9V 0V Output voltage Measuring unit: mV order	1.2	1.55	1.9	V
115		G_{PD}						⑯		1.2	1.55	1.9	V
116		B_{PD}						⑰		1.2	1.55	1.9	V
117	Black level potential difference during PIX controlling (PIX CENT)	$R_{PD(PIX\ CENT)}$				㉛ 6V		⑮	$R_{PD(PIX\ CENT)}-R_{PD}$	−105	0	105	mV
118		$G_{PD(PIX\ CENT)}$						⑯	$G_{PD(PIX\ CENT)}-G_{PD}$	−105	0	105	mV
119		$B_{PD(PIX\ CENT)}$						⑰	$B_{PD(PIX\ CENT)}-B_{PD}$	−105	0	105	mV
120	Black level potential difference during PIX controlling (PIX MIN)	$R_{PD(PIX\ MIN)}$				㉛ 0V		⑮	$R_{PD(PIX\ MIN)}-R_{PD}$	−158	0	158	mV
121		$G_{PD(PIX\ MIN)}$						⑯	$G_{PD(PIX\ MIN)}-G_{PD}$	−158	0	158	mV
122		$B_{PD(PIX\ MIN)}$						⑰	$B_{PD(PIX\ MIN)}-B_{PD}$	−158	0	158	mV

* Measuring point

| Measuring No. | SW condition | | |

Measuring No.	Measuring item	Symbol	Bias applying point and voltage E_1	E_2	E_3	E_4	E_5	*	Output waveform and description of measuring method	Min.	Typ.	Max.	Unit
123	Black level potential difference correlation (PIX MAX)	ΔP_D							$\Delta P_D = G_{PD} - R_{PD}$	−158	0	158	mV
124									$\Delta P_D = B_{PD} - R_{PD}$	−158	0	158	mV
125									$\Delta P_D = B_{PD} - G_{PD}$	−158	0	158	mV
126	Black level potential difference correlation	$\Delta P_{D(PIX\ CENT)}$							$\Delta P_{D(PIX\ CENT)} = G_{PD(PIX\ CENT)} - R_{PD(PIX\ CENT)} - \{G_{PD} - R_{PD}\}$	−105	0	105	mV
127									$\Delta P_{D(PIX\ CENT)} = B_{PD(PIX\ CENT)} - R_{PD(PIX\ CENT)} - \{B_{PD} - R_{PD}\}$	−105	0	105	mV
128									$\Delta P_{D(PIX\ CENT)} = B_{PD(PIX\ CENT)} - G_{PD(PIX\ CENT)} - \{B_{PD} - G_{PD}\}$	−105	0	105	mV
129	Black level potential difference correlation	$\Delta P_{D(PIX\ MIN)}$							$\Delta P_{D(PIX\ MIN)} = G_{PD(PIX\ MIN)} - R_{PD(PIX\ MIN)} - \{G_{PD} - R_{PD}\}$	−105	0	105	mV
130									$\Delta P_{D(PIX\ MIN)} = B_{PD(PIX\ MIN)} - R_{PD(PIX\ MIN)} - \{B_{PD} - R_{PD}\}$	−105	0	105	mV
131									$\Delta P_{D(PIX\ MIN)} = B_{PD(PIX\ MIN)} - G_{PD(PIX\ MIN)} - \{B_{PD} - G_{PD}\}$	−105	0	105	mV
132	BRT 1 control (MAX)	$R_{PD(MAX)}$	㊾ 7.8V	㊳ 3.5V				⑮	Input signal ㊷ SG1 ㉞ SG6	2.85	3.6	4.35	V
133		$G_{PD1(MAX)}$						⑯	Output waveform	2.85	3.6	4.35	V
134		$B_{PD1(MAX)}$						⑰	approx. 2.9 Vp-p, 0V, Output voltage	2.85	3.6	4.35	V
135	BRT 2 control (BRT MIN)	$R_{PD2(MIN)}$	㊿ 6.6V	㊳ 1.5V				⑮		0.74	1.2	1.66	V
136		$G_{PD(MIN)}$						⑯	Measuring items (132 to 140)	0.74	1.2	1.66	V
137		$B_{PD(MIN)}$						⑰	Measuring unit: mV order	0.74	1.2	1.66	V
138	BRT 2 control (BRT MAX)	$R_{PD2(MAX)}$	㊿ 4.3V	㊳ 3.5V				⑮		2.84	3.35	3.86	V
139		$G_{PD(MAX)}$						⑯		2.84	3.35	3.86	V
140		$B_{PD(MAX)}$						⑰		2.84	3.35	3.86	V
141	BRT 1 control correlation (MAX)	$\Delta P_{D1(MAX)}$							$\Delta P_{D1(MAX)} = G_{PD1(MAX)} - R_{PD2(MAX)} - \{G_{PD} - R_{PD}\}$	−155	0	55	mV
142		$\Delta P_{D2(MAX)}$							$\Delta P_{D1(MAX)} = B_{PD1(MAX)} - R_{PD1(MAX)} - \{B_{PD} - R_{PD}\}$	−155	0	55	mV
143									$\Delta P_{D1(MAX)} = B_{PD1(MAX)} - G_{PD1(MAX)} - \{B_{PD} - G_{PD}\}$	−105	0	105	mV
144	BRT 2 control correlation (MIN)	$\Delta P_{D2(MIN)}$							$\Delta P_{D2(MIN)} = G_{PD2(MIN)} - R_{PD2(MIN)}$	−165	0	165	mV
145									$\Delta P_{D2(MIN)} = B_{PD2(MIN)} - R_{PD2(MIN)}$	−165	0	165	mV
146									$\Delta P_{D2(MIN)} = B_{PD2(MIN)} - G_{PD2(MIN)}$	−165	0	165	mV
147	BRT 2 control correlation (MAX)	$\Delta P_{P2(MAX)}$							$\Delta P_{D2(MAX)} = G_{PD2(MAX)} - R_{PD2(MAX)} - \{G_{PD2(MIN)} - R_{PD2(MIN)}\}$	−105	0	55	mV
148									$\Delta P_{D2(MAX)} = B_{PD2(MAX)} - R_{PD2(MAX)} - \{B_{PD2(MIN)} - R_{PD2(MIN)}\}$	−105	0	55	mV
149									$\Delta P_{D2(MAX)} = B_{PD2(MAX)} - G_{PD2(MAX)} - \{B_{PD2(MIN)} - G_{PD2(MIN)}\}$	−105	0	105	mV

* Measuring point

| Measuring No. | SW condition | | |

Measuring No.	Measuring item	Symbol	Bias applying point and voltage E_1	E_2	E_3	E_4	E_5	*	Output waveform and description of measuring method	Min.	Typ.	Max.	Unit
150	SUB BRT control (MAX)	$R_{PDS(MAX)}$	⑩ 6V	⑧ 1.5V		⑧ 8V		⑮	Input signal ㉙ SG1 ㉞ SG6	1.4	1.9	2.4	V
151		$G_{PDS(MAX)}$						⑯	Output waveform is the same as items 132 to 140. (But the output voltage is different.) Measuring unit: mV order	1.9	2.45	3.0	V
152		$B_{PDS(MAX)}$						⑰		1.9	2.45	3.0	V
153	SUB BRT control (MIN)	$R_{PDS(MIN)}$					⑱⑱ 12V	⑮		1.5	2.0	2.4	V
154		$G_{PDS(MIN)}$						⑯		0.65	1.2	1.55	V
155		$B_{PDS(MIN)}$						⑰		0.65	1.2	1.55	V
156	SUB BRT control	$\Delta P_{DS(MAX)}$							$\Delta P_{DS(MAX)} = B_{PDS(MAX)} - G_{PDS(MAX)}$	−63	0	63	mV
157	correlation	$\Delta P_{DS(MIN)}$							$\Delta P_{DS(MIN)} = B_{PDS(MIN)} - G_{PDS(MIN)} - [B_{PDS(MAX)} - G_{PDS(MAX)}]$	−63	0	63	mV
158	During SUB BRT controlling, Rch black level varies	ΔR_{PDS}							$\Delta R_{PDS} = R_{PDS(MAX)} - R_{PDS(MIN)}$	−52.5	0	52.5	mV
159	EXT MAX output	R_M	⑤ 4.3V	③ 3.5V				⑮	Input waveform ㉞ SG6 ㉙ SG2 SG2 waveform DC0V 5V 0V 28μ 63.5μ Output waveform Output voltage	6.0			V
160		G_M						⑯		6.0			V
161		B_M						⑰		6.0			V
162	DG	D_R						⑮	Input signal ㉙ SG3 ㉞ SG6 Regarding input waveform measuring, see p.23.			21	%
163		D_G						⑯				21	%
164								⑰				21	%
165	Y_M pulse response	$T_{DR}Y_MR$	⑳ 3V	⑧ 1.5V		⑯ 6V		㊷	㊵ Input waveform SG7 100ns 3V 0V Output waveform 100ns $T_{DR}Y_M$ $T_{DF}Y_M$ (5.8V) 0V (3.7V) 2.2V A word in the parentheses means the voltage in the event of without C cut.	0	20	42	ns
166		$T_{DF}Y_MR$						㊷		0	20	42	ns
167		$T_{DR}Y_MG$						㊸		0	20	42	ns
168		$T_{DF}Y_MG$						㊸		0	20	42	ns
169		$T_{DR}Y_MB$						㊹		0	20	42	ns
170		$T_{DF}Y_MB$						㊹		0	20	42	ns
171	Y_S pulse response (TV side)	$T_{DR}Y_SR$						㊷	㊵ Input waveform SG7 100ns 3V 0V Output waveform 100ns $T_{DR}Y_S$ $T_{DF}Y_S$ (5V) DC 0V (0.9V) A word in the parentheses means the voltage in the event of without C cut.	0	20	42	ns
172		$T_{DF}Y_SR$						㊷		0	20	42	ns
173		$T_{DR}Y_SG$						㊸		0	20	42	ns
174		$T_{DF}Y_SG$						㊸		0	20	42	ns
175		$T_{DR}Y_SB$						㊹		0	20	42	ns
176		$T_{DF}Y_SB$						㊹		0	20	42	ns

* Measuring point

| Measuring No. | SW condition | | |

Measuring No.	Measuring item	Symbol	Bias applying point and voltage E_1	E_2	E_3	E_4	E_5	*	Output waveform and description of measuring method	Min.	Typ.	Max.	Unit
177	Ys pulse response (EXT side)	$T_{DR}Y_SER$						㊷	㊵ Input waveform SG7 100ns, 3V, 0V, 100ns Output waveform $T_{DR}Y_SE$ — $T_{DF}Y_SE$ (3.6V), 0V, (0.9V) A word in the parentheses means the voltage in the event of without C cut.	0	20	42	ns
178		$T_{DF}Y_SER$						㊷		0	20	42	ns
179		$T_{DR}Y_SEG$						㊸		0	20	42	ns
180		$T_{DF}Y_SEG$						㊸		0	20	42	ns
181		$T_{DR}Y_SEB$						㊹		0	20	42	ns
182		$T_{DF}Y_SEB$						㊹		0	20	42	ns
183	F characteristics	F_R			㊶ 1V			⑮	㉙ Input waveform SG4 14.3MHz 0.7V_{P-P} Output waveform 2.5V_{P-P}, 3.6V	1.6			V_{P-P}
184		F_G						⑯		1.6			V_{P-P}
185		F_B						⑰		1.6			V_{P-P}
186	Crosstalk (between EXTs)	CT1R						⑮	㉙ Input waveform SG5 3.58MHz 0.5V_{P-P} Obtain 20log(CT1R/CT1G) and 20log(CT1B/CT1G) by measuring the outputs of individual channels with RMS meter.		reference level	−39	dB
187		CT1G						⑯				2.1V_{P-P}	
188		CT1B			↓			⑰				−39	dB
189	Crosstalk (EXT→TV)	CT2R				㊻ 6V		⑮	㉙ Input SG5 3.58MHz 0.5V_{P-P} Obtain 20log(CT2R/CT1G), 20log (CT2G/CT1G), 20log(CT2B/CT1G), 20log(CT3R/CT1G), 20log(CT3G/CT1G) and 20log(CT3B/CT1G) by measuring the outputs of individual channels with RMS meter.			−49	dB
190		CT2G						⑯				−49	dB
191		CT2B						⑰				−49	dB
192	Crosstalk (EXT→TV)	CT3R						⑮				−49	dB
193		CT3G						⑯				−49	dB
194		CT3B				↓		⑰				−49	dB
195	Crosstalk (TV→EXT)	CT4R			㊶ 1V	㊼ 6V		⑮	㊺ Input waveform SG8 3.58MHz 2V_{P-P} Obtain 20log(CT4R/0.707), 20log (CT4G/0.707) and 20log(CT4B/0.707) by measuring the outputs of individual channels with RMS meter.			−44	dB
196		CT4G						⑯				−44	dB
197		CT4B	↓	↓	↓	↓	↓	⑰				−44	dB

* Measuring point

| Measuring No. | SW condition | | |

Electrical Characteristics Measuring Circuit

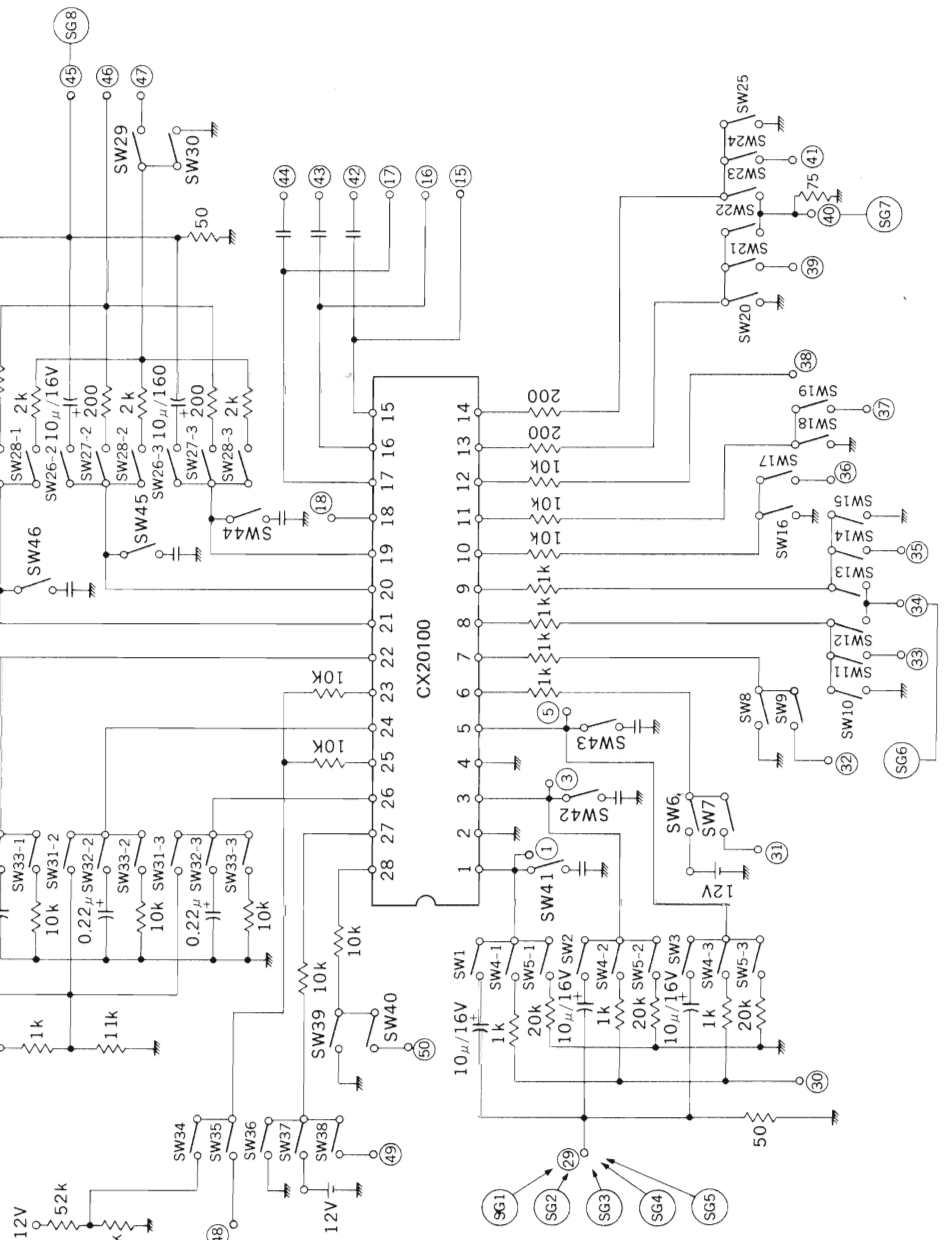


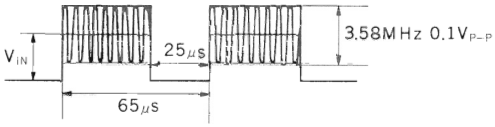
Fig. 1

Measuring Method Supplemental Description

Measuring items 162 to 164 DG

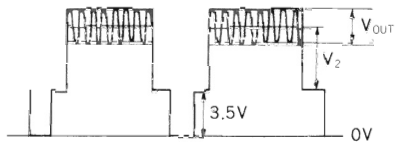
Output waveform and measuring method description

Input signal ㉙ SG3



V_{IN} 0.1V, 0.35V, 0.7V

Output signal waveform



When V_{IN} is 0.1V: V_2; approx. 0.43V, V_{OUT}; approx. 0.43 Vp-p
When V_{IN} is 0.35V: V_2; approx. 1.5V, V_{OUT}; approx. 0.43 Vp-p
When V_{IN} is 0.7V: V_2; approx. 2.9V; V_{OUT}; approx. 0.43 Vp-p

Calculation

Setting V_{OUT} as D_{R1}, D_{G1} and D_{B1} when V_{IN} is 0.1V,
setting V_{OUT} as D_{R2}, D_{G2} and D_{B2} when V_{IN} is 0.35V,
and setting V_{OUT} as D_{R3}, D_{G3} and D_{B3} when V_{IN} is 0.7V,
calculate the following equations in reference to individual RGB.

$$\frac{D_{R1} - D_{R2}}{D_{R1}} \times 100, \quad \frac{D_{R1} - D_{R3}}{D_{R1}} \times 100, \quad \frac{D_{R2} - D_{R3}}{D_{R2}} \times 100$$

(Similar calculation as the above should be carried out in reference to G and B.)

Standard Circuit Design Data

DC characteristics (See Fig. 2)

No.	Pin voltage [V] RGB TV signal mode (SW: a)	Pin voltage [V] RGB EXT signal mode (SW: b)	No.	Pin voltage [V] RGB TV signal mode (SW: a)	Pin voltage [V] RGB EXT signal mode (SW: b)
1	3.0	3.0	15	5.7 to 6.1	3.2 to 4.6
2	0	0	16	5.7 to 6.1	3.2 to 4.6
3	3.0	3.0	17	5.7 to 6.1	3.2 to 4.0
4	0	0	18	12.0	12.0
5	3.0	3.0	19	6.0	6.0
6	12.0	12.0	20	6.0	6.0
7	0	0	21	6.0	6.0
8	0	0	22	11.0	11.0
9	0	0	23	10.2	10.2
10	3.0	0	24	11.0	11.0
11	0	0	25	10.2	10.2
12	1.5	1.5	26	11.0	11.0
13	0	0	27	0	0
14	1.0	1.0	28	0	0

DC Characteristics Measuring Circuit

{ RGB TV signal mode SW: a
RGB EXT signal mode SW: b

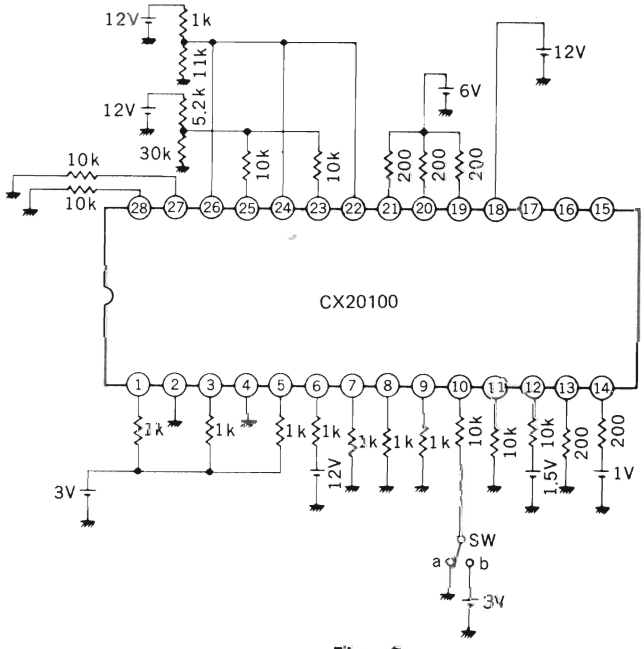


Fig. 2

Description of Operation

In the CX20100, input analog signals of 2 systems are processed and output as shown in the block diagram of Fig. 3.

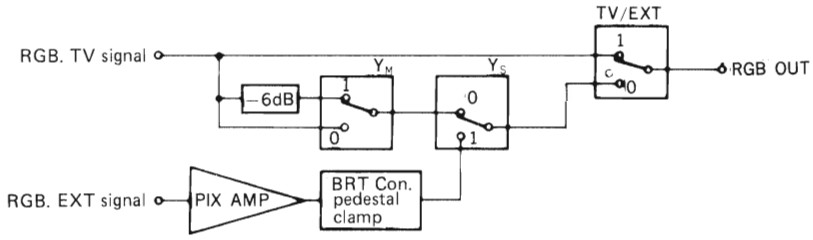


Fig. 3

It is obvious from the diagram (Fig. 3) that by combining with these TV/EXT, Y_M and Y_S switches the output modes shown in Table 1 are realized. Furthermore, the combinations of these TV/EXT, Y_M and Y_S switches, and output modes are determined by based upon the EIAJ standards.

When the output mode is TV mode, RGB TV signal is output as it is through the buffer amplifier. When it is in halftone mode, from black to white signals are output, but their levels are lowered 6 dB. When EXT mode, RGB EXT signal is output. RGB EXT signal is output after being picture controlled and bright controlled.

There are 3 picture controlling pins; namely, PIX-1 (pin 6), PIX-2 (pin 7) and LEVEL SHIFT (pin 11). In operation, either one of PIX-1 or a combination of PIX-2 and LEVEL SHIFT is used.

In PIX-1, it has a positive correlation between PIX-1 control voltage and the picture amplifier gain. However, in PIX-2, it has a negative correlation between PIX-2 control voltage and the picture amplifier gain. The applied voltage to the LEVEL SHIFT pin is superimposed to the voltage applied to PIX-2 controlling pin, and it is further applied to the picture amplifier as a picture amplifier gain controlling voltage.

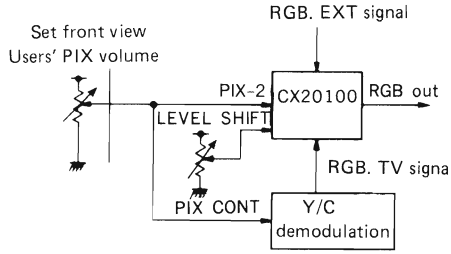


Fig. 4

Here, an actually used example of the LEVEL SHIFT is briefly described. As shown in Fig. 4, PIX control voltage from PIX Cont. volume, which is generally used by the users, is applied to the picture control section of Y/C demodulation circuit and PIX-2 pin of the CX20100. At this point, the gain levels of RGB TV signal and RGB EXT signal at RGB out become almost the same levels. However, it is often desired that the level of RGB EXT signal is suppressed lower than that of RGB TV signal. Unfortunately, PIX-2 has a negative correlation between the applied voltage and picture amplifier gain as previously mentioned, therefor, in order to suppress the level of RGB EXT signal, it is necessary that to apply a higher voltage than the PIX control voltage that has been applied to the picture control section of Y/C demodulation circuit. It is sufficient to apply the voltage higher than the PIX control voltage to the LEVEL SHIFT pin. The bright control of CX20100 has 4 control pins; namely, BRT_1 (pin 27), BRT_2 (pin 28), B-sub BRT (pin 23) and G-sub BRT (pin 25). When using them, either one combination of BRT_1 and B.G-sub BRT or BRT_2 and B.G-sub BRT has to be used. G.B-sub BRT is subordinated to BRT_1 or BRT_2. At BRT_1 and BRT_2, R-ch, G-ch and B-ch are changed simultaneously. At G-sub BRT and B-sub BRT, G-ch and B-ch can be adjusted independently. At BRT_1 and BRT_2, the correlation between the applied control voltage and the pedestal level is inverse.

That is, at BRT_1, if the control voltage increases, the pedestal level becomes up and at BRT_2, if the control voltage increases, the pedestal level becomes down.

Application circuit

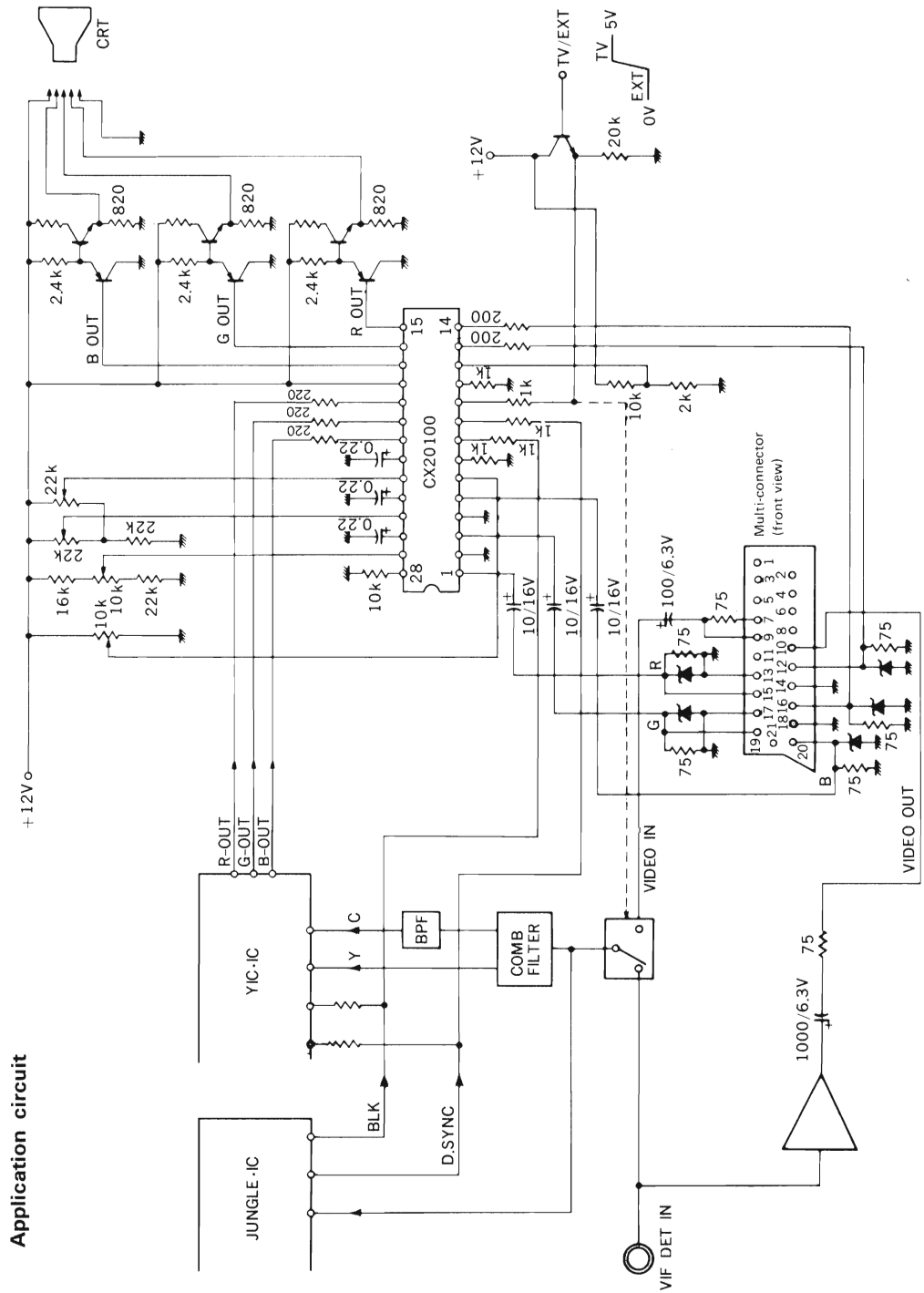
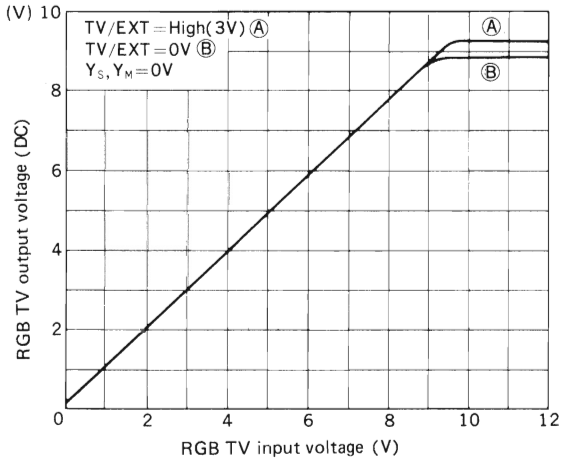
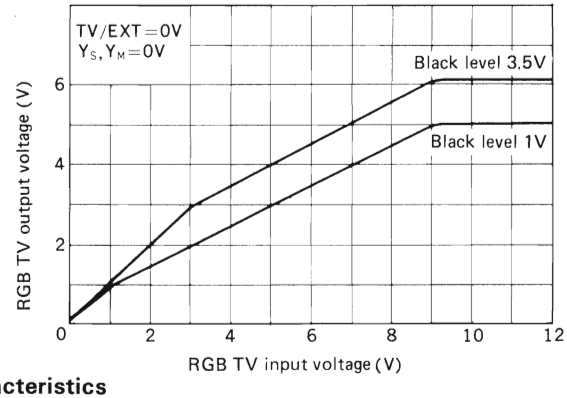


Fig. 5

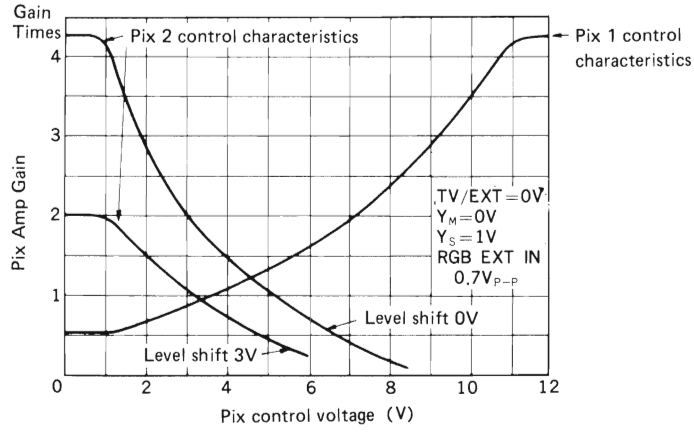
TV input/output characteristics



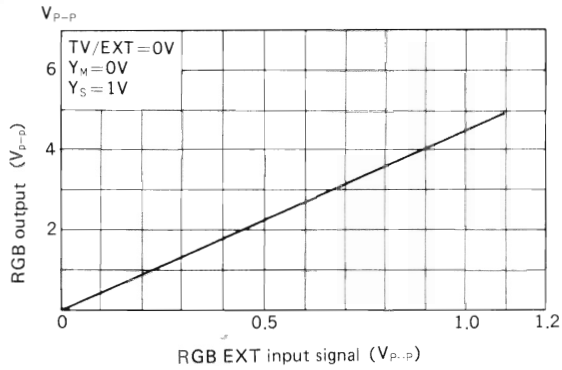
Input/output characteristics during halftone



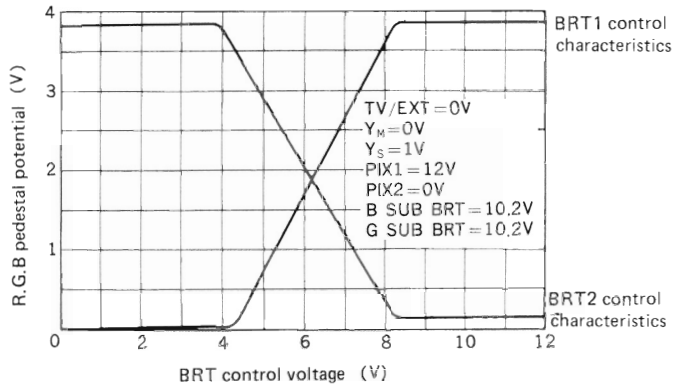
PIX control characteristics



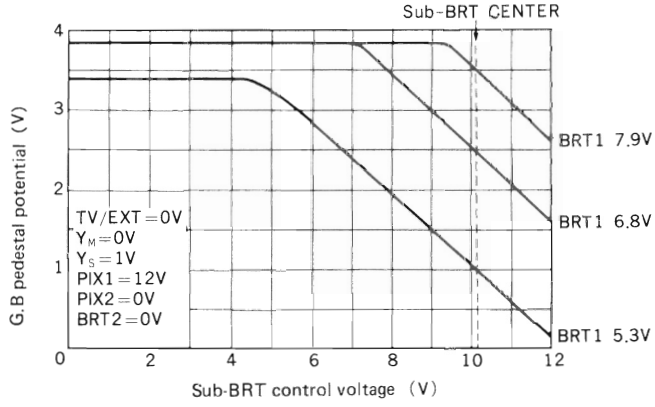
PIX Amp. D range



BRT control characteristics



Sub-BRT control chracteristics



SONY **CX20106A**

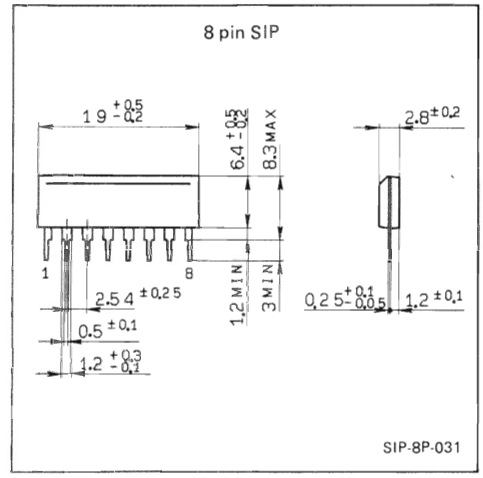
Preamplifier for Remote Control Use

Description

The CX20106A is a bipolar IC for receiving preamplifier of infraredremote control system. It is comprised of a primary stage amplifier, limiter amplifier, BPF, signal waveform detecting circuit, waveform shaping circuit, etc..

Package Outline

Unit: mm



Features

- Low power consumption (Vcc=5V, 9 mW typ.)
- Low power supply voltage (Vcc=5V)
- Built-in filter (Enables to vary center frequency with an externally attached resistor. fo=30 kHz to 60 kHz, 40 kHz typ.)
- It is free from inductance due to magnetic field since it uses no inductance coil.
- Possible to direct connection to a photodiode
- Open collector output (possible to direct connection to TTL and CMOS)

Structure

Bipolar silicon monolithic IC.

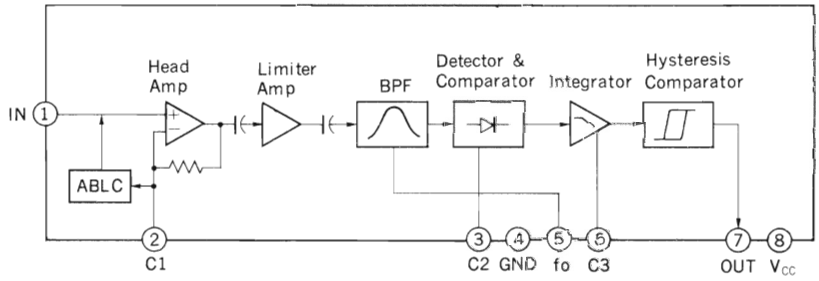
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	17	V
• Input voltage	V_{IN}	5	Vp-p (pin 1 input)
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	P_D	0.6	W

Recommended Operating Condition

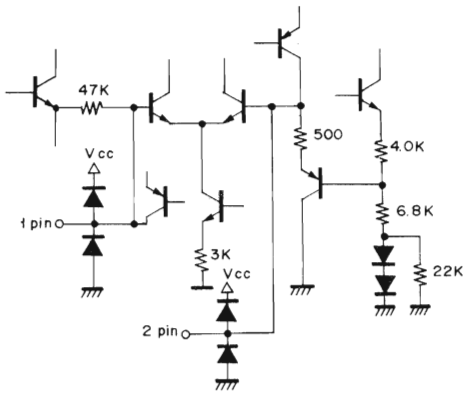
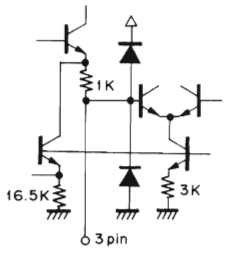
• Supply voltage	V_{CC}	4.7 to 5.3	V

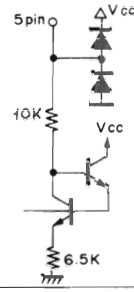
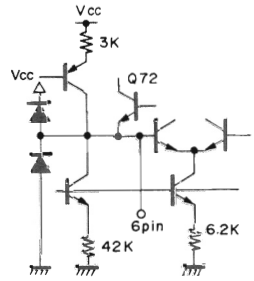
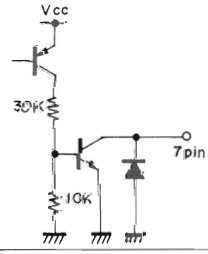
Block Diagram



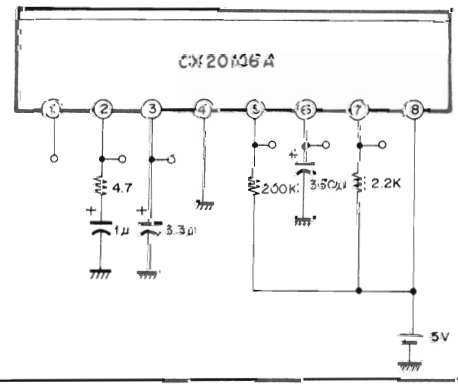
Pin Description

Pin voltages are depended on the DC Characteristics Test Circuit.

No.	Symbol	Voltage	Equivalent circuit	Description
1	IN	2.5V		An input pin. Connect a photodiode with PIN structure between the pin and GND.
2	C1	2.5V		Connect a resistor and capacitor in series between the pin and GND and set the frequency characteristics and gain of the "Head amp". When the resistance is large and capacitance is small, the gain becomes small. When the capacitance is large, the sensitivity is lowered against the transient response.
3	C2	1.5V		Connect a detection capacitor between the pin and GND. When the capacitance is large, the sensitivity becomes lowered against the mean value detection wave and transient response. When the capacitance is small, fluctuation of the peak detection wave and output pulse width becomes large. The capacitor to be used is of standard 3.3 μF, however, set it so that the output pulse width fluctuation and noise elimination characteristics become optimum.
4	GND			An GND pin of the IC. Make the pattern design so that the parts to be attached externally will be located as closely as possible to this pin and to be grounded them at the same one point. The reaching distance and noise elimination characteristics are greatly influenced by the pattern design of around the GND.

No.	Symbol	Voltage	Equivalent circuit	Description
5	fo	1.4V		Connect a resistor between the pin and the power supply. Set the center frequency of the built-in BPF. See "Pin 5 externally attached resistor vs. Center frequency characteristics".
6	C3	1.0V		Connect an integral capacitor between the pin and GND. Connect an integral capacitor of standard 330 pF. When a large capacitance is used, it becomes strong against disturbance noise and the low level section of the output pulse becomes longer. However, if the capacitance becomes too large the reaching distance becomes shorter.
7	OUT	5.0V		An open-collector output. Connect a loading resistor between this pin and the power supply. It should be low level standard of 0.2V when using a loading resistor of 2.2 kΩ.
8	Vcc	5.0V		The power supply voltage pin.

DC Characteristics Test Circuit



Electrical Characteristics

V_{CC} = 5V, Ta = 25 ℃

No.	Item	Symbol	Test condition			Test point	Min.	Typ.	Max.	Unit	Remark
			Signal	Level	ON-SW						
1	Input pin voltage (1)	$V_{IN}1$			S1, 8, 11−a	A	2.0	2.5	3.1	V	
2	Input pin voltage (2)	$V_{IN}2$			S1, 2, 4, 8, 11−a	A	0.6	1.0	1.7	V	
3	L level output voltage	V_{OL}			S3, 7−a, 10, 11−a	D	−	0.2	0.4	V	
4	Output leakage current	I_{OH}			S3, 7−b, 9, 11−a	C	−	0	2.2	μA	
5	Voltage gain	A_v	40 kHz cw	50μV_{P-P}	S2, 5, 6, 7−c, 11−a	B	74	79	84	dB	
6	BPF characteristics	A_{vo}	30 kHz, 37 kHz, 43kHz, 50kHz cw	50μV_{P-P}	S2, 5, 6, 7−c, 11−a	B	4	9	−	dB	*1
7	Input impedance	r_{in}	40 kHz cw	0.2 V_{P-P}	S1, 2, 6, 8, 11−a	A	27	40	55	kΩ	Input level denotes Vi and measured value Vx. *2
8	Detecting ability (1)	$V_{in}1$	burst wave	60μV_{P-P}	S2, 5, 6, 8, 10, 11−a	D	440	540	770	μs	Input a burst wave signal of 1.2 mS cycle, 40 kHz.
9	Detecting ability (2)	$V_{in}2$	burst wave	50mV$_{P-P}$	S2, 5, 6, 8, 10, 11−b	D	440	660	770	μs	Input a burst wave signal of 1.2 mS cycle, 40 kHz.
10	Consumption current	I_{CC}			S3, 8, 11−a	E	1.0	1.8	2.8	mA	

Note) *1 The level ratio between AC level of during 37 kHz and that of 30 kHz denotes A1[dB].

$$A1 \equiv 20\log \frac{\text{measure value(f=37 kHz)}}{\text{measure value(f=30 kHz)}}$$

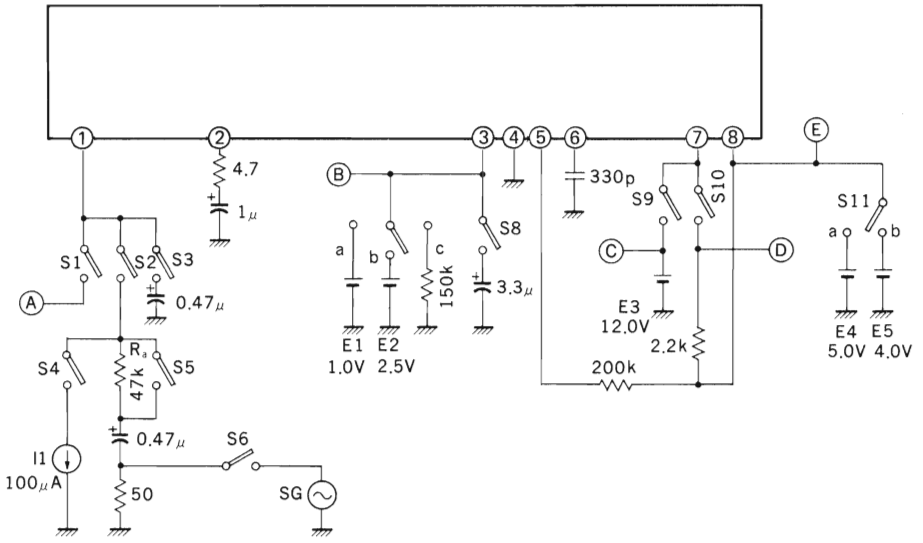
The level ratio between AC level of during 43 kHz and that of 50 kHz denotes A2[dB].

$$A2 \equiv 20\log \frac{\text{measure value(f=43 kHz)}}{\text{measure value(f=50 kHz)}}$$

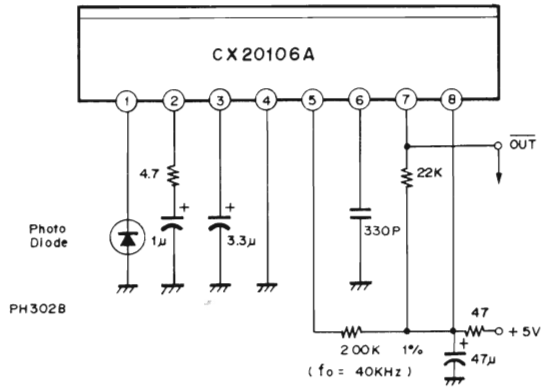
Note) *2 $rin \equiv \dfrac{47\ k\Omega}{\frac{Vi}{Vx} - 1}$ [kΩ]

SONY®

Electrical Characteristics Test Circuit



Application Circuit

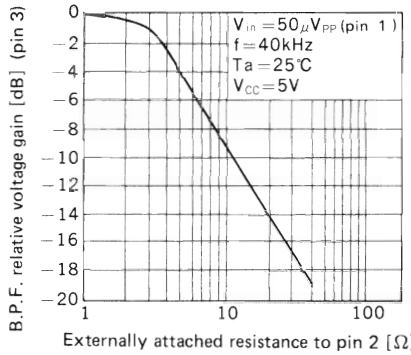


Description of Operation (See the Block Diagram)

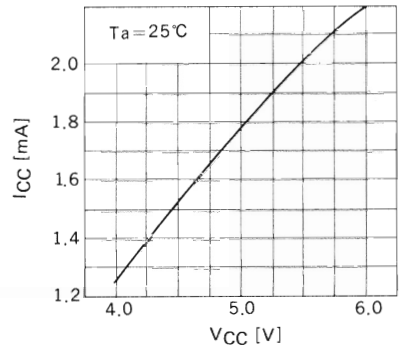
Receive the infrared signal transmitted from the infrared remote control commander with a photodiode and output rectangular waves as an output.

I/O pin	Waveform	Operation
Pin 1 input waveform	40μVp-p to 2.5Vp-p 600μS Standard Standard 40kHz	Converts the signal current of a photodiode into voltage and amplifies it.
BPF output waveform (Pin 3)		Suppresses the noise component with BPF.
Pin 6 Hysteresis Comparator input waveform		Detects the signal component and performs wave detection.
Pin 7 output waveform	5V 0.2V Standard	Integrates the signal component and makes it as rectangular wave output from the Hysteresis Comparator.

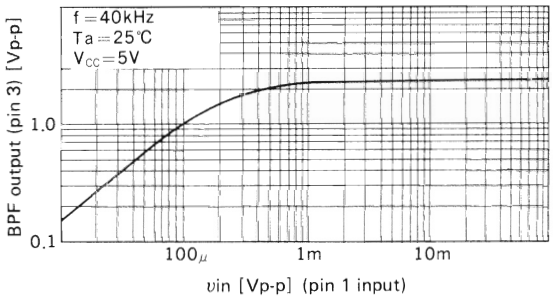
AV characteristics vs. Externally attached resistance to pin 2



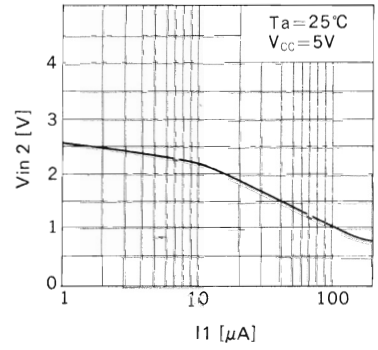
ICC vs. VCC characteristics



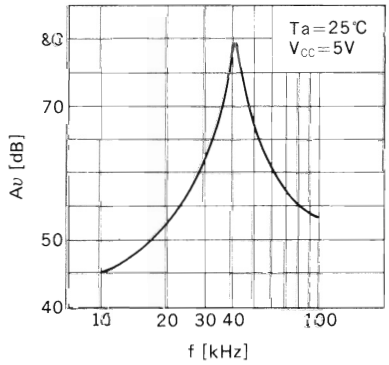
Pin 3 output voltage characteristics vs. Pin 1 input voltage



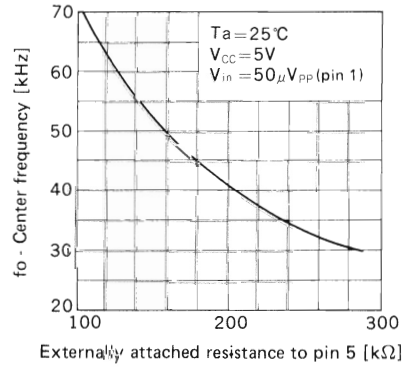
VIN2 vs. I1 characteristics



AV vs. f characteristics



Center frequency characteristics vs. Externally attached resistance



SONY CX20112

US Audio Multiplexing Decoder

Description

The CX20112 is a bipolar IC for the Zenith system of US TV audio multiplexing decoding, having all the necessary filters for stereo demodulation and SAP (Separate Audio Program) demodulation within the IC. In combination with the CXA1011P for dbx-TV NR IC, a US audio multiplexing demodulating system can easily be realized.

Features

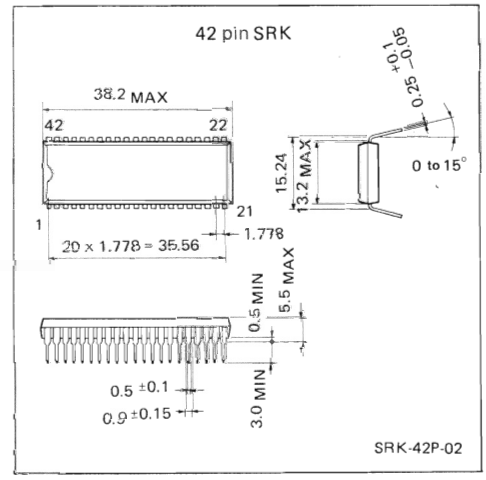
- Incorporation of various kinds of filters within the IC, permits a maked reduction in the number of parts to be externally attached to it.
- Excellent channel separation characteristics when stereo playing. Min. 46 dB when applying 1 kHz.
- Permits selection of individual modes of MAIN/SAP/BOTH.
- Permits directly driving mode display LED.

Structure

Bipolar silicon monolithic IC

Package Outline

Unit: mm



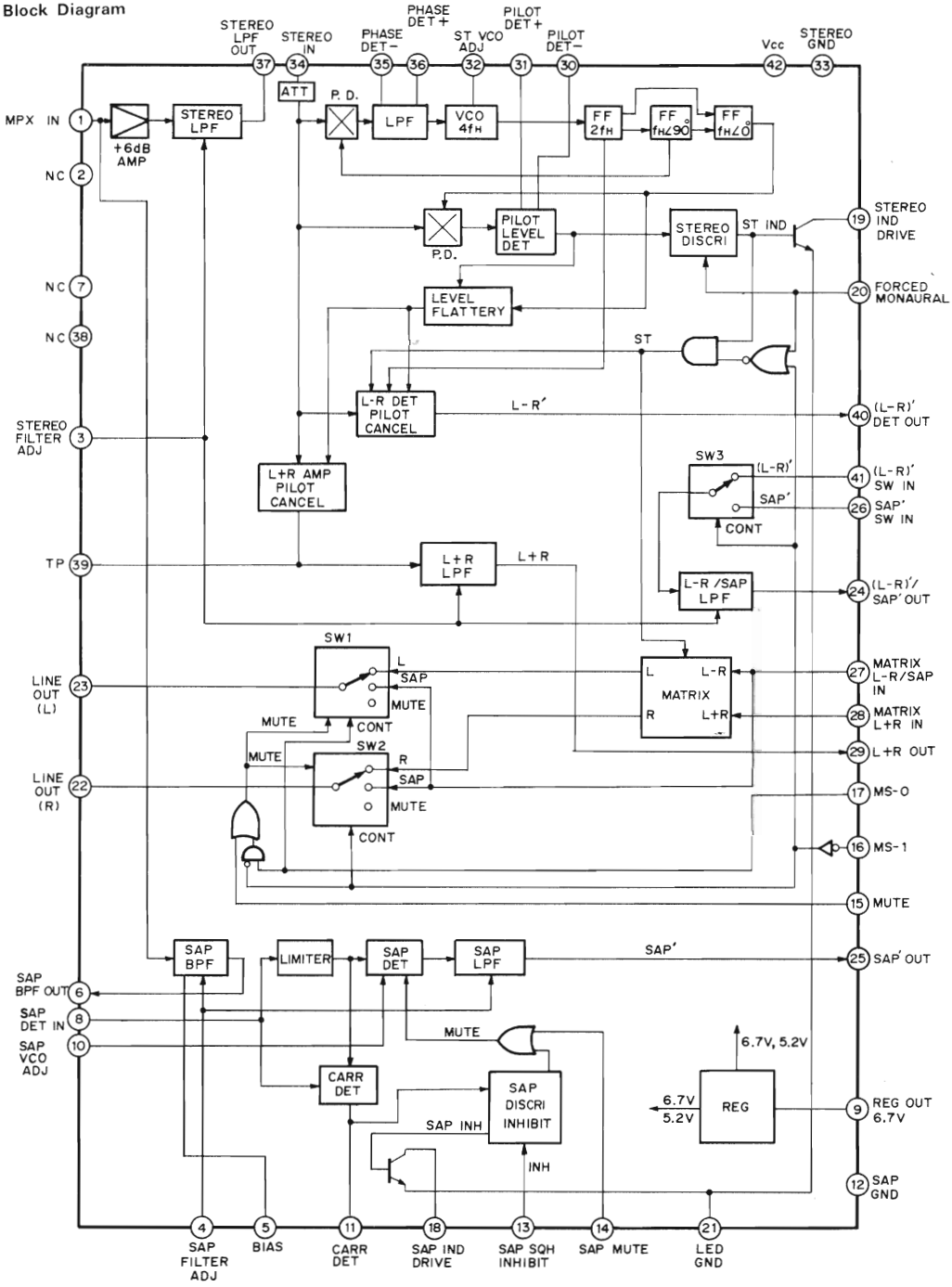
Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	17	V
• Operating temperature	Topr	−10 to +65	°C
• Storage temperature	Tstg	−55 to +150	°C
• Individual controlling pins	$V_{14\ to\ 17, 20}$	V_{CC} +0.3	V
• LED driving current	I_{LED}	25	mA
• Allowable power dissipation	P_D	1800	mW

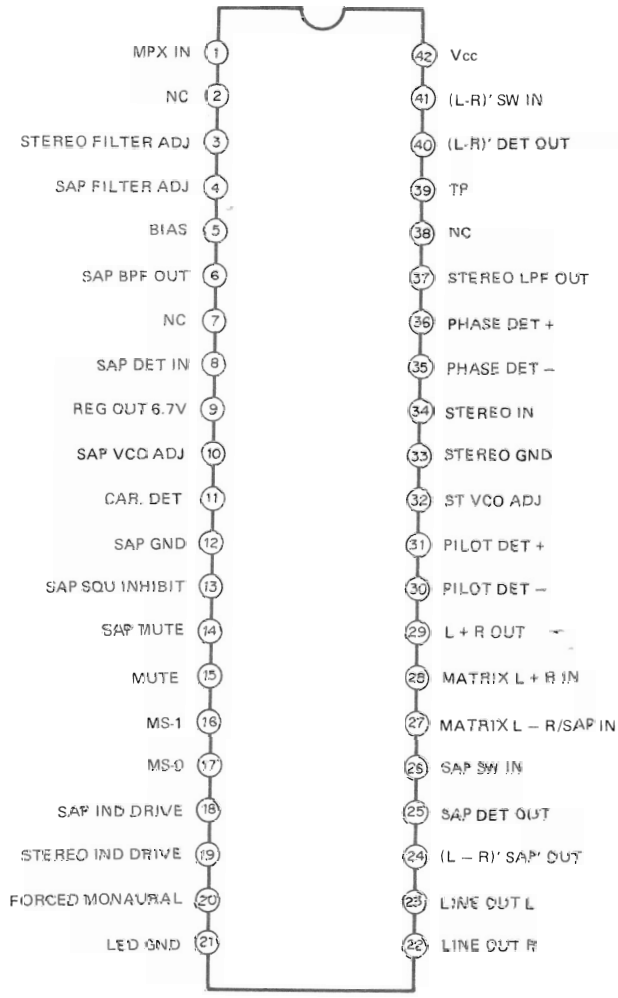
Recommended Operating Condition

• Supply voltage	V_{CC}	9.0±0.5	V

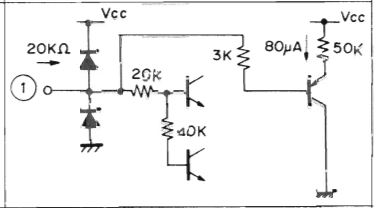
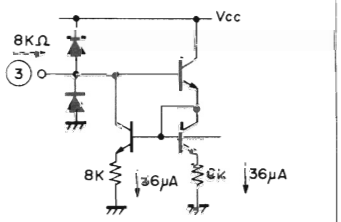
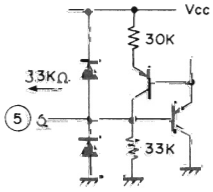
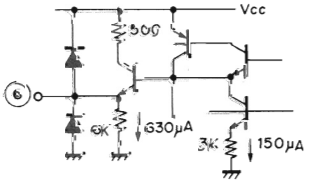
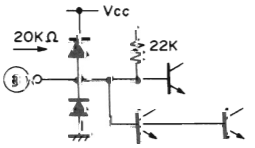
Block Diagram

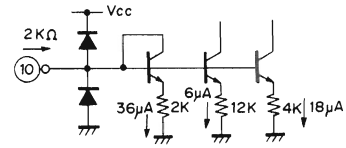
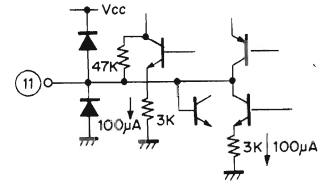
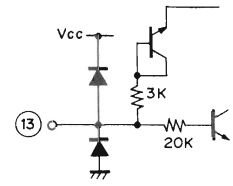
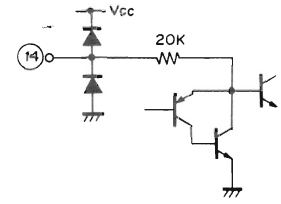
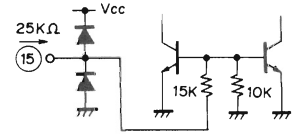
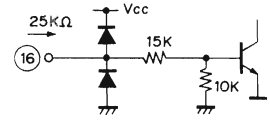


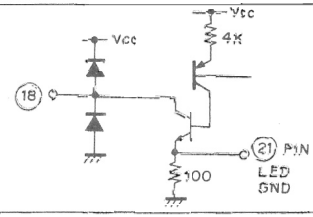
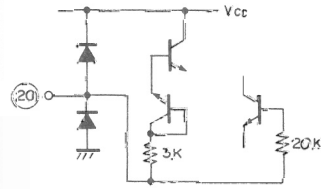
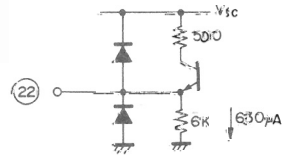
Pin Configuration

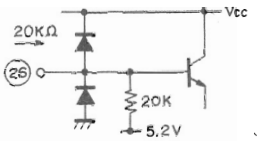
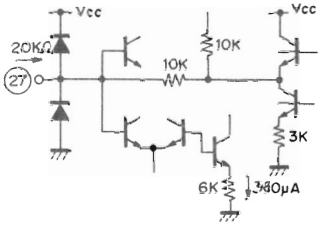
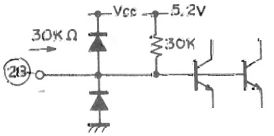
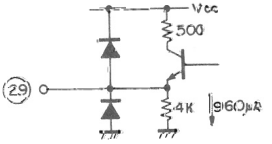
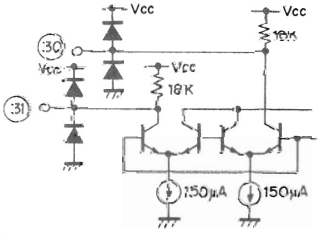


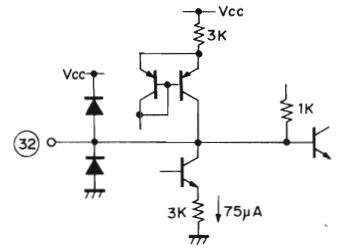
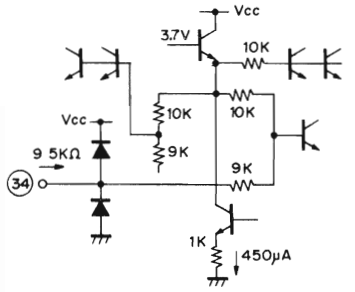
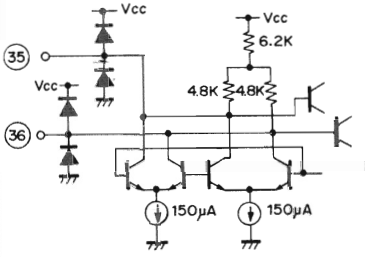
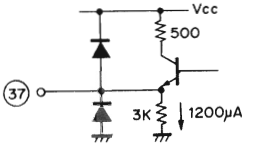
Pin Description (Ta=25°C, Vcc=9V)

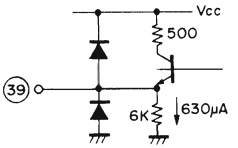
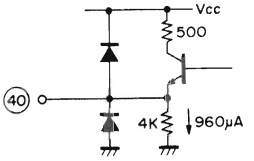
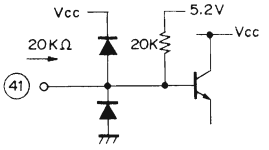
No.	Symbol	Description	Voltage (Typ.)	Equivalent circuit
1	MPX IN	A composite signal is input from this pin. Its reference level is 0.7 Vp-p (247 mVrms, −9.9 dBs) when monaural 100 % (±25 kHz).	4.5V	
2	NC			
3	STEREO FILTER ADJ.	Connects resistances in series and a variable resistance between pins 9 and 3. The characteristics of a filter are adjusted with variable resistance. Stereo low-pass filter, L+R low-pass filter and L-R/SAP low-pass filter, are operated in interlocking manner to adjust the cut off frequency.	1.7V	
4	SAP FILTER ADJ.	Adjusts the cutoff frequency of SAP band-pass filter and SAP low-pass filter.	1.7V	Similar to pin 3
5	BIAS	An internal bias current fine adjustment pin of SAP band-pass filter.	7.4V	
6	SAP BPF OUT	An output pin of SAP band-pass filter.	3.4V	
7	NC			
8	SAP DET IN	An input pin of SAP detecting circuit. Its input is the output of SAP band-pass filter with capacitance coupling.	2V	
9	REG OUT 6.7V	A stabilized power supply output.	6.7V	

No.	Symbol	Description	Voltage (Typ.)	Equivalent circuit
10	SAP VCO ADJ.	Adjust VCO of SAP detector to 5f_H (78.67 kHz) by using this pin. Actually, it is adjusted with DC voltage of pin 25.	0.77V	
11	CARR DET	An output pin of SAP carrier detecting (AM detecting) circuit. Smoothing is carried out by connecting a capacitance to this pin. Existence or non-existence of SAP is found with this DC voltage.	2.55V	
12	SAP GND	A GND of SAP block.		
13	SAP SQH INHIBIT	When the carrier of SAP is in the non-existent state, it becomes muting function due to squelch. If it is necessary to prohibit this function, set it to Vz M level (2.5V to 5.5V). In addition, if it is set to Vz H (8V to V_{CC}), SAP indicating output can not be output even when SAP broadcasting is existent, accordingly, the lamp is not lit.		
14	SAP MUTE	Mutes the outputs of LINE and OUT (pins 22 and 23). It works at Vx H level.		
15	MUTE	If this pin is set to Vx H level, the output of pin 25 (SAP, OUT) becomes muting.		
16	MS-1	A mode switch. It is used in combination with MS-0 of pin 17.		
17	MS-0	A mode switch. It is used in combination with MS-1 of pin 16.		Similar to pin 16.

No.	Symbol	Description	Voltage (Typ.)	Equivalent circuit
18	SAP IND DRIVE	When existence of SAP broadcasting is distinguished, it drives the indicator. The inflowing current of this pin is 20 mAmax. ($V_{CE(SAT)}$=1.3 Vtyp.) with an open collector output.		
19	STEREO IND DRIVE	When existence of stereo broadcasting is distinguished, it drives the indicator, etc. The inflowing current of this pin is 20 mAmax. ($V_{CE(SAT)}$=1.3 Vtyp.) with an open collector output.		Similar to pin 18
20	FORCED MONAURAL	A 3-value input pin. It works stereo function when it is set to Vz L level, and monaural function (stereo indicator is in normal operation) when set to Vz M level (2.5V to 5.5V). When it is set to H level (over 8V to Vcc), it is set to monaural function, and stereo indicating output is prohibited.		
21	LED GND	The GND of LED current connect to grounding. (see pin 33)		-
22	LINE OUT (R)	It is the right side line out pin. The reference level of its output is 1.3 Vp-p when 0.7 Vp-p is input to pin 1.	3.7V	
23	LINE OUT (L)	The left side out pin. Its level gain is similar to pin 22.	3.7V	Similar to pin 22
24	(L−R)/SAP OUT	An output pin whose output has been passed through the low-pass filter which has been switched into (L−R) and SAP modes. It is connected to a noise reduction unit.	3.6V	Similar to pin 22
25	SAP OUT	It is an output pin of FM detector of SAP.	3.5V	Similar to pin 22

No.	Symbol	Description	Voltage (Typ.)	Equivalent circuit
26	SAP' SW IN	Input the output of pin 25 SAP' OUT to this pin. Either one signal of L−R' which is input from pin 41 or this signal is selected by SW, and it is output to pin 24 after going through the low-pass filter. Matching of the input level of SAP, which is to be input to the noise reduction unit, to the reference input level can be carried out by adjusting the input level to this pin.	5.15V	
27	L-R/SAP IN	The output of the noise reduction unit is input to this pin. The reference level is 1.4 Vp-p with 100% individually. Practically, adjust this input level so that the channel separation becomes maximum.	4.4V	
28	L+R IN	Input the output signal of pin 29 after passing through the de-emphasis circuit which is attached externally. Determines the de-emphasis constant. The equivalent input impedance of the circuit is 30 kΩ.	5V	
29	L+R OUT	An output pin of L+R. The de-emphasis circuit connected at the near of this pin. (See pin 28)	3.45V	
30	PILOT DET−	An output pin of the pilot level detector. The output is smoothed by connecting a capacitance.	6.45V	
31	PILOT DET+	By connecting a variable resistance between pins 30 and 31, pilot signal cancelling adjustment can be performed.	6.45V	

No.	Symbol	Description	Voltage (Typ.)	Equivalent circuit
32	ST VCO ADJ.	The oscillation frequency is determined by the time constants of capacitance and resistance connected here. In consideration of the temperature characteristics, use polypropylene (P.P.) capacitor.		
33	ST GND	The GND of stereo block. Connect to grounding.		
34	STEREO IN	Input the output of pin 37.	3V	
35 36	PHASE DET− PHASE DET+	Connect the time constant for low-pass filter of PLL between pins 35 and 36	6.75V 6.75V	
37	STEREO LPF OUT	An output pin for stereo low-pass filter.	3.15V	

No.	Symbol	Description	Voltage (Typ.)	Equivalent circuit
38	NC			
39	T.P.	A monitoring pin of L+R AMP/pilot cancelling circuit output. Normally, it is not used.	3.7V	
40	(L−R), DET OUT	An output pin of SUB(L−R) after being synchronous AM detected. The output includes harmonic components of $2f_H$, etc.	3.8V	
41	(L−R), SW IN	Similar to pin 26, an input pin to SW and LPF.	5.15V	
42	V_{CC}	Apply +9V to this pin.	9V	

Electrical Characteristics (Vcc=9V, 0 dBs=0.775 Vrms, Ta=25°C)

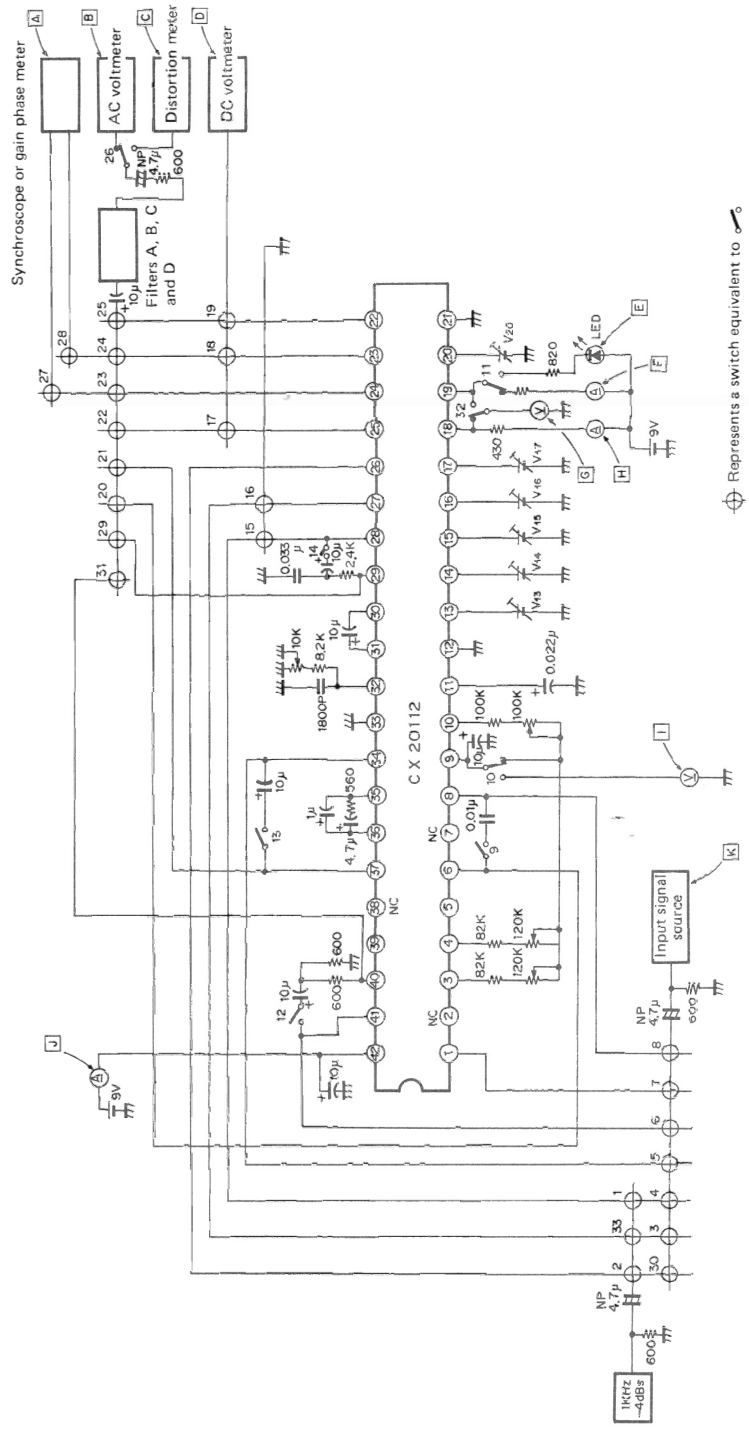
No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	SAP noise level	$V_{SAP,\ N}$	Pin 1 input 5 f_H (−14.4 dBs) Pin 25 output 15 kHz LPF is attached		−40	−36	dBs
2	SAP carrier leakage	CL_{SAP}	Pin 1 input 5f_H (−14.4 dBs) Pin 25 output		−33	−30	dBs
3	SAP carrier detecting sensitiviry	S_{CARR}	Pin 1 input 5f_H Input level during LED of pin 18 is lighting on	−29.0	−25.0	−21.5	dBs
4	SAP frequency characteristics 10 kHz	A_{SAP}	Pin 1 input SAP 10 kHz 100% (−14.4 dBs) Pin 25 output 15 kHz LPF is attached	−4.0	−1.5	2.0	dBs
5	SAP output level	V_{SAP}	Pin 1 input SAP 1 kHz 100% (−14.4 dBs) Pin 25 output 15 kHz LPF is attached	−0.8	−0.1	0.6	dBs
6	SAP distortion ratio	THD_{SAP}	Pin 1 input SAP 1 kHz 100% (−14.4 dBs) Pin 25 output 15 kHz LPF is attached		4.0	8.0	%
7	SAP BPF frequency characteristics 5f_H	A BPF 5f_H	Pin 1 input 5f_H (−14.4 dBs) Pin 6 output	−16	−13.5	−11.5	dBs
8	SAP BPF frequency characteristics 3f_H	A BPF 3f_H	Pin 1 input 3f_H (−14.4 dBs) Pin 6 output		−32.5	−29.5	dBs
9	SAP BPF frequency characteristics 6.5f_H	A BPF 6.5f_H	Pin 1 input 6.5f_H (−14.4 dBs) Pin 6 output		−31.6	−29.5	dBs
10	SAP detecting characteristics	$V_{SAP\ FM}$	Pin 8 input 63.37 kHz (−14.4 dBs) 93.67 kHz (−14.4 dBs) Pin 25 output	100	110	118	mV/kHz
11	SAP muting attenuation amount	AT_{SAP}	Pin 8 input SAP 1 kHz 100% (−14.4 dBs) Pin 25 output 15 kHz LPF is attached		−68	−65	dBs
12	MONAURAL noise level	$V_{ST\ NM}$	Non-input Pin 23 output 15 kHz LPF is attached		−75	−70	dBs
13	STEREO noise level	$V_{ST\ NS}$	Pin 1 f_H (−24 dBs) Pins 40 to 41 −6 dB ATT Pin 24 output 15 kHz LPF is attached		−70	−66	dBs
14	MAIN output level	V_{MAIN}	Pin 1 input1 kHz (−10 dBs) 75 μs deemphasis is attached Pin 23 output 15 kHz LPF is attached	−5.6	−5.0	−4.6	dBs
15	SUB detecting level	V_{SUB}	Pin 1 input SUB 1 kHz 100% Pins 40 to 41 −6 dB ATT Pin 24 output 15 kHz LPF is attached	−9		−6	dBs

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
16	MONAURAL distortion ratio	THD_{MONO}	Pin 1 input 1 kHz (−10 dBs) Pin 23 output 15 kHz LPF is attached		0.25	0.50	%
17	STEREO distortion	THD_{STE}	Pin 1 input SUB 1 kHz 100% Pin 24 output 15 kHz LPF is attached		0.75	1.20	%
18	Pilot cancel (L+R)	PC_{L+R}	Pin 1 input f_H (−24 dBs) 75 us de-emphasis is attached Pin 23 output f_H BPF is attached		−57.0	−51.5	dBs
19	Pilot cancel (L−R)	PC_{L-R}	Pin 1 input f_H (−24 dBs) Pins 40 to 41 −6 dB ATT Pin 24 output f_H BPF is attached		−41	−35	dBs
20	MAIN Balance of between channels	CB_{MAIN}	Pin 34 input f_H (−18 dBs) Input 1 kHz (−4 dBs) to pin 28 and find the output level difference between pins 22 and 23 by measuring the outputs (15 kHz LPF is attached) of pins 22 and 23 independently.	−0.3	0	0.3	dB
21	SUB Balance of between channels	CB_{SUB}	Input 1 kHz (−4 dBs) to pin 27 and find the output level difference between pins 22 and 23 by measuring the outputs (15 kHz LPF is attached) of pins 22 and 23 independently. The above applicable to pin 28 except that non-input to pin 28 .	−0.3	0	0.3	dB
22	Separation check 1 kHz	SEP_{1K}	Pin 1 input L-ch 100% DSB 1 kHz Measure phase difference between the outputs of pins 24 and 29 .	45	60		dB
23	Crosstalk (L−R) (SAP)	$CT_{L-R\ SAP}$	Pins 26 and 41 input 1 kHz (−4 dBs) Pin 24 output +1 kHz BPF		−80	−67	dBs
24	Crosstalk L SAP	$CT_{L\ SAP}$	Pins 27 and 28 output 1 kHz (−4 dBs) Pin 23 output +1 kHz BPF		−80	−74	dBs
25	Crosstalk R SAP	$CT_{R\ SAP}$	Pins 27 and 28 input 1 kHz (−4 dBs) Pin 22 output +1 kHz BPF		−80	−74	dBs
26	Stereo LPF frequency characteristics ($6f_H$)	$ALP1\ 6f_H$	Pin 1 input $6f_H$ (−10 dBs) Pin 37 output		−45	−36	dBs
27	(L+R) LPF frequency characteristics (12 kHz)	ALP2 12k	Pin 34 input 12 kHz (−4 dBs) Pin 29 output	−5.2	−4.3	−2.8	dBs
28	(L+R) LPF frequency characteristics ($2f_H$)	$ALP2\ 2f_H$	Pin 34 input $2f_H$ (−4 dBs) Pin 29 output		−52	−43	dBs

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
29	L−R LPF frequency characteristics (12 kHz)	ALP3 12k	Pin 26 input 12 kHz (−4 dBs) Pin 24 output	−6.5	−5.3	−4.0	dBs
30	L−R LPF frequency characteristics ($2f_H$)	ALP3 $2f_H$	Pin 26 input $2f_H$ (−4 dBs) Pin 24 output		−52	−43	dBs
31	Stereo capture range LOW	CR_{LO}	Pin 34 input f_H vicinity (−18 dBs) Measure the input frequency when the LED of pin 19 goes on and off by changing the burst signal frequency.			14.95	kHz
	Stereo capture range HIGH	CR_{HI}	Pins 35 and 36, 1 μF and 4.7 μF 560Ω	16.52			kHz
32	During forced monaural crosstalk (L)	CT_L	Pin 27 input 1 kHz (−4 dBs) Pin 23 output +1 kHz BPF		−80	−74	dBs
33	During forced monaural crosstalk (R)	CT_R	Pin 27 input 1 kHz (−4 dBs) Pin 22 output +1 kHz BPF		−80	−74	dBs
34	Muting SW V15 High Muting attenuation amount (L) (R)	$AT_{ST\ L}$	Pin 27 input 1 kHz (−4 dBs) Pins 22 and 23 output +15 kHz LPF		−80	−74	dBs
35	DC offset voltage while muting and stereo are turned on	$VO_{MU\ ST}$	Durig non-input During non-input	−120	−20	120	mV
36	DC offset voltage while muting and SAP are turned on	$VO_{MU\ SAP}$	During non-input	−50	5	50	mV
37	DC offset voltage while SAP and monaural are turned on	$VO_{SAP\ MO}$	During non-input	−50	0	50	mV
38	DC offset voltage while SAP and stereo are turned on	$VO_{SAP\ ST}$	During non-input	−120	0	120	mV
39	DC offset voltage while stereo and monaural are turned on	$VO_{ST\ MO}$	During non-input	−120	−20	120	mV
40	Circuit current	I_{CC}	Value of inflowing current into pin 42	25	36	48	mA
41	V_{14}, V_{15}, V_{16} and V_{17} controlling voltage (L)	Vx L		GND		1.0	V
42	V_{14}, V_{15}, V_{16} and V_{17} controlling voltage (H)	Vx H		2.5		V_{CC}	V

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
43	V_{13} and V_{20} controlling voltage (L)	V_Z L		GND		1.0	V
44	V_{13} and V_{20} controlling voltage (M)	V_Z M		2.5		5.5	V
45	V_{13} and V_{20} controlling voltage (H)	V_Z H		8.0		V_{CC}	V
46	Stereo discriminating level	STE Vth	Pin 30 and 31 10 μF f_H level is variable	12	26	39	mVrms
47	Regulator voltage	V_{REG}	Pin 9 DC		6.7		V

Electrical Characteristics Test Circuit



Supplemental Description of Signal

- SAP 10 kHz 100% MOD
  78.67 kHz±10 kHz FM modulation, −14.4 dBs
- SAP 1 kHz 100% MOD
  78.67 kHz±10 kHz FM modulation, −14.4 dBs
- SUB 1 kHz 100%
  1 kHz DSB (2f_H, 1.4 Vp-p) + f_H (0.14 Vp-p)
- L-ch 100% DSB 1 kHz
  1 kHz DSB (2f_H 1.4 Vp-p) + f_H (0.14 Vp-p) + 1 kHz (0.35 Vp-p)
- f_H vicinity (−18 dBs) burst signal
  A burst signal which enables variation of frequencies around the center frequency of 15.734 kHz and with time intervals over 0.5 second.

Description of Filters for Measurement

A	Low-pass filter	[Tertiary butterworth 15 kHz (−3 dB)]
B	Band-pass filter	[Secondary f_H (15.734 kHz), bandwidth 1.5 kHz]
C	Band-pass filter	[Secondary 1 kHz, bandwidth 100Hz]
D	Through	

Notes on Measuring

Adjustment before measurement

1. ST FILTER ADJ
   Adjust at the trapping point of stereo low-pass filter.
   Input a signal (0.42 Vp-p) of 5f_H (78.67 kHz) to MPX IN (pin ①) and adjust so that the output of ST LPF OUT (pin ㊲) becomes minimum.

2. SAP BPF ADJ
   Adjust at the trapping point of SAP band-pass filter.
   Input a signal (0.42 Vp-p) of 4f_H (62.936 kHz) to MPX IN (pin ①) and adjust so that the output of SAP BPF OUT (pin ⑥) becomes minimum.

3. ST VCO ADJ
   Examine the connected portion (W1, W2) of the solid resistance and variable resistance, which are being connected to pin ㉜ in a non-input state, by using a probe of low capacity high impedance, and adjust its free-running frequency within 4f_H (62.936 kHz±100 Hz).
   Specification of the probe is high impedance (≧1MΩ) and low capacity (≦10 pF).

4. SAP VCO ADJ
   Measure the DC voltage of pin ㉕ when Vx H (2.5V to 5.5V) is applied to pin ⑭, and denotes the measured voltage as V_{25}. Then, applying Vx L to pin ⑭, input a signal (0.42 Vp-p) of 5f_H (78.67 kHz) to MPX IN (pin ①). At this point, adjust so that the DC voltage of SAP, OUT (pin ㉕) becomes within V_{25}±0.1V.

5. Regarding channel separation measurement
   The channel separation measurement can be conducted by connecting the outputs of pins ㉔ and ㉓ to X and Y axes of a synchroscope and by either using a resurge graph or to read the phase difference directly. If a gain phase meter is available, more precise separation measurements than the above can be achieved by using it.

6. Regarding measurement of the balance between channels L and R
   To measure the balance between L channel and R channel, it is necessary to measure pins ㉒ and ㉓ separately. At first, turn relay SW24 for output on and read the values of pins ㉓, and turn relay SW24 for outputs off, and then turn relay SW25 for output on and read the values of pins ㉒. The specification is that the difference value between pins ㉓ and ㉒.

Mode Matrix

Mode Function

Pin No.		LINE OUT	
17	16	L	R
L	L	L+R	SAP
L	H	L	R
H	L	SAP	SAP
H	H	(MUTE)	

Forced Monaural Function

Pin No.	LINE OUT		STEREO INDICATOR
20	L	R	
L	L	R	ON
M	L+R	L+R	ON
H	L+R	L+R	OFF

SAP SQH(squelch) Inhibit Function

Pin No.		SAP
13	SQH	INDICATOR
L	ON	ON
M	OFF	ON
H	OFF	OFF

Description of Operation

This IC is a USA TV audio multiplexing decoder which has the baseband spectrum as shown in Fig. 1. The flows of the signals are roughly separated into 3; namely, L+R (MAIN), L−R (SUB) and SAP as shown in Fig. 2.

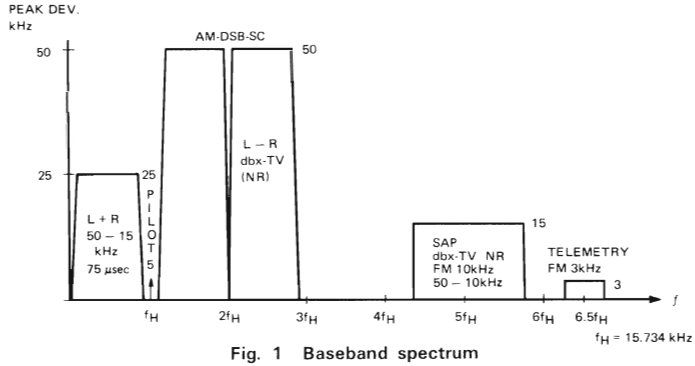


Fig. 1 Baseband spectrum

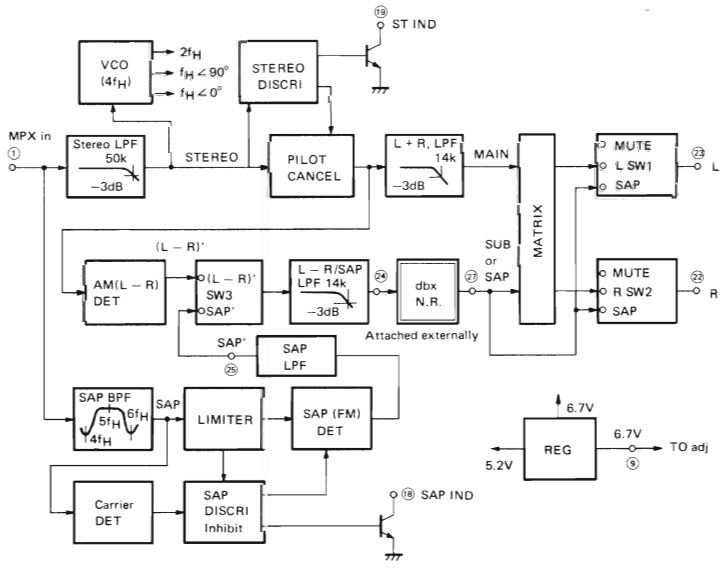


Fig. 2 Block diagram

A. L+R (MAIN)
MPX signal is input from pin ① , and SAP and TELEMETRY are eliminated with stereo LPF. Then, pilot cancellation is carried out. Finally, L−R is eliminated with L+R LPF and L+R only is selected to be input to the matrix.

B. L−R (SUB)
Up to the pilot cancellation, similar to L+R. Since L−R is an AM-DSB, amplitude modulation is carried out. At this point, up to 15 kHz there exists L−R on the signal spectrum and also signals remain in the high frequency band. The signal is being encoded with dbx, therefore, it is represented as (L−R)' in Fig. 2. Then, select (L−R)', and SAP', and they are input to SW3 allows to use LPF and dbx noise reduction circuits to be used commonly, and the residual signals in the high frequency band are eliminated with L−R/SAP LPF. As L−R is being applied to dbx NR, connect dbx noise reduction decoder between pins ㉔ and ㉗ . After this, it is input to the matrix as L−R (SUB).

C. SAP is FM signal whose carrier is of $5f_H$ therefore, eliminates only the SAP signal is eliminated by using a BPF of $5f_H$. It is input to SW3 after it is FM detected. The rear stage from SW3 is a combined use with L−R. SAP, in the figure means SAP' signal which is being encoded with dbx.

D. In addition to the above, there is a mode discriminating circuit. Discrimination of stereo is carried out by detecting the amplitude of the pilot signal. Discrimination of SAP is carried out by detecting the carrier of $5f_H$. VCO generates $4f_H$ with PLL and provides $2f_H$, $f_H \angle 90°$, and $f_H \angle 0°$ by dividing it with a flip-flop. $2f_H$ is used for AM detection, $f_H \angle 90°$ for PLL, and $f_H \angle 0°$ to extract the pilot signal. The regulator provides voltages of 6.7V and 5.2V and those are supplied to the individual circuits within the IC, 6.7V is also output to pin 9 which is used as a regulation voltage.
L+R and L−R are separated into L and R with the matrix, and they are input to SW1 and SW2. SW1 and SW2 are used with mode selection pins to allocate the outpus of pin ㉓ L and pin ㉒ R to either one of L+R, SAP, MUTE, L and R.

Description of Application Circuit

1. The pilot cancellation amount can be improved by connecting a variable resistance between pins ㉚ and ㉛ . The adjusting method is to input 15.734 kHz, 0.14 Vp-p to pin ① first, then observe the level from pin ㊵ through the 15.734 kHz BPF, and adjust with the volume so that it becomes minimum.

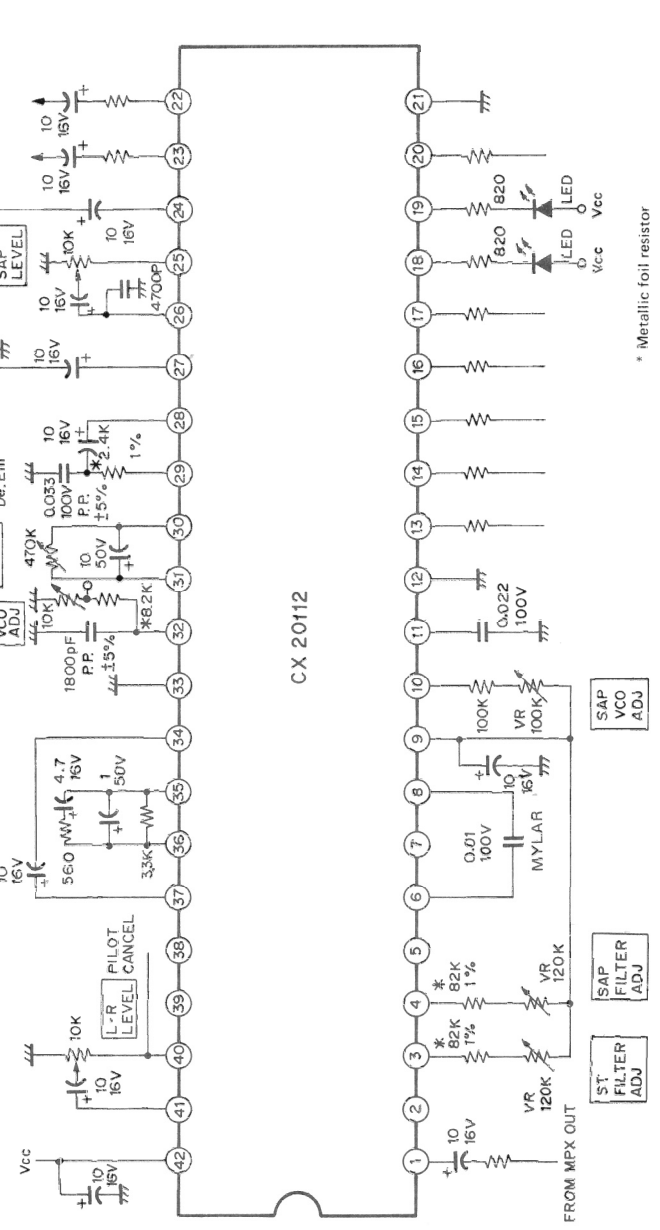
2. The DC loop gain can be reduced by connecting a resistance between pins ㊱ and ㉟ . (Makes it possible to change the capture range)

3. L and R level adjustment (pins ㊵ to ㊶)
Input a signal of 400 Hz, pre-emphasis off, VR off and SUB 100%. Set the mode of the IC into stereo (set pin ⑰ to Vx L and pin ⑯ to Vx H). At this point, adjust the level of NR IN so that it becomes 100% of the level that is specified with NR.

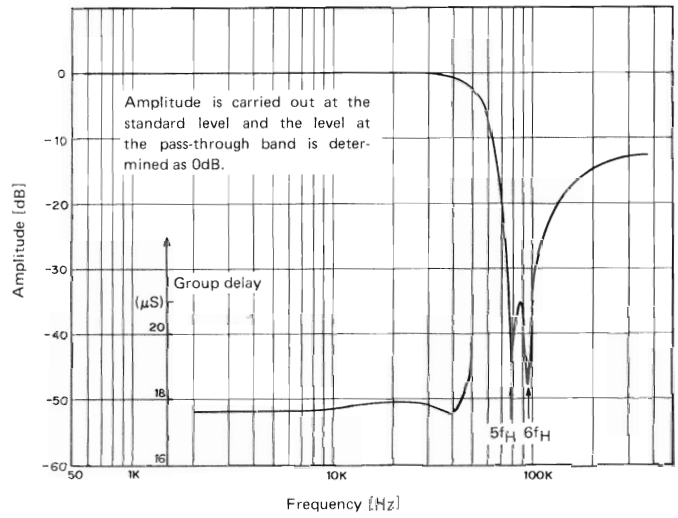
4. SAP adjustment (pins ㉕ to ㉖)
Input a signal of 400 Hz, noise reduction off, and SAP 100% modulated. Set the mode of IC into SAP mode (set pin ⑰ to Vx H and pin ⑯ to Vx L). At this point, adjust the level of NR IN so that it becomes 100% of the level that is specified with NR.

5. Separation adjustment (NR OUT to pin ㉗)
First, adjustment of the noise reduction circuit should be carried out. Then, adjust the input level of pin ㉗ so that separation at individual frequencies becomes maximum.

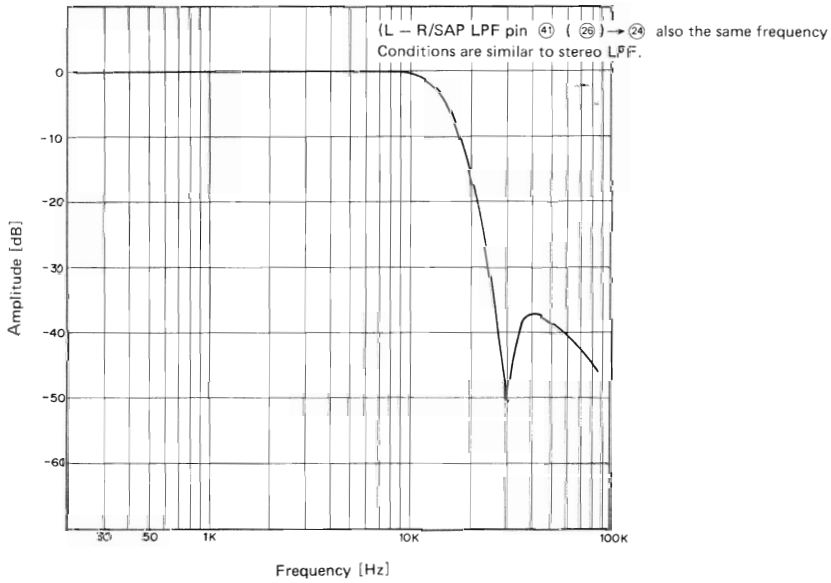
Application Circuit



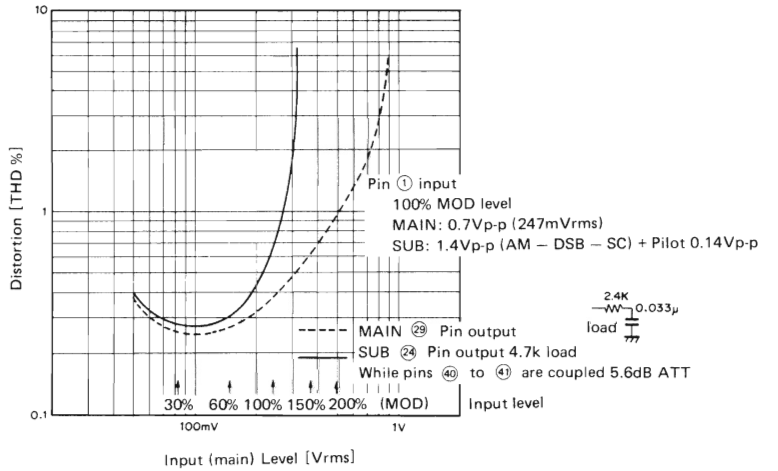
Stereo LPF frequency characteristics pins ① → ㊲



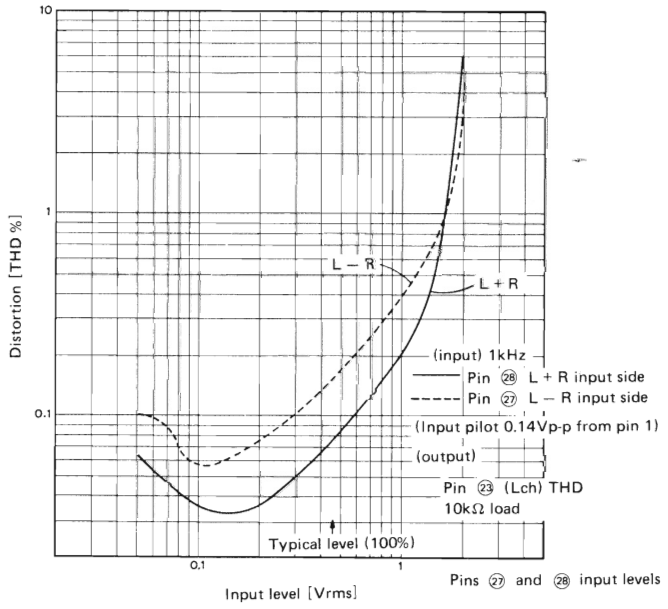
Frequency characteristics of L+R LPF pins ㉞ → ㉙



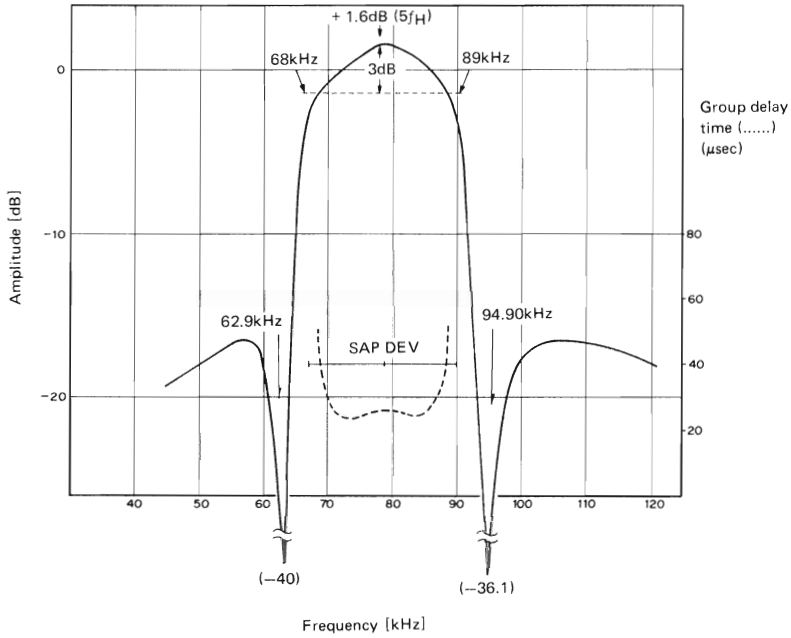
Distortion rate characteristics — MAIN and SUB input



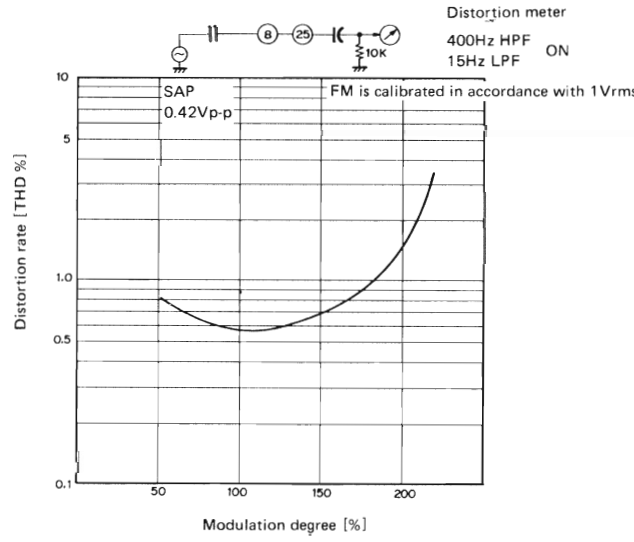
Distortion rate characteristics — stereo matrix input



SAP BPF frequency characteristics and group delay



SAP detector dynamic range



Dynamic Picture

Description

The CX20125 is a bipolar IC designed for luminance signal processing of video signals. It has several functions such as auto pedestal, DC restoration correction, black extension amplifier, etc.

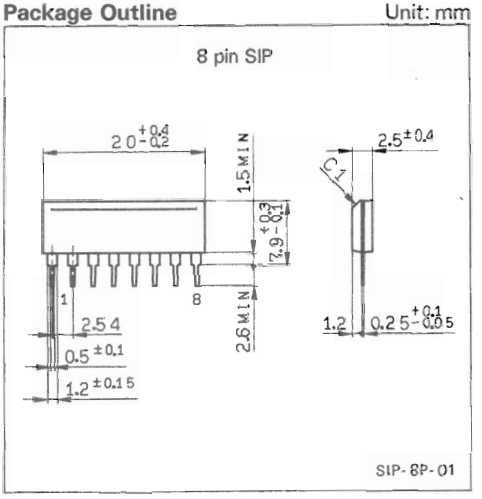
This IC detects signals with the blackest level and controls the gain of black level in video signals automatically, to render the blackest level equal to the pedestal level.

Features

As the auto pedestal function only operates near the black level of video signals in the CX20125, it is least affected on the white side compared to auto pedestal ICs in other systems. (For example, it is not affected by luminance to chrominance ratio variations or luminous intensity changes due to sudden level variations in black signals.)

Package Outline

Unit: mm



Structure

Bipolar silicon monolithic IC

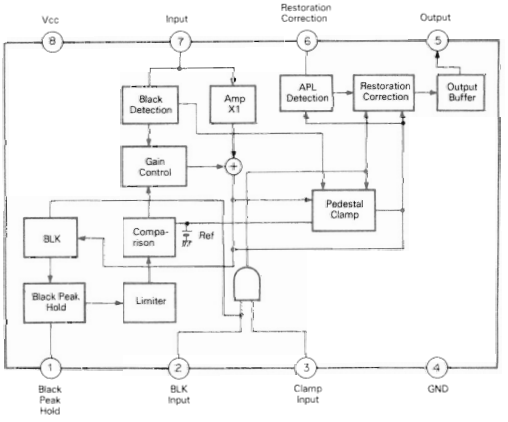
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	15	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	600	mW

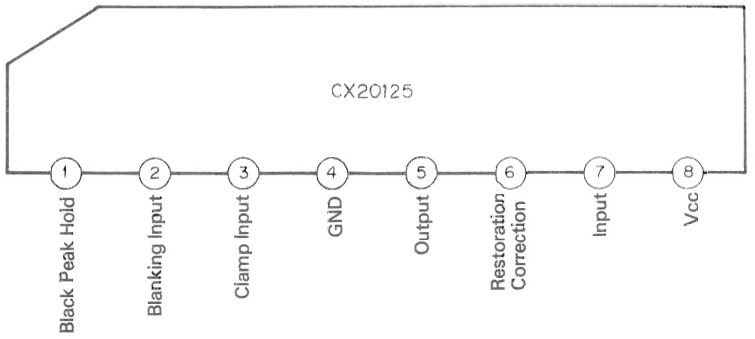
Recommended Operating Condition

• Supply voltage	Vcc	12.0±0.5	V

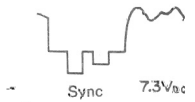
Block Diagram



Pin Configuration

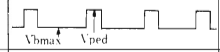
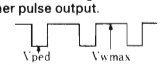
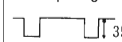
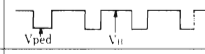


Pin Description

No.	Name	Description
1	Black Peak Hold	The blackest DC level among the pedestal-clamped signals in the IC is output. That is, the peak is detected by the external R and C.
2	Blanking Input	composite blanking pulse input (threshold 1 V_{BE})
3	Clamp Input	Clamp pulse input (threshold 2 V_{BE})
4	GND	
5	Output	The luminance signal with its black extended and transmission rate correction pulse added is output. The pedestal DC level is 7.3V and its polarity is the same as the input. 
6	Restoration Correction	The luminance signal without sync is output. This signal is integrated by the external R and C for controlling the restoration correction pulse height of the pin (5) output. (This pulse is in the pedestal interval) The amount of correction varies according to R.
7	Input	A luminance signal is coupled through a capacitor to this pin with 1 Vp-p (0.7Vp-p for "black" → "white") This capacitor performs the clamping. The pedestal level of this pin is 5.4V DC. The input signal is supplied through the emitter follower.
8	Vcc	1.2V

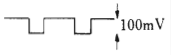
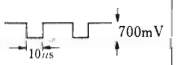
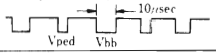
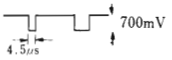
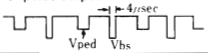
Electrical Characteristics

Ta = 25°C, Vcc = 12V

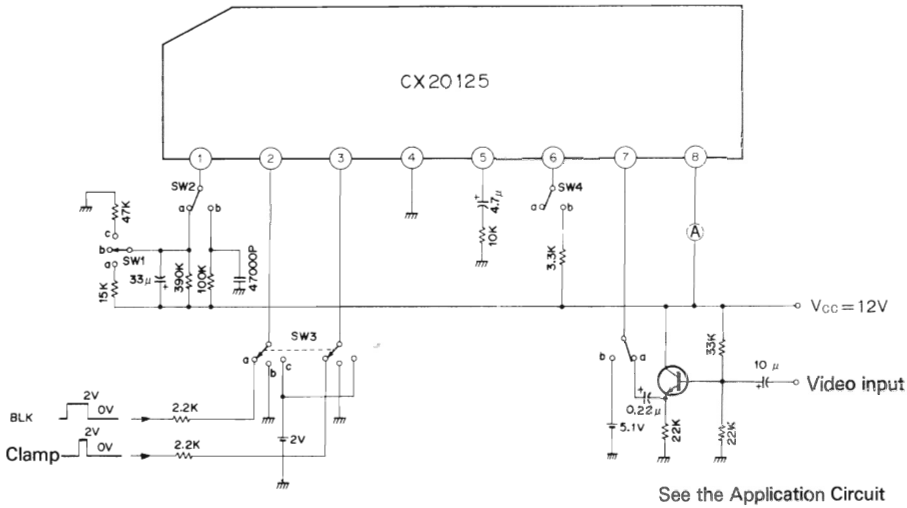
No.	Item	Symbol	SW conditions SW1	SW2	SW3	SW4	SW5	Input signal	Test point	Output waveform & testing method	Min.	Typ.	Max.	Unit
1	Current consumed		b	a	a	a	a		⑧ Vcc		5.7	7.5	9.5	mA
2	Pedestal clamp operation	Vped	b	a	a	a	a		⑤	Measure DC voltage (pedestal level) of pin 5 when no signal is on.	6.3	7.3	7.9	V
3-1	Black extension operation	Vbmax	a	a	a	a	a		⑤	Measure DC voltage of lower pulse output when no signal is on. 				
3-2	Black extension value	ΔVb								Calculation ΔVb = Vped − Vbmax	100	150	200	mV
4-1	White output level 1	Vw	c	a	a	a	a	Input signal (a)	⑤	Measure DC voltage of higher pulse output.				
4-2	Gain	ΔVw-ped								Calculation Black/white level $\Delta Vw-ped = \frac{Vw-Vped}{\text{Pedestal output of white output}}$	605	670	735	mV
5-1	White output level 2	Vwmax	a	a	a	a	a	Input signal (a)		Measure DC voltage of higher pulse output. 				
5-2	Black extension operation point 1 (White side)	ΔVw								Calculation ΔVw = Vw − Vwmax Measure white level variation when the black gain turns from maximum to minimum.	−10.5	0	10.5	mV
6-1	50% output level 1	VH	c	a	a	a	a	Input signal (b) 	⑤	Measure DC voltage of higher pulse output.				
6-2	50% output level 2	VHmax	a	a	a	a	a		⑤	Measure DC voltage of higher pulse output. 				
6-3	Black extension operation point 2 (50% level)	ΔVH								Calculation ΔVw = Vw − Vwmax Measure 50%-level variation when the black gain turns from maximum to minimum.	−2.1		19	mV

Electrical Characteristics

Ta = 25°C, Vcc = 12V

No.	Item	Symbol	SW conditions SW1	SW2	SW3	SW4	SW5	Input signal	Test point	Output waveform & testing method	Min.	Typ.	Max.	Unit
7-1	Black level	Vb1	b	a	a	a	a	Input signal (c) 	⑤	Measure DC voltage of higher pulse output.				
7-2	Black extension operation (White side)	ΔVb1								Calculation ΔVb1 = Vb1 − Vped Measure black level output (input 100mV black).	32	43	54	mV
8-1	Larger area black level	Vbb	b	a	a	a	a	Input signal (d) 	⑤	Measure DC voltage of black signal area (10-μ wide) of pulse output. 				
8-2	Larger area operation	ΔVbb								Calculation ΔVbb = Vbb − Vped The larger black signal level becomes the same as Vped.	−21		21	mV
9-1	Small area black level	Vbs	b	a	a	a	a	Input signal (e) 	⑤	Measure DC voltage of black signal area (4.5-μ wide) of pulse output. 				
9-2	Smaller area operation	ΔVbs								Calculation ΔVbs = Vbs − Vbmax Smaller black signal is reduced to Vbmax.	−21		21	mV
10-1	Sync. slicer check	Vsy	b	b	b	a	b		⑥	Measure DC voltage.				
10-2		Vcl2	b	b	c	a	a		⑥					
10-3	Sync. slicer check	ΔVsy								Calculation ΔVsy = Vc12 − Vsy	4.7		53	mV
11-1	Black peak limiter check	Vp	b	b	b	a	b		①	Measure DC voltage.				
11-2		ΔVp								Calculation	38		157	mV
12-1		Vcl1	b	b	c	a	a		⑤	Measure DC voltage.				
12-2	Transmission rate correction circuit check	V_{DC}	b	b	c	b	a		⑤					
12-3		ΔV_{DC}								$\Delta V_{DC} = Vcl1 - V_{DC}$	660		987	mV

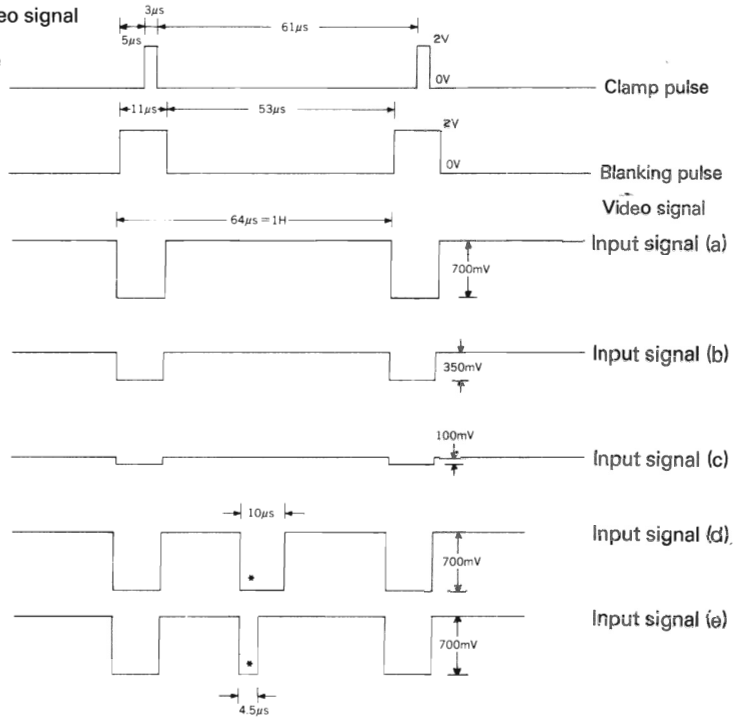
Electrical Characteristics Test Circuit



See the Application Circuit

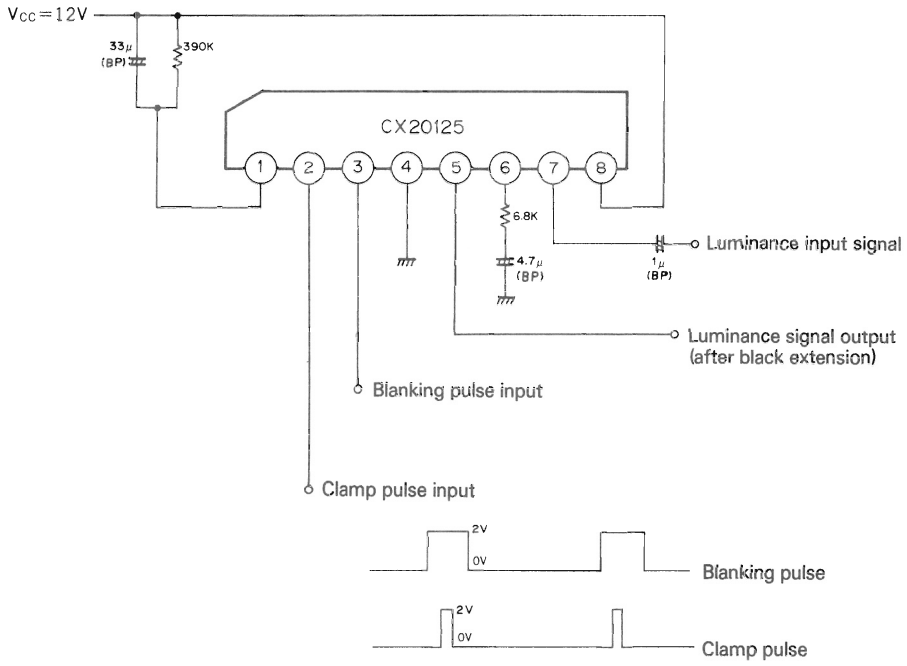
Input Signal Waveform

- Equivalent video signal
- Clamp pulse
- Blanking pulse



* Any position is permissible.

Application Circuit



Description of Functions

The level of the input video signal for CX20125 is 1Vp-p (0.7Vp-p "white"-"black"). As the IC is for luminance signal processing, the chroma is designed to be removed by trapping. The signal is coupled through a capacitor to pin 7. This external capacitor is for the feedback-type pedestal clamp operation in the IC.

The clamped input signal is sliced at about half of luminance signal, or 0.35V from the black level to obtain a black signal.

The gain of the black signal is controlled and the signal is added to the original luminance signal for the black extension operation.

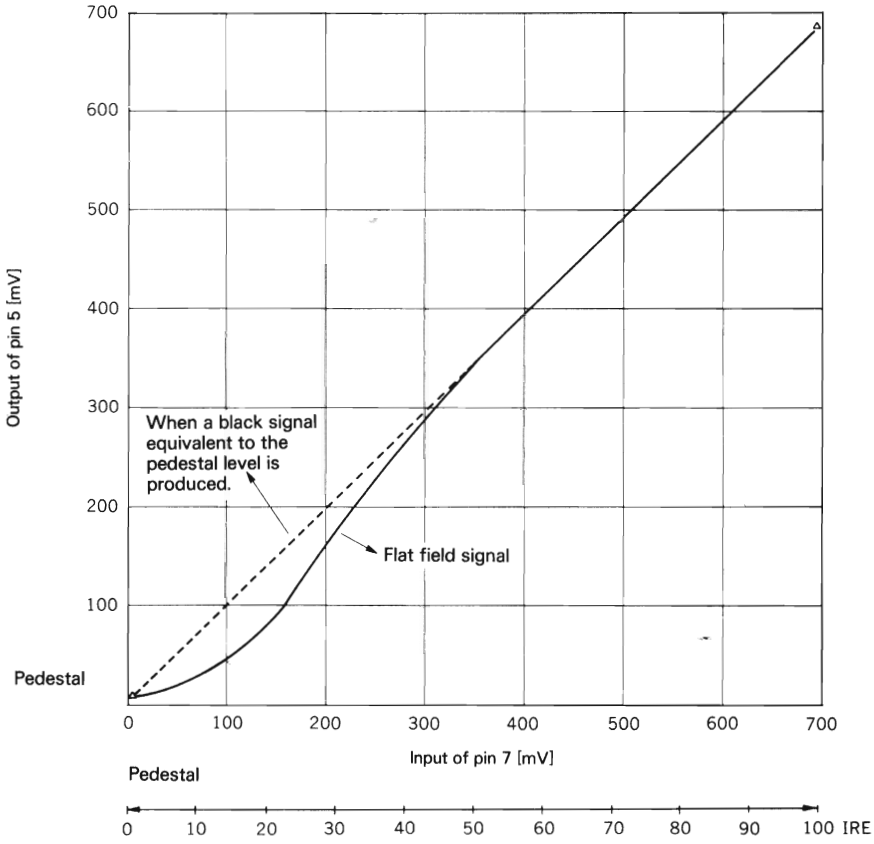
After the black extension, luminance signal is fed to the black peak hold circuit as its "front porch", "sync", and other portions excluding picture signal intervals are removed by the composite blanking signal.

The blackest level obtained by luminance signal at the black peak hold circuit is compared with the signal's pedestal DC level and its error signal is output.

The error signal becomes the control signal for the gain control circuit of the above-mentioned black signal and forms a feedback loop. The auto pedestal operation is performed according to the black signal extension system. After its sync are removed and its APL is detected, luminance signal becomes a DC restoration reverse correction pulse in proportion to APL. It is then added to the luminance signal pedestal for output.

This function is used for the reverse correction of the DC restoration for the luminance and chroma processor to be connected at a later stage.

I/O Characteristics
Signal Flat Field 0 to 100 IRE



Power Supply IC for TV

Description

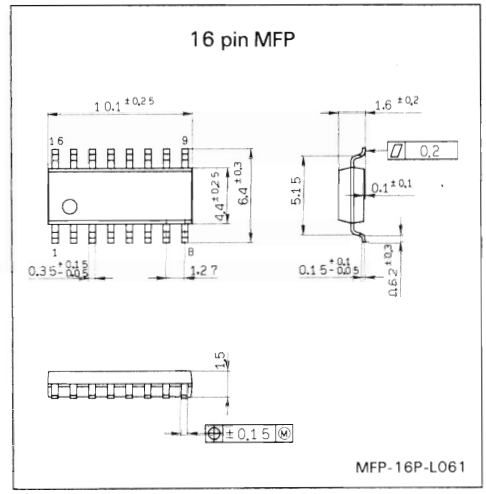
The CX20159 is a power regulator IC specially developed for small portable TVs, in which a low-voltage series regulator and a high-voltage switching regulator are integrated to form one IC chip. (External transistors are used in the output sections of the regulators.)

Features

- Operating supply voltage 3.8 to 10 V
- Low-saturation voltage regulator: 4.8 V output driver control stage incorporated; 4.8 V 300 mA
- Step up switching regulator to generate 32 V for variable capacitor incorporated; 32 V 1.5 mA
- 4.8 V enable pin method
- Zener diode for applying voltage to variable capacitor incorporated

Package Outline

Unit: mm



Structure

Bipolar silicon monolithic IC

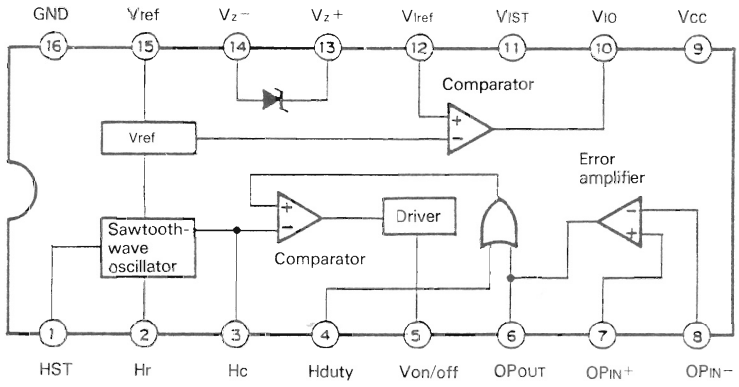
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	12	V
• ON/OFF output current	Io	20 (Vcc = 6 V)	mA
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−40 to +125	°C
• Allowable power dissipation	PD	330	mW

Recommended Operating Condition

• Supply voltage	Vcc	3.8 to 10	V

Block Diagram



Pin Description

No.	Name	Description	No.	Name	Description
1	HST	Input pin for synchronization pulses	9	Vcc	Input pin for power supply
2	Hr	Resistor pin for sawtooth-wave oscillation	10	V_{IO}	Pin for external PNP base of series regulator section
3	Hc	Capacitor pin for sawtooth-wave oscillation	11	V_{IST}	Pin for strobing series regulator section
4	Hduty	Pin for oscillation duty	12	V_{lref}	Pin for reference voltage of series regulator section (1.2 V)
5	Von/off	Pin for switching drive	13	V_z+	Pin for anode of 25.2 V Zener diode
6	OP_{OUT}	Output pin for error amplifier	14	V_z-	Pin for cathode of 25.2 V Zener diode
7	$OP_{IN}+$	Input pin (+) for error amplifier	15	Vref	Pin for reference voltage (1.2 V)
8	$OP_{IN}-$	Input pin (−) for error amplifier	16	GND	Ground pin

Electrical Characteristics

Ta = 25°C, Vcc = 6 V

Item	Symbol	Conditions	Applied pin	Test circuit	Min.	Typ.	Max.	Unit
Current consumption	Icc		Vcc – GND	1	2.2	3.6	5.0	mA
Reference voltage (1)	Vref 1	Vcc = 6 V	Vref – GND	1	1.1	1.2	1.3	V
Reference voltage (2)	Vref 2	Vcc = 3.8 V	Vref – GND	1	1.1	1.2	1.3	V

Series Regulator Section

Item	Symbol	Conditions	Applied pin	Test circuit	Min.	Typ.	Max.	Unit
Output voltage	V_{O1}	I_{O1} = 150 mA	V_{O1} – GND	1	4.5	4.8	5.1	V
Line regulation	$\triangle V_{O1}$ Line	I_{O1} = 150 mA 5.5V < Vcc < 9V	V_{O1} – GND	1			20	mV
Ripple rejection ratio	Rrej	f = 120 Hz	V_{O1} – GND	1	40			dB
Temeprature coefficient of output voltage	$K\triangle V_{O1}/\triangle T$		V_{O1} – GND	1		±2		mV/°C
Reset ON voltage	V_{DNST}	* 1	Vlst – GND	1	0.85	0.95	1.10	V
Temeprature coefficient of reset ON voltage	$K\triangle V_{DNST}/\triangle T$		Vlst – GND	1		2.05		mV/°C
V1 reference voltage	V1ref		V1ref	1	1.1	1.2	1.3	V
Output current	IO		V10				10	mA

* Note 1) Voltage which appears during the operation of the reset circuit

Oscillation Section

Item	Symbol	Conditions	Applied pin	Test circuit	Min.	Typ.	Max.	Unit
Charging current at HC pin 1	$I_{HC}1$	Vcc = 6 V R6 = 33 kΩ	HC – GND	2	55	60	65	μA
Charging current at HC pin 2	$I_{HC}2$	Vcc = 3.8 V R6 = 33 kΩ	HC – GND	2	52.5	57.5	62.5	μA
Temperature coefficient of current at HC pin	$K\triangle I_{HC}/\triangle T$	0°C < Ta < 50°C Vcc = 6 V	HC – GND	2		±0.01		μA/°C
Oscillation frequency 1	f1	Vcc = 6 V * 2	HC – GND	3	10		17	KHz
Oscillation frequency 2	f2	Vcc = 3.8 V * 2	HC – GND	3	11		18	KHz
Threshold voltage	VthH	Vcc = 6 V * 2	HC – GND	3	0.7	0.9	1.1	V
Threshold voltage	VthL	Vcc = 6 V * 2	HC – GND	3			0.2	V
Synchronization pulse ON voltage	VON HST		HST – GND	3	3.0			V

* Note 2) R6 = 33 kΩ, C2 = 6800 pF

Error Amplifier Section

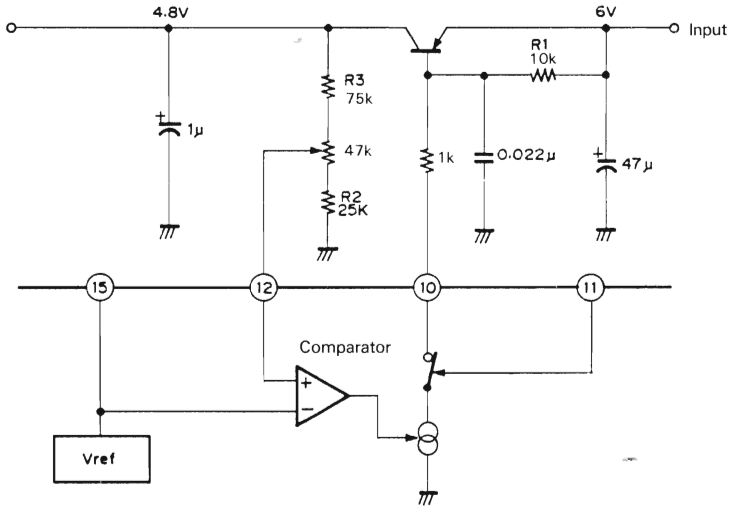
Item	Symbol	Conditions	Applied pin	Test circuit	Min.	Typ.	Max.	Unit
Offset voltage	V_{OP} OFFset	Vcc = 6V V_{OPIN^+} = 1.2 V	OP_{IN^+} – OP_{OUT}	4	–30		30	mV
Input bias current 1	$I_{B^+ OP}$		OP_{IN^+} – GND	2			1	μA
Input bias current 2	$I_{B^- OP}$		OP_{IN^-} – GND	2			1	μA
ON/OFF output saturation voltage	V_{5sat}	I_{O5} = 10 mA	$V_{ON/OFF}$ – GND				0.3	V
Zener voltage	V_Z	I_{IN} = 100μA	$V_{Z^+} - V_{Z^-}$		23.9	25.2	26.5	V

Dormant Period Adjustment Section

Item	Symbol	Conditions	Applied pin	Test circuit	Min.	Typ.	Max.	Unit
Bias current	IB Hduty		Hduty – GND	2			1	μA

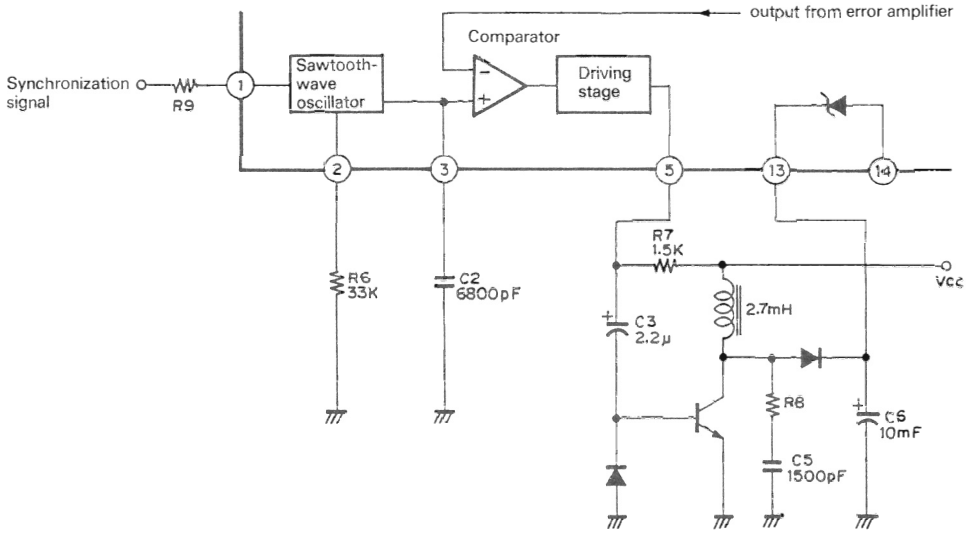
Description of Basic Operation

1) Series Regulator



The configuration of the series regulator is shown above. The main component is an external PNP transistor whose emitter works as an input pin and the collector as an output pin. The base is connected to pin 10, a current source inside the IC, and is controlled by a comparator. Current in the regulator decreases or increases depending on the high or low output levels of the comparator. Voltage at pin 15, a pin for inverting input to the comparator, is fixed to the reference voltage of 1.2 V. Pin 12 for non-inverting input supplies the output voltage which is split using resistors. Pin 11 for resetting operates at approx. 1 V to disconnect the power source.

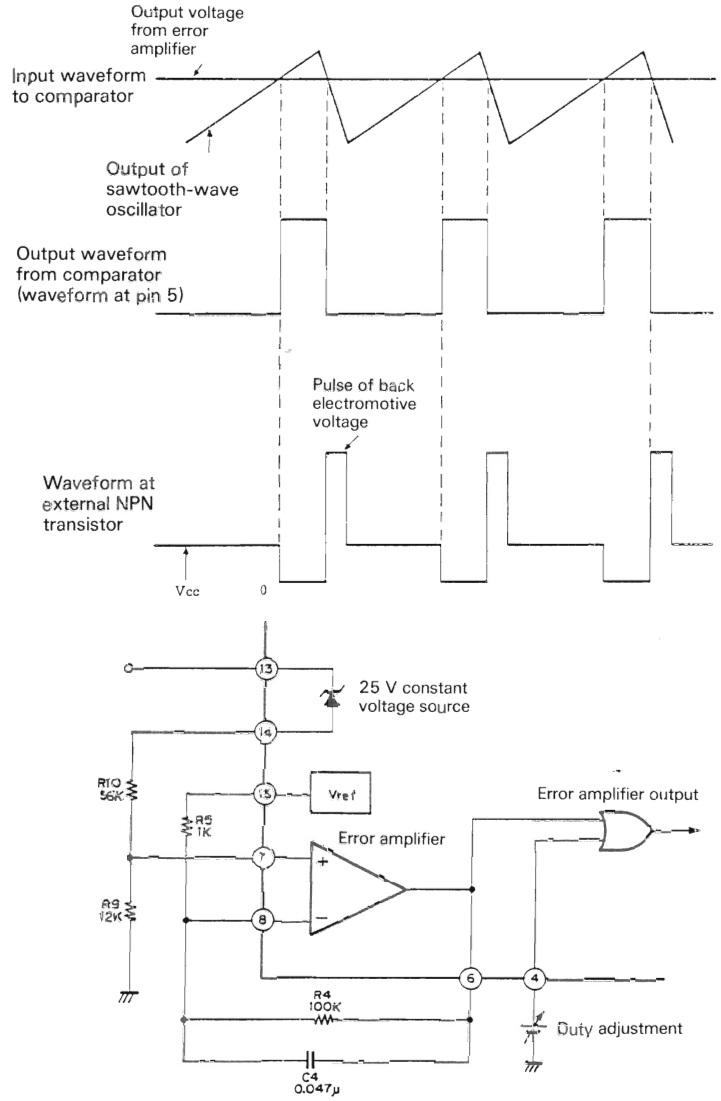
2) Switching Regulator



The following paragraph describes the operations of the oscillator, comparator and driving stage of the switching regulator with reference to the above drawing.

When a synchronization signal is input through pin 1 to generate a sawtooth wave, the wave is then converted into pulses according to the constants of the external resistor at pin 2 and the external capacitor at pin 3, and is output from pin 5 via the driving stage. Addition of this output to the base of an external NPN transistor, with an inductive load connected to the collector, results in back electromotive force being generated, which is then rectified to produce a high voltage. If the output voltage of the error amplifier is raised, the pulse width at pin 5 becomes narrower. Back electromotive force is consequently reduced to lower the output voltage.

3) Waveforms in Switching Regulator



The voltage detection section and control section of the switching regulator are shown here. The output voltage of the switching regulator (pin 13) is set to 32 V. A constant voltage source of 25 V is placed between pins 13 and 14, which gives 7 V at pin 14. This voltage is applied to pin 7, a pin for non-inverting input to the error amplifier, after being divided by resistors. Pin 8, a pin for inverting input to the error amplifier, is supplied with the reference voltage of 1.2 V (from pin 15) via resistor R5 (1 kΩ). Feedback resistor R4 (100 kΩ) is placed between pin 6, an output pin of the error amplifier, and pin 8 so that the gain of the error amplifier becomes 100. Cf is used to prevent oscillation.
Pin 4 is provided for adjusting the pulse width.

SONY CXA1011P/CXA1011M

dbx-TV Noise Reduction IC

Description

The CXA1011P/CXA1011M is an integrated circuit designed for the dbx-TV noise reduction decode circuit for the multichannel TV sound system. This device contains a voltage controlled amplifier, a variable de-emphasis circuit with new configuration and RMS detectors with completely integrated active band pass filters, and offers the complete integrated active band pass filter, and offers the complete dbx-TV noise reduction decoder only with a few external components.

Features

- Integrated band pass filters using active filtering technique and thin film structure with high capacitance
- Variable de-emphasis circuit with new circuit configuration
- Minimum number of external components
- Wide operation voltage range (4.7 to 16V)

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta=25°C)

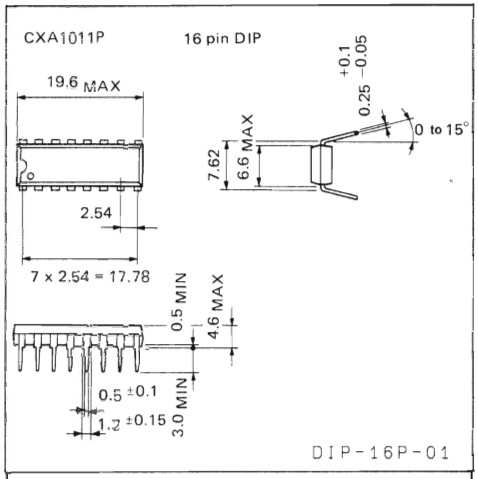
• Supply voltage	V_{CC}	17	V
• Operating temperature	Topr.	−20 to +75	°C
• Storage temperature	Tstg.	−55 to +150	°C
• Allowable power dissipation			
	P_D	CXA1011P 900	mW
	P_D	CXA1011M 500	mW

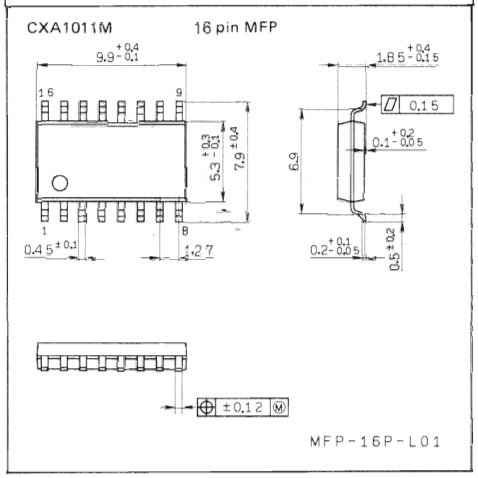
Recommended Operating Condition

• Supply voltage	V_{CC}	5 to 15	V

Package Outline

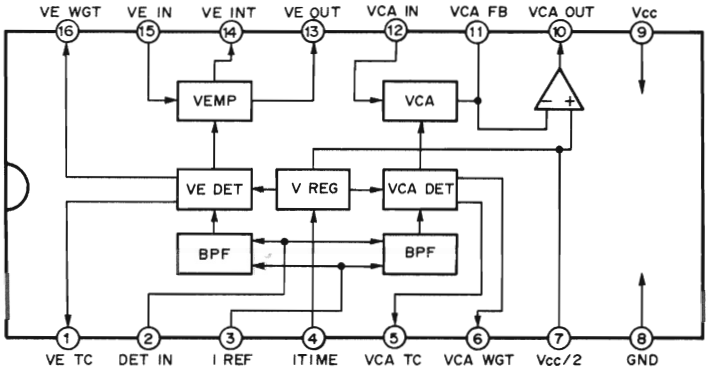
Unit: mm





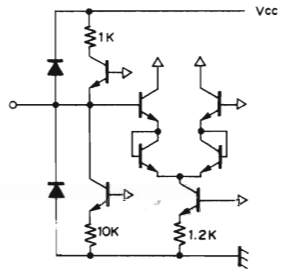
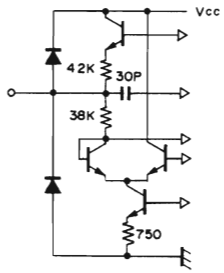
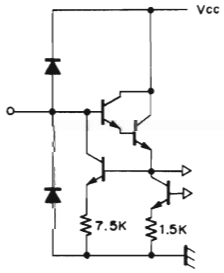
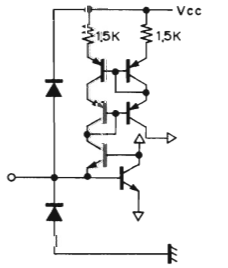
* This device is available only to the licensees of the dbx-TV noise reduction system.

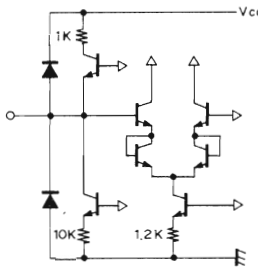
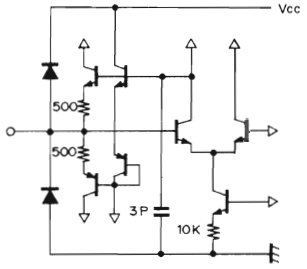
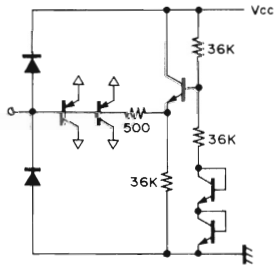
Block Diagram and Pin Configuration (Top View)

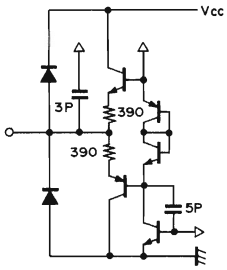
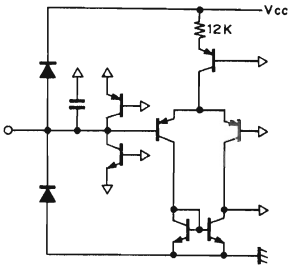
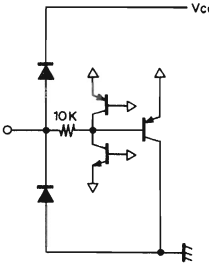
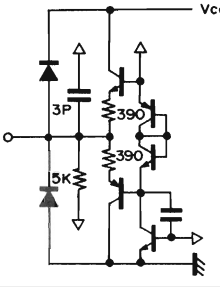


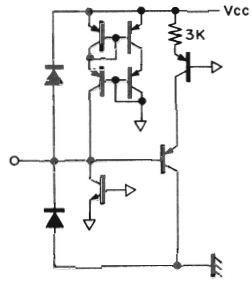
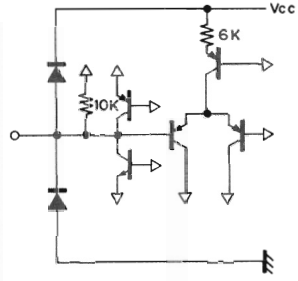
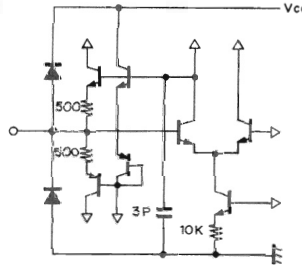
Pin Description (Ta=25°C Vcc=9V No Signal)

* Input Resistance
** Terminal DC Voltage

No.	Symbol	* RIN (Ω)	** DC(V)	Equivalent circuit	Description
1	VE TC	—	1.7		Time constant capacitor terminal of the RMS detector for the variable de-emphasis circuit. The specified attack and release time constants will be provided with 3.3 μF capacitor.
2	DET IN	20k	4.4		Input terminal of the band pass filters to weight the input signal for the RMS detectors.
3	IREF	—	2.7		Reference current input terminal for the band pass filters. The current will determine the cutoff frequencies of the band pass filters. The specified transfer characteristics will be provided with 560K resistor connected between Vcc terminal (pin 9) and this terminal.
4	ITIME	—	1.3		Timing current input terminal for the RMS detectors. The current will determine the attack and release time constants and will also determine the characteristics of the variable de-emphasis.

No.	Symbol	* RIN (Ω)	** DC(V)	Equivalent circuit	Description
5	VCA TC	—	1.7		Time constant capacitor terminal of the RMS detector for the voltage controlled amplifier. The specified attack and release time constant will be provided with 10 μF capacitor.
6	VCA WGT	low	4.5		Weighting impedance terminal of the RMS detector for the voltage controlled amplifier. The filter output signal will appear at the terminal. The RC series circuit connected to the terminal converts the signal from voltage to current which is the input current of the RMS detector. 15μArms input current will correspond to unity current gain of the voltage controlled amplifier. The pole frequency of the RC circuit will constitute the lower side cutoff frequency of the band pass filter and must have specified 35 Hz pole frequency.
7	Vcc/2	15k	4.5		Signal ground with half potential of the supply voltage Vcc. The capacitance connected the terminal will improve the supply rejection characteristics.
8	GND	—	0		Ground terminal.
9	Vcc	—	9.0		Power supply terminal.

No.	Symbol	* R_{IN} (Ω)	** DC(V)	Equivalent circuit	Description
10	VCA OUT	low	4.5		Output terminal of the voltage controlled amplifier stage. The decoded signal will obtain from this terminal.
11	VCA FB	low	4.5		Feedback terminal of the Voltage controlled amplifier output stage. The RC circuit connected between VCA OUT terminal (pin 10) and this terminal will converts the signal current from the voltage controlled amplifier cell to the output voltage and will provide fixed de-emphasis characteristics specified.
12	VCA IN	10k	4.5		Input terminal of the voltage controlled amplifier. The signal will be fed from VE OUT terminal (pin 13) via the coupling capacitor for rejection of the offset component.
13	VE out	low	4.5		Output terminal of the variable de-emphasis stage.

No.	Symbol	* RIN (Ω)	** DC(V)	Equivalent circuit	Description
14	VE INT	—	4.6		Terminal for integrating circuit of the variable de-emphasis stage. The variable de-emphasis characteristics will be determined with the RC series circuit connected externally. The values of 360Ω and 22 nF will be provide the specified transfer characteristics.
15	VE IN	low	4.5		Input terminal of the variable de-emphasis stage. This terminal provides the current input characteristic. The fixed de-emphasis network must be connected externally.
16	VE WGT	low	4.5		Weighting impedance terminal of the RMS detector for the variable de-emphasis circuit. The filter output signal will appear at the terminal. The RC series circuit connected to the terminal converts the signal from voltage to current which is input current of the RMS detector. 7.5 μArms input current will correspond to the flat response of the variable de-emphasis characteristics. The capacitance is only for rejection of the offset components.

Electrical Characteristics

See the Electrical characteristics Ta=25°C Vcc=+9V Reference level: 0 dB=−5 dBm (436 mVrms)

Characteristics	Symbol	Test condition			Min.	Typ.	Max.	Unit
		f(Hz)	Vi(dB)	Other				
Consumption current	Icc	—	—	no signal	4.0	5.0	6.3	mA
Decode characteristics								
300 Hz, −5 dB	V_{od}-1	300	−5		5.5	7.0	8.5	dB
300 Hz, −15 dB	V_{od}-2	300	−15		−14.5	−13.0	−11.5	dB
300 Hz, −30 dB	V_{od}-3	300	−30		−44.5	−43.0	−41.5	dB
1 kHz, 0 dB	V_{od}-4	1k	0		1.3	3.3	5.3	dB
1 kHz, −10 dB	V_{od}-5	1k	−10		−19.4	−17.4	−15.4	dB
1 kHz, −20 dB	V_{od}-6	1k	−20		−39.6	−37.6	−35.6	dB
8 kHz, 0 dB	V_{od}-7	8k	0		−4.3	−1.8	0.7	dB
8 kHz, −10 dB	V_{od}-8	8k	−10		−30.9	−28.4	−25.9	dB
8 kHz, −15 dB	V_{od}-9	8k	−15		−45.2	−42.7	−40.2	dB
VCA Filter characteristics				refer to 1 kHz				
3 kHz	V_{fp}-1	3k	0		−5.5	−4.0	−2.5	dB
8 kHz	V_{fp}-2	8k	0		−13.0	−11.0	−9.0	dB
V_{emp}. Filter characteristics				refer to 8 kHz				
5 kHz	V_{fg}-1	5k	0		−9.4	−7.4	−5.4	dB
2 kHz	V_{fg}-2	2k	0		−32.3	−28.8	−25.3	dB
Total harmonic distortion ratio	THD	1k	−3		—	0.1	0.3	%
Maximum output voltage				THD =1.5%				
300 Hz	V_{om}-1	300	—		11.0	15.0	—	dB
8 kHz	V_{om}-2	8k	—		−2.0	5.5	—	dB
Output noise level	V_{on}	—	—	A weight	—	−104	−80	dB
Timing current	I_{time}	—	—		7.1	7.5	7.9	μA
Center potential	$V_{cc}/2$	—	—		4.3	4.5	4.7	V

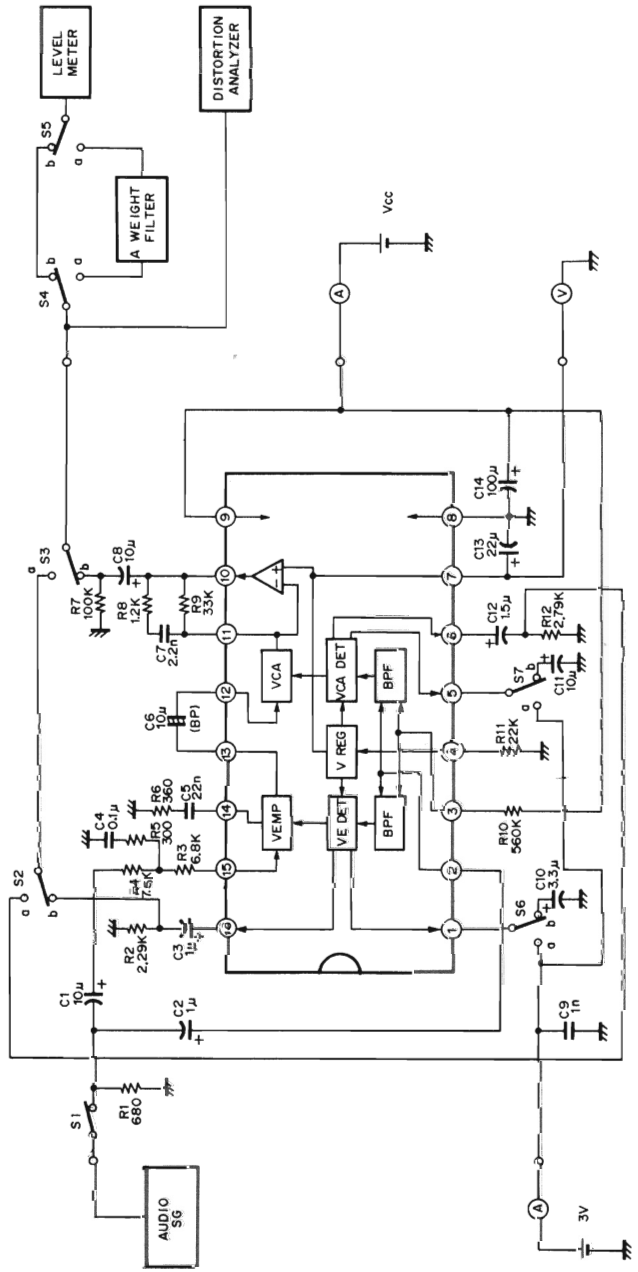
Electrical Characteristics

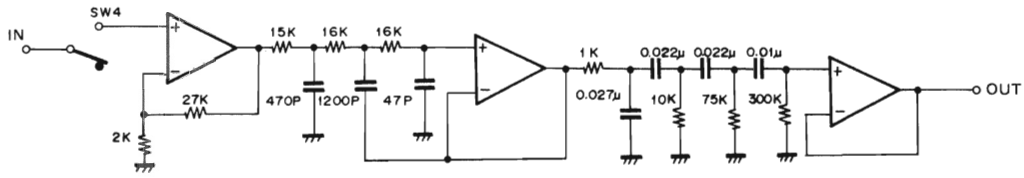
Ta=25°C, Vcc=+9V, Reference level: 0 dB=−5 dBm (436 mVrms)
See the Electrical characteristics

Item	Symbol	Switch condition						
		1	2	3	4	5	6	7
Consumption current	Icc	OFF	—	—	—	—	b	b
Decoding characteristics								
300 Hz, −5 dB	Vod-1	ON	—	b	b	b	b	b
300 Hz, −15 dB	Vod-2	ON	—	b	b	b	b	b
300 Hz, −30 dB	Vod-3	ON	—	b	b	b	b	b
1 kHz, 0 dB	Vod-4	ON	—	b	b	b	b	b
1 kHz, −10 dB	Vod-5	ON	—	b	b	b	b	b
1 kHz, −20 dB	Vod-6	ON	—	b	b	b	b	b
8 kHz, 0 dB	Vod-7	ON	—	b	b	b	b	b
8 kHz, −10 dB	Vod-8	ON	—	b	b	b	b	b
8 kHz, −15 dB	Vod-9	ON	—	b	b	b	b	b
VCA filter characteristics								
3 kHz	Vfp-1	ON	a	a	b	b	b	b
8 kHz	Vfp-2	ON	a	a	b	b	b	b
Vemp filter characteristics								
5 kHz	Vfg-1	ON	b	a	b	b	b	b
2 kHz	Vfg-2	ON	b	a	b	b	b	b
Total harmonic distortion ratio	THD	ON	—	b	b	b	b	b
Maximum output voltage								
300 Hz	Vom-1	ON	—	b	b	b	b	b
8 kHz	Vom-2	ON	—	b	b	b	b	b
Output noise level	Von	OFF	—	b	a	a	b	b
Middle point potential	Vcc/2	OFF	—	—	—	—	b	b
Timing current								
VCA detector	Itime-1	OFF	—	—	—	—	b	a
Vemp detector	Itime-2	OFF	—	—	—	—	a	b

Note) It suffices that a or b is inserted into (−).

Electrical Characteristics Measuring Circuit

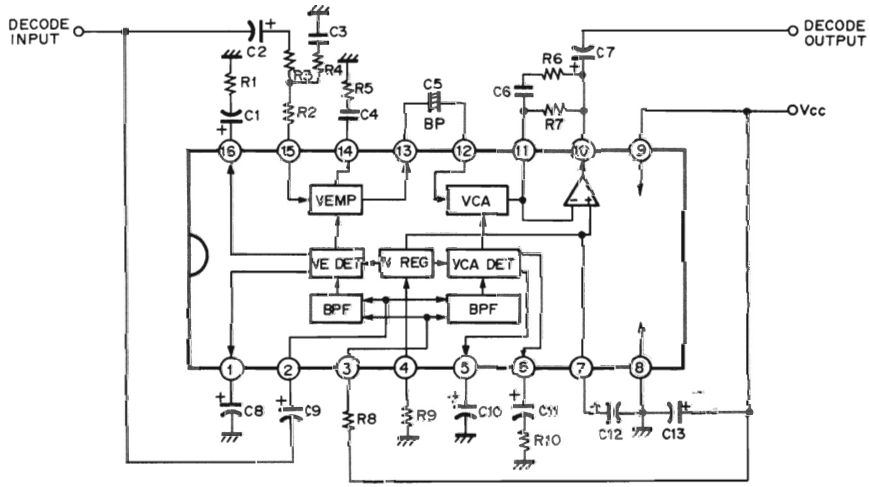




"A" Weighting Filter Circuit (20 dB Gain)

Description of Operation

(1) dbx-TV decoder characteristics



Basic Application Circuit

*1 The figure of basic application circuit shows the dbx-TV NR decode circuit using the CXA1011P/CXA1011M. The input signal is fed to the variable de-emphasis circuit through the fixed de-emphasis circuit which is composed of R2 to R4, C2 and C3. The output signal is fed to VCA through C5. The signal current from VCA is converted to the output voltage by an operational amplifier, which has the other fixed de-emphasis circuit composed of R6, R7 and C6, and then the output signal is obtained as the decoded signal.

The transfer function of the variable de-emphasis and the gain of VCA are controlled by their individual RMS detectors.

*2 The individual RMS detectors give predetermined weighting characteristics to the input signal through the band pass filters, and detect the signals of RMS value and obtain the control signal.

*1. The dbx-TV NR decode circuit using of CXA1011P/CXA1011M is shown above.

*2. In the individual RMS detectors, the input signal is given the specified weighting characteristics by the band pass filters, and converts to the RMS values, which are control signals of the variable de-emphasis circuit and VCA.

(2) Description of system block

1 Variable de-emphasis circuit
The variable de-emphasis circuit is an amplifier with variable high frequency response controlled by the control signal of the RMS detector for the variable de-emphasis.
Characteristics of the variable de-emphasis determined by the RC series circuit of VE INT terminal (pin 14) and the current of ITIME terminal (pin 4).

2 VCA circuit
VCA is a variable gain amplifier controlled by the control signal of the RMS detector for VCA.

3 RMS detector for the variable de-emphasis circuit
The RMS detector for the variable de-emphasis circuit detects RMS value of the current flowing in VE WGT terminal (pin 16) and control the variable de-emphasis circuit.
The input current which gives flat response to the variable de-emphasis characteristics is the reference input current of the RMS detector, and the current is designed to 7.5μArms in this IC.
The specified attack and release time constants are determined by the capacitor of VE TC terminal (pin 1).

4 RMS detector for VCA
The RMS detector for VCA detects RMS value of the current flowing in the VCA WGT terminal (pin 6) and controls gain of VCA.
The input current which gives unity current gain to VCA is the reference input current of the RMS detector, and the current is designed to 15μArms in this IC.
The specified attack and release time constants are determined by the capacitor of VCA TC terminal (pin 5).

5 Band pass filter for the variable de-emphasis
The band pass filter for the variable de-emphasis is formed by an integrated active filter which is series circuit of 2nd order lowpass filter (f_o=20 kHz, Q=0.69) 2nd order high pass filter (f_o=7.66 kHz, Q=0.95) and 1st order high pass filter (f_o=3.92 kHz).
The transfer characteristics of the band pass filter is determined by the reference current flowing in IREF terminal (pin 3).

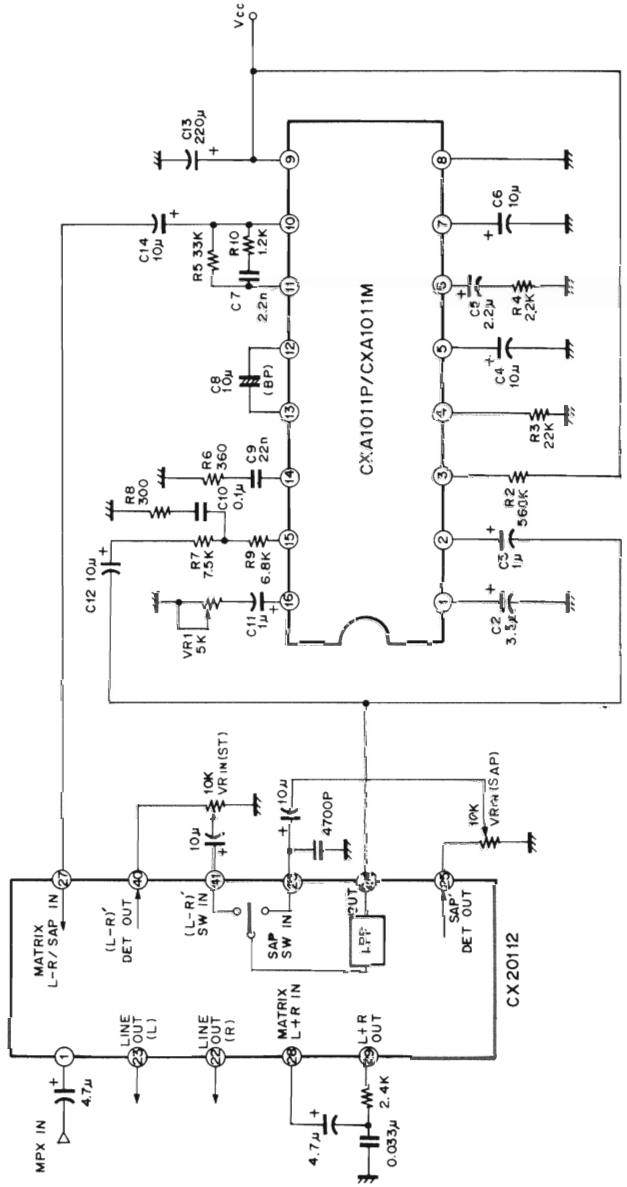
6 Band pass filter for VCA
The band pass filter for VCA is formed by the integrated active filter of 1st order low pass filter and the RC series circuit connected to VCA WGT terminal.
The cutoff frequency of the filter is determined by the reference current flowing in IREF terminal (pin 3) as the cutoff frequencies of the variable de-emphasis filter.

(3) Application circuit for multichannel television sound decoder
This application circuit is multichannel television sound decoder using the CX20112 for multiplexing sound de-modulator IC and the CXA1011P/CXA1011M for the dbx-TV NR IC.
The calibration of the processor, which has a switchable dbx-TV NR processor for stereo and SAP mode, is as follows. For calibration, Multichannel television sound encoder and two input signals for the encoder need.

	frequency	input level (refer to the encoder reference level)	dbx-TV Encoder
Signal 1	400 Hz	−10 dB	ON
Signal 2	2 kHz	−10 dB	ON

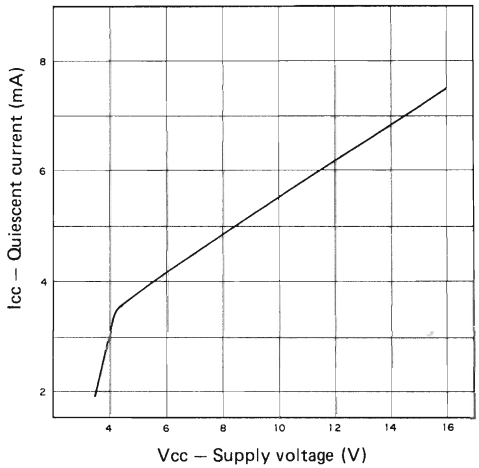
1. Adjust VR1 to mechanical center.
2. Set the stereo mode, connect signal 1 (freq=400 Hz, −10 dB) to left channel input of the multichannel television sound encoder. At this point, adjust VRin (ST) so that the matrix output level of right channel becomes minimum.
3. Change the input signal to signal 2 (freq=2 kHz, −10 dB), at this point, adjust VR1 so that the matrix output level of right channel becomes minimum.
4. Change the input signal to signal 1 again. At this point, adjust VRin (ST) so that the matrix output level of right channel becomes minimum.
5. Measures the output level (pin 10 of CXA1011P/CXA1011M), and record the level.
6. Repeat step 3.
7. Change to SAP mode and connect signal 1 to SAP input of the encoder, adjust VRin (SAP) so that the output level (pin 10 of CXA1011P/CXA1011M) becomes same as the recorded level of step 5.

Audio Multiplexing Decoder Application Circuit

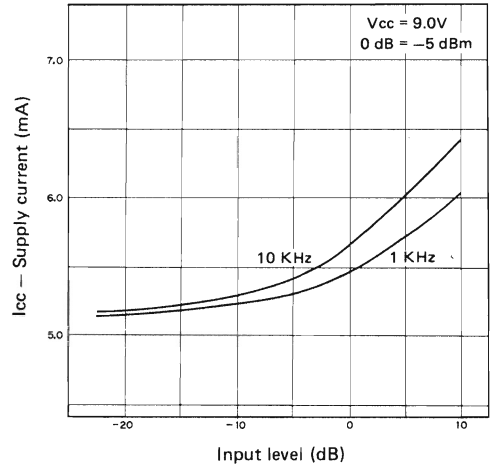


R2, R3 Metal film resistor
C2, C4 Tantalum capacitor (± 5%)
C7, C9, C10 PP capacitor or Mylar capacitor (± 5%)
C5 ± 10% capacitor

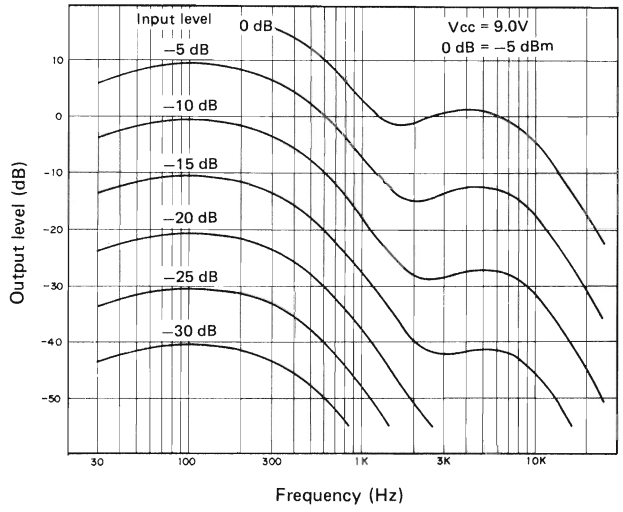
Quiescent current vs. Supply voltage



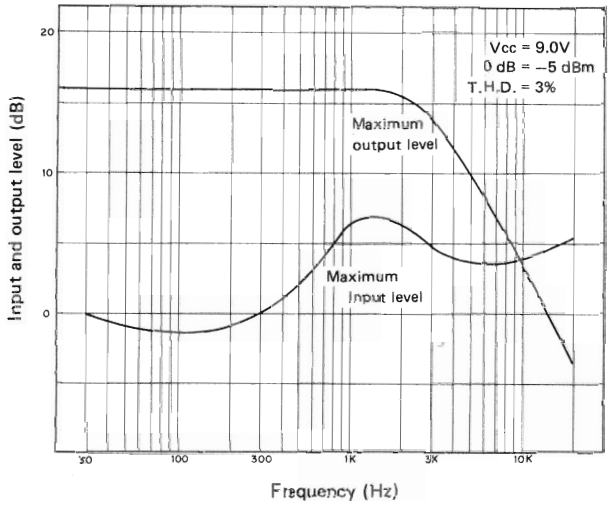
Supply current vs. Input level



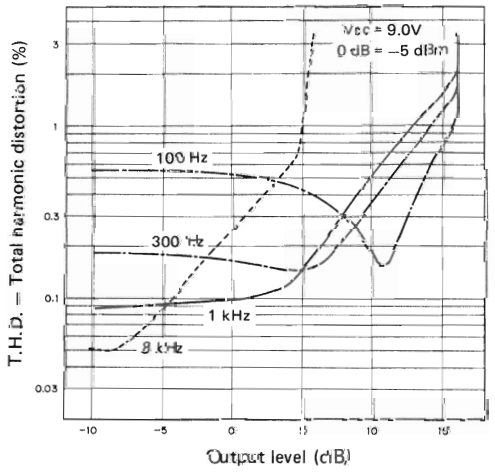
Decode characteristics



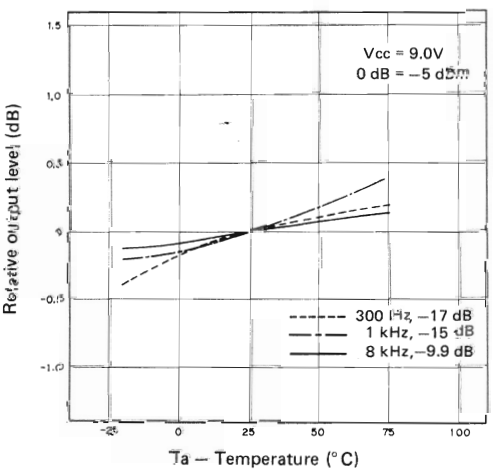
Maximum output and input level



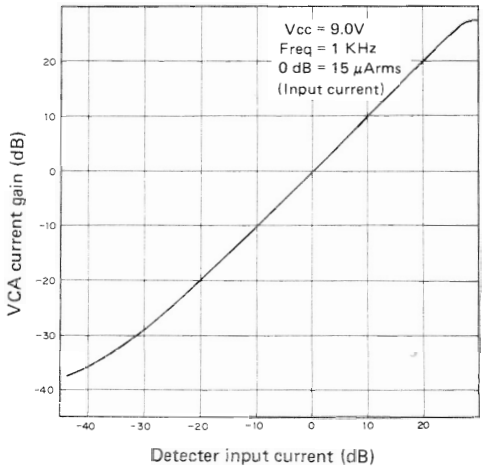
Total harmonic distortion



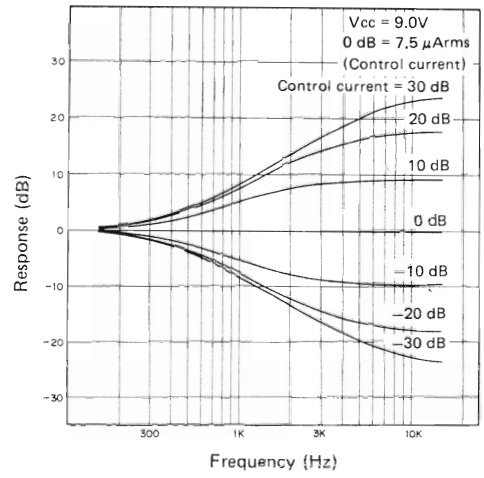
Temperature characteristics



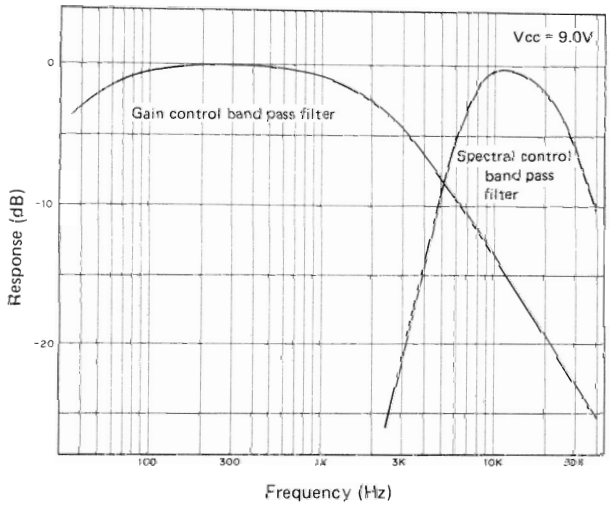
VCA control characteristics



Variable de-emphasis characteristics



Band pass filter frequency response



RGB Interface, Automatic White Balance

Description

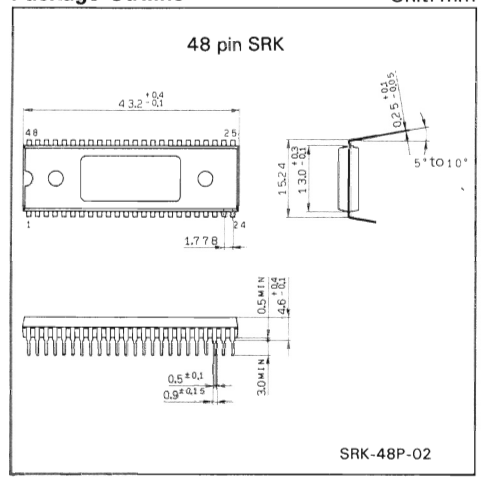
The CXA1024S is a bipolar IC designed for the RGB interface and AWB (Automatic White Balance) adjustment of televisions and color displays.

With the RGB interface a high quality audio-visual TV can be constructed with fewer components.

AWB executes the CRT cutoff and drive adjustment automatically. It also compensates for any discolouring through usage to keep the original white changes.

Package Outline

Unit: mm



Features

- 9V single power supply operation
- Conforms to EIAJ standards
- High-speed switching of YS and YM
- Several inputs (3 inputs and on-screen display input)

Functions

- AWB, automatic cutoff
- RGB interface
- TV RGB input clamp, linear RGB input clamp
- Picture control, brightness control
- Blanking, power-on mute

Structure

Bipolar silicon monolithic IC

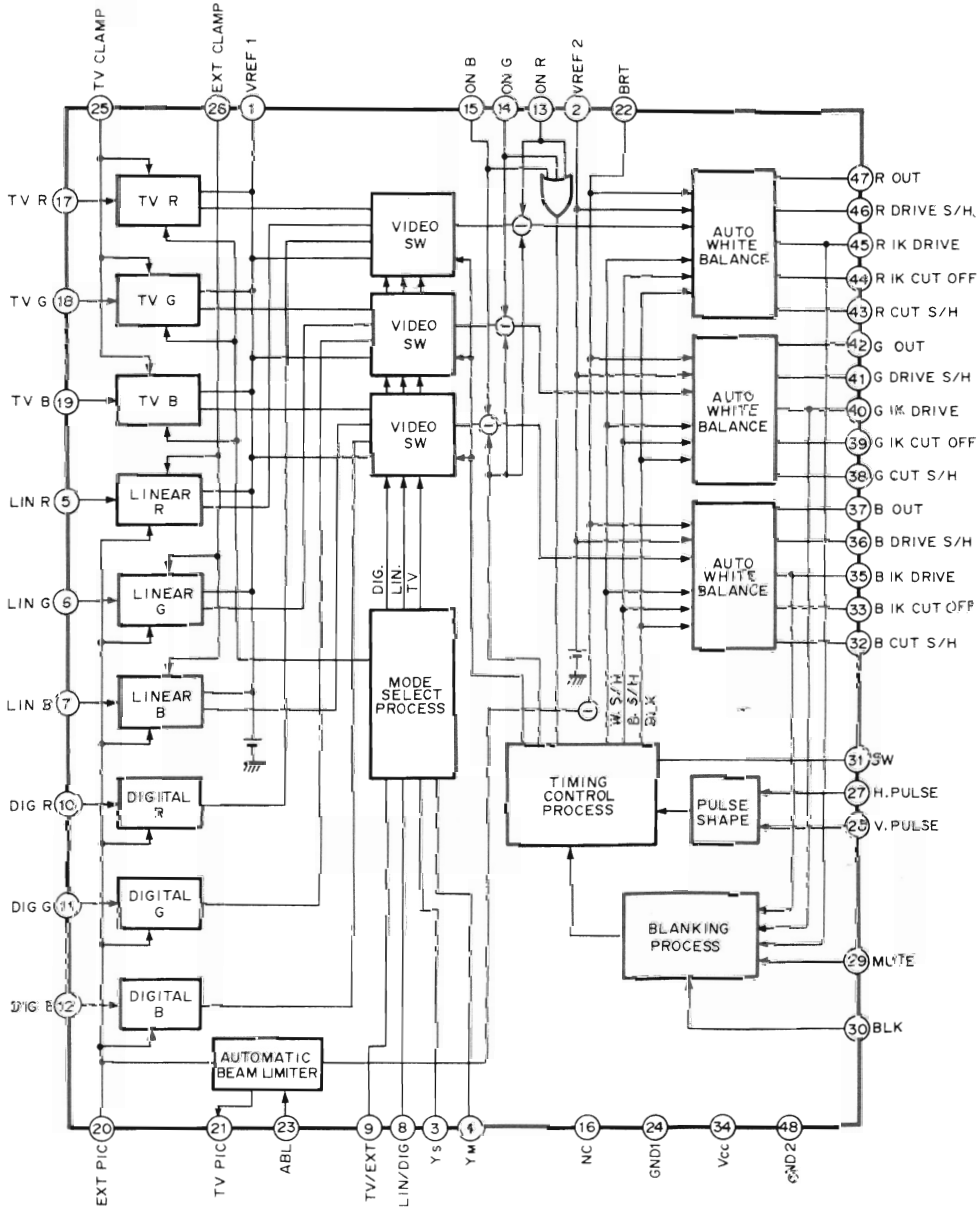
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	17	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	1.9	W

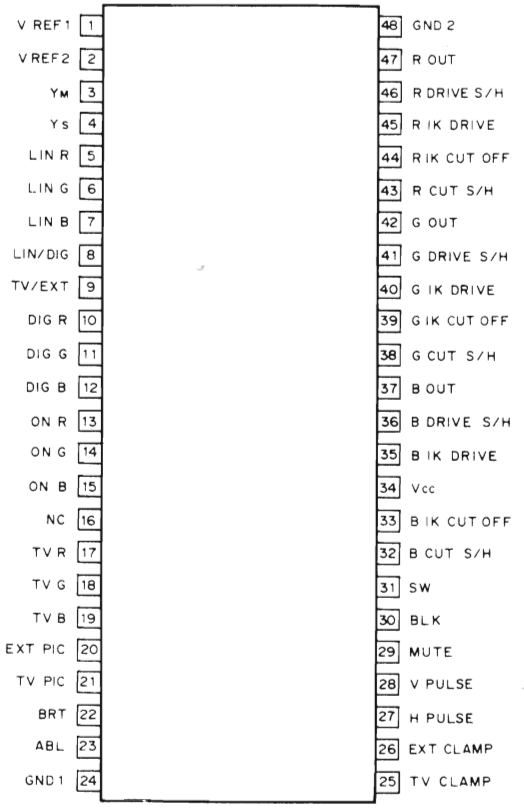
Recommended Operating Conditions

• Supply voltage	Vcc	9.0	V
• Operating range	Vcc	8.0 to 10.0	V

Block Diagram



Pin Configuration (Top View)

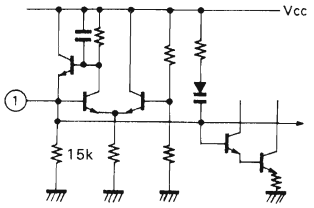
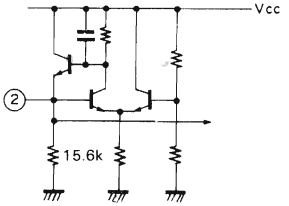
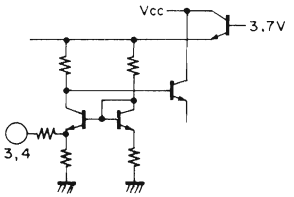
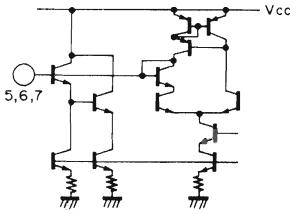
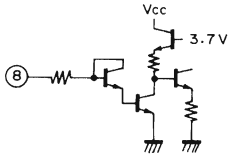
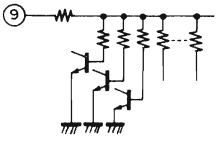


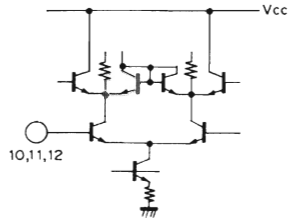
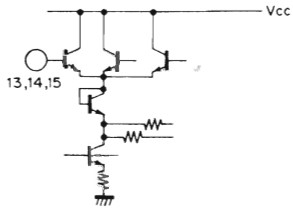
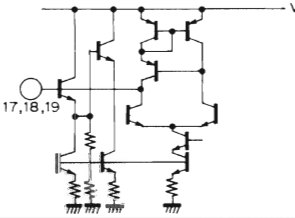
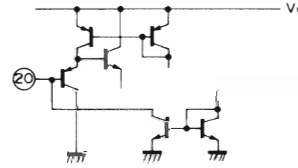
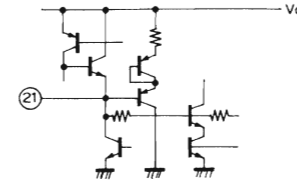
I/O Truth Table

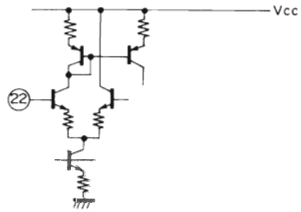
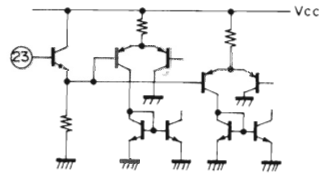
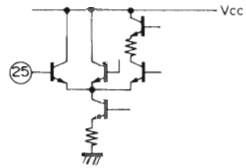
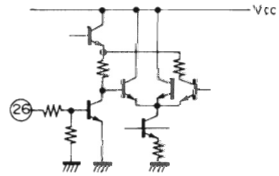
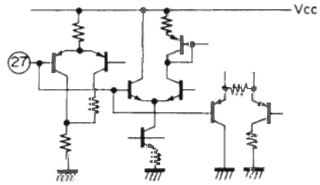
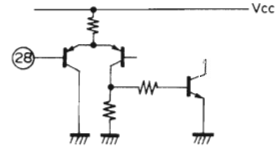
TV/EXT	H	L			
LIN/DIG	X	H			L
YS	X	L		H	X
YM	X	L	H	X	X
Control / Mode	TV	TV	TV −6 dB	LIN	DIG

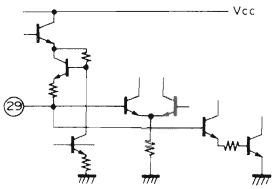
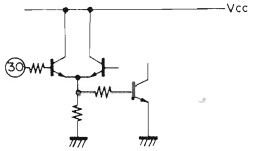
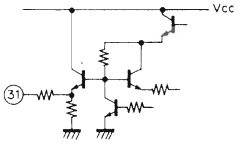
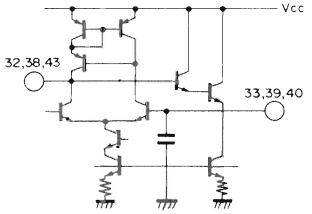
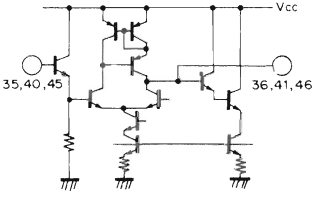
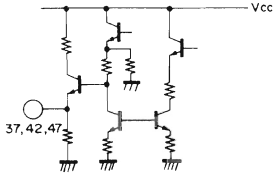
LIN : Linear
DIG : Digital

Pin Description

No.	Symbol	Equivalent circuit	Description
1	V REF1		Clamp reference voltage
2	V REF2		Detection reference voltage
3 4	YM YS		Pin 3: YM switch control pin Pin 4: YS switch control pin
5 6 7	LIN R LIN G LIN B		R, G, B signal input pin for linear input mode
8	LIN/DIG		Switching control pin for linear input mode and digital input mode
9	TV/EXT		Switching control pin for TV input mode and External input mode (Linear Digital)

No.	Symbol	Equivalent circuit	Description
10 11 12	DIG R DIG G DIG B		R, G, B signal input pin for digital input mode
13 14 15	ON R ON G ON B		R, G, B signal input pin for On-Screen display (CRT display)
16	NC		Open pin, Ground
17 18 19	TV R TV G TV B		R, G, B signal input pin for TV input mode
20	EXT PIC		Picture control pin for External signal (Linear, Digital)
21	TV PIC		External picture control DC with ABL (Automatic Beam Limiter). Can be input to the Y/C IC PIC pin.

No.	Symbol	Equivalent circuit	Description
22	BRT		Brightness control pin
23	ABL		Lowers gain of picture or brightness according to ABL input (Automatic Beam Limiter) DC. PIC ABL : Less than 4.5V BRT ABL : Less than 2.0V
24	GND1		Ground pin
25	TV CLAMP		Clamp timing pulse input pin of the TV input pin
26	Ext CLAMP		Clamp timing pulse input pin of the Linear input pin
27	H PULSE		Horizontal pulse input pin
28	V PULSE		Vertical pulse input pin

No.	Symbol	Equivalent circuit	Description
29	MUTE		Determines the mute time when Power is ON by means of an external capacitor.
30	BLK		Blanking pin for internals of the entire signal
31	SW		ON/OFF output pin for the weighted resistance of drive Ik.
32 38 43	B CUT S/H G CUT S/H R CUT S/H		External capacitor pin for sampling hold of the cut-off control
33 39 44	B IK CUT OFF G IK CUT OFF R IK CUT OFF		Ik input pin. Controls the signal output cutoff by comparing this signal with the internal reference voltage. (Vref 3.0V)
35 40 45	B IK DRIVE G IK DRIVE R IK DRIVE		Ik input pin. Controls the signal output drive by comparing this signal with the internal reference voltage. (Vref 3.0V)
36 41 46	B DRIVE S/H G DRIVE S/H R DRIVE S/H		External capacitor pin for sampling hold of the drive control.
37 42 47	B OUT G OUT R OUT		R, G, B output pins.
34	Vcc		Power supply pin
48	GND2		Ground pin

Electrical Characteristics

Ta = 25°C Vcc = 9V See the Electrical Characteristics Test Circuit

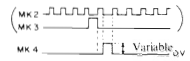
Test No.	Test item	Symbol	SW setting to ON	Bias condition (V) V1	V2	V3	VS1	VS2	VS3	VS4	VS5	VS6	VS7	Composit In and Markers	Test point	Description of output waveforms and test method	Min.	Typ.	Max.	Unit
1	Current consumption	I_{CC}		9.0		9.0	0	0	9.0	4.5	6.0	0	4.0				50.0	75.0	100.0	mA
2	Black detection voltage (R)	RV_B	A11 C1 C9 C10		9.0	↓	↓	↓	↓	↓	↓	↓	↓	MK1 9V 0V MK2 9V 0V MK3	VM3	Output waveform	2.90	3.05	3.20	V
	Black detection voltage (G)	GV_B	A12 C2 C7 C8		↓	↓	↓	↓	↓	↓	↓	↓	↓							
	Black detection voltage (B)	BV_B	A13 C3 C5 C6		↓	↓	↓	↓	↓	↓	↓	↓	↓							
3	Black detection voltage correlation	ΔV_{B1}														ΔV_{B1} $RV_B - GV_B$				
	Black detection voltage correlation	ΔV_{B2}														ΔV_{B2} $GV_B - BV_B$	−10.0	0.0	10.0	mV
	Black detection voltage correlation	ΔV_{B3}														ΔV_{B3} $BV_B - RV_B$				
4	White detection voltage (R)	RV_W	C1 C9 C10		↓	↓	↓	↓	↓	↓	↓	↓	↓		VM1		3.65	3.80	3.95	V
	White detection voltage (G)	GV_W	C2 C7 C8		↓	↓	↓	↓	↓	↓	↓	↓	↓							
	White detection voltage (B)	BV_W	C3 C5 C6		↓	↓	↓	↓	↓	↓	↓	↓	↓							
5	White detection voltage correlation	ΔV_{W1}														ΔV_{W1} $RV_W - GV_W$				
	White detection voltage correlation	ΔV_{W2}														ΔV_{W2} $GV_W - BV_W$	−25.0	0.0	25.0	mV
	White detection voltage correlation	ΔV_{W3}														ΔV_{W3} $BV_W - RV_W$				
6	BLK detection level (R)	RV_{BLK}	A11 C1 C9 C10		↓	↓	↓	↓	↓	↓	↓	↓	↓		VM3		0.54	0.64	0.74	V
	BLK detection level (G)	GV_{BLK}	A12 C2 C7 C8		↓	↓	↓	↓	↓	↓	↓	↓	↓							
	BLK detection level (B)	BV_{BLK}	A13 C3 C5 C6		↓	↓	↓	↓	↓	↓	↓	↓	↓							
7	BLK detection level correlation	ΔV_{BLK1}														ΔV_{BLK1} $RV_{BLK} - GV_{BLK}$				
	BLK detection level correlation	ΔV_{BLK2}														ΔV_{BLK2} $GV_{BLK} - BV_{BLK}$	−10.0	0.0	10.0	mV
	BLK detection level correlation	ΔV_{BLK3}														ΔV_{BLK3} $BV_{BLK} - RV_{BLK}$				
8	Minimum black level (R)	$RV_{B\,min}$	C10 C11		↓	↓	↓	↓	↓	↓	8.0	↓	↓		VM2		0.75	1.25	1.75	V
	Minimum black level (G)	$GV_{B\,min}$	C8 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓							
	Minimum black level (B)	$BV_{B\,min}$	C6 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓							
9	Maximum black level (R)	$RV_{B\,max}$	C10 C11		↓	↓	↓	↓	↓	↓	2.0	↓	↓		VM2		3.95	4.30	4.65	V
	Maximum black level (G)	$GV_{B\,max}$	C8 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓							
	Maximum black level (B)	$BV_{B\,max}$	C6 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓							
10	Minimum white amplitude (R)	$RV_{W\,min}$	C10 C12		↓	↓	↓	↓	↓	↓	8.0	↓	↓		VM2		0.75	0.95	1.15	V
	Minimum white amplitude (G)	$GV_{W\,min}$	C8 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓							
	Minimum white amplitude (B)	$BV_{W\,min}$	C6 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓							
11	Maximum white amplitude (R)	$RV_{W\,max}$	C10 ↓		↓	↓	↓	↓	↓	↓	2.0	↓	↓		VM2		1.75	2.05	2.35	V
	Maximum white amplitude (G)	$GV_{W\,max}$	C8 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓							
	Maximum white amplitude (B)	$BV_{W\,max}$	C6 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓							

Test No.	Test item	Symbol	SW setting to ON	Bias condition (V) V1	V2	V3	VS1	VS2	VS3	VS4	VS5	VS6	VS7
12	Output BLK level (R)	R_{OL}	C1 C9 C10		9.0	9.0	0	0	9.0	4.5	6.0	0	4.0
	Output BLK level (G)	G_{OL}	C2 C7 C8		↓	↓	↓	↓	↓	↓	↓	↓	↓
	Output BLK level (B)	B_{OL}	C3 C5 C6		↓	↓	↓	↓	↓	↓	↓	↓	↓
13	V pulse threshold	V_{TH9}	C1 C10		↓	↓	↓	↓	↓	↓	0	0	4.5
14	N.H. pulse threshold	NH_{TH9}	↓ ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓
15	BLK threshold	BLK_{TH9}	↓ ↓ B16		↓	↓	↓	↓	↓	↓	↓	Variable	↓
16	Mute threshold	M_{TH9}	↓ ↓ B15		↓	↓	↓	↓	↓	↓	↓	↓	↓
17	Clamp reference voltage	VREF1	↓ ↓		↓	↓	↓	↓	↓	↓	↓	0	↓
18	Detection reference voltage	VREF2	↓ ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓
19	TV input dynamic range (R)	RV_{TVD}	B8 C10		↓	↓	2.0	2.0	↓	↓	2.0	↓	↓
	TV input dynamic range (G)	GV_{TVD}	B10 C8		↓	↓	↓	↓	↓	↓	↓	↓	↓
	TV input dynamic range (B)	BV_{TVD}	B12 C6		↓	↓	↓	↓	↓	↓	↓	↓	↓
20	TV gain (R)	RG_{TV}	B10 C		↓	↓	↓	↓	↓	↓	↓	↓	↓
	TV gain (G)	GG_{TV}	B10 C8		↓	↓	↓	↓	↓	↓	↓	↓	↓
	TV gain (B)	BG_{TV}	B12 C6		↓	↓	↓	↓	↓	↓	↓	↓	↓
21	TV gain correlation	ΔG_{TV1}			↓	↓	↓	↓	↓	↓	↓	↓	↓
	TV gain correlation	ΔG_{TV2}											
	TV gain correlation	ΔG_{TV3}											
22	Y_M Suppress (R)	RG_{YM}	A2 B8 C10 A3		↓	↓	↓	0	↓	↓	↓	↓	↓
	Y_M Suppress (G)	GG_{YM}	↓ B10 C8 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓
	Y_M Suppress (B)	BG_{YM}	↓ B12 C6 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓
23	YM supress correlation	ΔG_{YM1}											
	YM supress correlation	ΔG_{YM2}											
	YM supress correlation	ΔG_{YM2}											
24	YM threshold	V_{YM}	↓ B8 C10 ↓		↓	↓	↓	↓	↓	↓	↓	↓	Variable
25	YM pulse response (R)	RT_{YM}	A1 ↓ ↓ A4		↓	↓	↓	↓	↓	↓	↓	↓	0
	YM pulse response (G)	GT_{YM}	↓ B10 C8 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓
	YM pulse response (B)	BT_{YM}	↓ B12 C6 ↓		↓	↓	↓	↓	↓	↓	↓	↓	↓
26	TV black level (R)	RB_{TV}	↓ B8 C10		↓	↓	↓	2.0	↓	↓	↓	↓	4.5
	TV black level (G)	GB_{TV}	↓ B10 C8		↓	↓	↓	↓	↓	↓	↓	↓	↓
	TV black level (B)	BB_{TV}	↓ B12 C6		↓	↓	↓	↓	↓	↓	↓	↓	↓
27	TV clamp threshold	CV_{TV}	A16 B14 C10		↓	↓	↓	↓	↓	↓	↓	↓	↓

Composit In and Markers

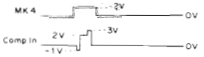
No change in MK1 to MK3 from preceding page.

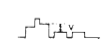
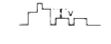
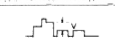
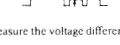
No change in MK1 to MK3



No change in MK1 to MK4 (However, MK4 amplitude is 2Vp-p)

No change in MK1 to MK4

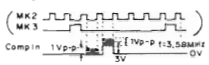


Test point	Description of output waveforms and test method	Min.	Typ.	Max.	Unit
VM2				50	mV
VM2	Threshold of V pulse (MK1) amplitude	2.80	3.00	3.20	V
VM2	Threshold of N.H. pulse (MK2) amplitude	6.90	7.08	7.35	V
VM2	BLK threshold voltage	1.25	1.50	1.75	V
VM2	Mute threshold voltage	3.70	3.85	4.00	V
MP2	DC test	3.50	3.65	3.80	V
MP3	DC test	2.95	3.05	3.15	V
VM2	 Input amplitude when the output gain decreases by 1 dB for the input waveform (MK4)	3.5	3.6		V
VM2	 Measure V for gain with the input waveform (MK4) amplitude at 2 Vp-p	−5.5	−4.0	−2.5	dB
	ΔG_{TV1} $RG_{TV}-GG_{TV}$ ΔG_{TV2} $GG_{TV}-BG_{TV}$ ΔG_{TV3} $BG_{TV}-RG_{TV}$	−1.5	0.0	1.5	dB
VM2	 Measure V, calculate gain for an external G_v and obtain the difference from TV gain. G_{YM} $G-G_{TV}$	−6.25	−6.05	−5.85	dB
	ΔG_{YM1} $RG_{YM}-GG_{YM}$ ΔG_{YM2} $GG_{YM}-BG_{YM}$ ΔG_{YM3} $BG_{YM}-RG_{YM}$	−0.4	0.0	0.4	dB
	YM threshold voltage	0.50	0.66	0.90	V
VM2	Average value of the time difference (rise and fall)		33	50	ns
VM2	 Measure the voltage difference V	90	275	460	mV
MP6	TV clamp threshold voltage	1.65	1.85	2.05	V

Test No.	Test item	Symbol	SW setting to ON								Bias condition (V)									
											V1	V2	V3	VS1	VS2	VS3	VS4	VS5	VS6	VS7
28	TV DG (R)	RD_{TV}	B 7	C 10								9.0	9.0	2.0	2.0	9.0	4.5	2.0	0	4.5
	TV DG (G)	GD_{TV}	B 9	C 8								↓	↓	↓	↓	↓	↓	↓	↓	↓
	TV DG (B)	BD_{TV}	B 11	C 6								↓	↓	↓	↓	↓	↓	↓	↓	↓
29	TV frequency response (R)	Rf_{TV}	A 14	B 7	B 15	C 10						↓	↓	↓	↓	↓	↓	↓	↓	↓
	TV frequency response (G)	Gf_{TV}	↓	B 9	↓	C 8						↓	↓	↓	↓	↓	↓	↓	↓	↓
	TV frequency response (B)	Bf_{TV}	↓	B 11	↓	C 6						↓	↓	↓	↓	↓	↓	↓	↓	↓
30	TV input channel crosstalk	CT_{1RG}	A 14	B 8	B 9	B 12	B 15	C 10				↓	↓	↓	0	↓	↓	↓	↓	↓
		CT_{1GB}	↓	↓	↓	↓	↓	C 6				↓	↓	↓	↓	↓	↓	↓	↓	↓
31	Mode crosstalk (TV→LIN)	CT_{2R}	A 4	A 6	A 8	A 10	A 14	B 7	B 15	C 10		↓	↓	↓	↓	↓	↓	↓	↓	↓
		CT_{2G}	↓	↓	↓	↓	↓	B 9	↓	C 8		↓	↓	↓	↓	↓	↓	↓	↓	↓
		CT_{2B}	↓	↓	↓	↓	↓	B 11	↓	C 6		↓	↓	↓	↓	↓	↓	↓	↓	↓
32	Mode crosstalk (TV→DIG)	CT_{3R}					↓	B 7	↓	C 10		↓	↓	0	↓	↓	↓	↓	↓	↓
		CT_{3G}					↓	B 9	↓	C 8		↓	↓	↓	↓	↓	↓	↓	↓	↓
		CT_{3B}					↓	B 11	↓	C 6		↓	↓	↓	↓	↓	↓	↓	↓	↓
33	LIN. input dynamic range (R)	RV_{LD}	A 4	A 6	C 10	C 11	C 12					↓	↓	2.0	↓	↓	↓	↓	↓	↓
	LIN. input dynamic range (G)	GV_{LD}	↓	A 8	C 8	↓	↓					↓	↓	↓	↓	↓	↓	↓	↓	↓
	LIN. input dynamic range (B)	BV_{LD}	↓	A 10	C 6	↓	↓					↓	↓	↓	↓	↓	↓	↓	↓	↓
34	PIC.AMP.GAIN MAX (R)	$RG_{L\,max}$	↓	A 6	C 10							↓	↓	↓	↓	↓	↓	↓	↓	↓
	PIC.AMP.GAIN MAX (G)	$GG_{L\,max}$	↓	A 8	C 8							↓	↓	↓	↓	↓	↓	↓	↓	↓
	PIC.AMP.GAIN MAX (B)	$BG_{L\,max}$	↓	A 10	C 6							↓	↓	↓	↓	↓	↓	↓	↓	↓
35	PIC.AMP.GAIN MAX correlation	$\Delta G_{L\,max\,1}$																		
	PIC.AMP.GAIN MAX correlation	$\Delta G_{L\,max\,2}$																		
	PIC.AMP.GAIN MAX correlation	$\Delta G_{L\,max\,3}$																		
36	PIC.AMP.GAIN MIN (R)	$RG_{L\,min}$	↓	A 6	C 10							↓	↓	↓	↓	0.3	↓	↓	↓	↓
	PIC.AMP.GAIN MIN (G)	$GG_{L\,min}$	↓	A 8	C 8							↓	↓	↓	↓	↓	↓	↓	↓	↓
	PIC.AMP.GAIN MIN (B)	$BG_{L\,min}$	↓	A 10	C 6							↓	↓	↓	↓	↓	↓	↓	↓	↓

Composit In and Markers

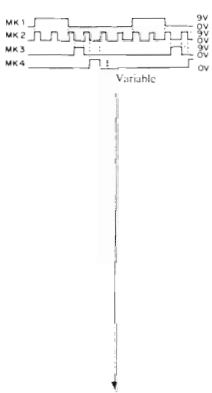
No change in MK1 to MK3



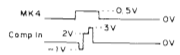
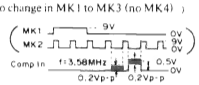
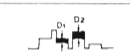
- MK1, MK4→GND
- MK2

RF IN : CW of 1Vp-p,
- 500 kHz, 200 MHz

RF IN : 3.58MHz, 3.0Vp-p



Test point	Description of output waveforms and test method	Min.	Typ.	Max.	Unit
VM2	$\frac{D_1 - D_2}{D_1} \times 100$ %			20	%
RF VM1	Gain difference at 500 kHz to 20 MHz	−5.0	−3.0	0.0	dB
RF VM1	R and B output ratios against the G output $CT_1 = 20 \log \frac{V_{R\ or\ B}}{V_G}$			−30	dB
RF VM1	Calculate CT2 = $20 \log \frac{V}{V_0}$ against the amplitude Vo in the TV input mode (VS = 2.0V)			−35	dB
RF VM1	When the measured value is set at V, $CT_1 = 20 \log \frac{V}{V_0}$			−40	dB
VM2	Similar to the TV input dynamic range	0.65	0.7		V
VM2	Fix the MK4 amplitude at 0.5 Vp-p and measure V. $G_{L\,max} = 20 \log \frac{V}{0.5} - G_{TV}$	11.7	12.7	13.7	dB
	$\Delta G_{L\,max\,1} : RG_{L\,max} \quad GG_{L\,max}$ $\Delta G_{L\,max\,2} : GG_{L\,max} \quad BG_{L\,max}$ $\Delta G_{L\,max\,3} : BG_{L\,max} \quad RG_{L\,max}$	−0.9	0.0	0.9	dB
VM2	Fix the MK4 amplitude at 0.5 Vp-p and measure V. $G_{L\,min} = 20 \log \frac{V}{0.5} - G_{TV}$	−3.5	1.5	6.5	dB

Test No.	Test item	Symbol	SW setting to ON								Bias condition (V)									Composit In and Markers	Test point	Description of output waveforms and test method	Min.	Typ.	Max.	Unit
											V1	V2	V3	VS1	VS2	VS3	VS4	VS5	VS6	VS7						
37	PIC AMP GAIN MIN correlation	$\Delta G_{L\,min\,1}$																				$\Delta G_{L\,min\,1}$ $RG_{L\,min}$ $GG_{L\,min}$				
	PIC AMP GAIN MIN correlation	$\Delta G_{L\,min\,2}$																				$\Delta G_{L\,min\,2}$ $GG_{L\,min}$ $BG_{L\,min}$	−2.5	0.0	2.5	dB
	PIC AMP GAIN MIN correlation	$\Delta G_{L\,min\,3}$																				$\Delta G_{L\,min\,3}$ $BG_{L\,min}$ $RG_{L\,min}$				
38	Ext PIC (pin 20) input range	V_{20}										9.0	9.0	2.0	0	Variable	4.5	2.0	0	4.5		Input range of pin 20	0.5		9.0	V
39	LIN. black level (R)	RB_{LIN}	A4	A6	C10						↓	↓	↓	↓	9.0	↓	↓	↓	↓	No change in MK1 to MK4 from the preceding page (However, the MK4 amplitude is fixed at 0.5 Vp-p)	VM2	Measure V	90	275	460	mV
	LIN. black level (G)	GB_{LIN}	↓	A8	C8						↓	↓	↓	↓	↓	↓	↓	↓	↓							
	LIN. black level (B)	BB_{LIN}	↓	A10	C6						↓	↓	↓	↓	↓	↓	↓	↓	↓							
40	Picture ABL operating voltage	PV_{ABL}	↓	A5	B13	C10					↓	↓	↓	↓	↓	↓	Variable	↓	↓		VM2	Threshold voltage when the picture ABL operates.	4.30	4.40	4.50	V
41	Brightness ABL operating voltage	BV_{ABL}	↓	↓	↓	↓					↓	↓	↓	↓	↓	↓	↓	↓	↓		VM2	Threshold voltage when the brightness ABL operates.	3.35	3.55	3.75	V
42	TV/EXT threshold	V_{MOD}	↓	↓		↓					↓	↓	↓	Variable	↓	↓	2.0	↓	↓		VM2	TV/EXT control threshold voltage	0.70	1.00	1.30	V
43	LIN/DIG threshold	V_{LD}	↓	↓		↓					↓	↓	Variable	0	↓	↓	↓	↓	↓		VM2	LIN/DIG control threshold voltage	1.00	1.20	1.40	V
44	EXT clamp threshold	V_{EB}	↓	A15	C4	↓					↓	↓	2.0	↓	↓	↓	↓	↓	↓		MP1	EXT clamp threshold voltage	0.90	1.00	1.10	V
45	Ys threshold	V_{YS}	↓	A5		↓					↓	↓	↓	↓	↓	↓	↓	↓	Variable		VM2	Ys threshold voltage	0.50	0.65	0.90	V
46	Ys pulse response (R)	RT_{YS}	↓	A6		↓					↓	↓	↓	↓	↓	↓	↓	↓	4.5	No change in MK1 to MK4 	VM2	Average value of time difference (rise and fall)		50	75	nsec
	Ys pulse response (G)	GT_{YS}	↓	A8		C8					↓	↓	↓	↓	↓	↓	↓	↓	↓							
	Ys pulse response (B)	BT_{YS}	↓	A10		C6					↓	↓	↓	↓	↓	↓	↓	↓	↓							
47	LIN DG (R)	RD_L	↓	A5	C10						↓	↓	↓	↓	↓	↓	↓	↓	↓	No change in MK1 to MK3 (no MK4) 	VM2	 $\frac{D_1 - D_2}{D_1} \times 100\%$			13	%
	LIN DG (G)	GD_L	↓	A7	C8						↓	↓	↓	↓	↓	↓	↓	↓	↓							
	LIN DG (B)	BD_L	↓	A9	C6						↓	↓	↓	↓	↓	↓	↓	↓	↓							
48	LIN. frequency response (R)	Rf_L	↓	A5	A14	B15	C10	C14			↓	↓	↓	↓	↓	↓	↓	4.5	↓	MK1, MK4 : GND MK2 RF IN : Input CW of 0.5 Vp-p, 500 kHz, 200 MHz	RF VM1	Gain difference at 500 kHz to 20 MHz.	−5.0	−3.7	0.0	dB
	LIN. frequency response (G)	Gf_L	↓	A7	↓	↓	C8	↓			↓	↓	↓	↓	↓	↓	↓	↓	↓							
	LIN. frequency response (B)	Bf_L	↓	A9	↓	↓	C6	↓			↓	↓	↓	↓	↓	↓	↓	↓	↓							
49	LIN. input channel crosstalk	CT_{RG}	↓	A6	A7	A10	A14	B15	C10	C14	↓	↓	↓	↓	↓	↓	↓	↓	↓	RF IN : 3.58MHz, 0.5Vp-p	RF VM1	R and B output ratios against the G output $CT_4 = 20\log\frac{V_{R,B}}{V_G}$			−30	dB
		CT_{GB}	↓	↓	↓	↓	↓	C6	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓							
50	Mode crosstalk (LIN→TV)	CT_{5R}	A5	B8	B10	B12	↓	↓	C10	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓		RF VM1	Calculate $CT_5 = 20\log\frac{V}{V_O}$ against the output amplitude Vo in the LIN input mode (SW A4 ON)			−45	dB
		CT_{5G}	A7	↓	↓	↓	↓	↓	C8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓							
		CT_{5B}	A9	↓	↓	↓	↓	↓	C6	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓							

Test No.	Test item	Symbol	SW setting to ON					Bias condition (V)										Composit In and Markers	Test point	Description of output waveforms and test method	Min.	Typ.	Max.	Unit
								V1	V2	V3	VS1	VS2	VS3	VS4	VS5	VS6	VS7							
51	Mode crosstalk (LIN→DIG)	CT_{6R}	A 5	A 14	B 15	C 10	C 14		9.0	9.0	0	0	9.0	4.5	2.0	4.5	4.5	RF IN : 3.58MHz, 0.5Vp-p	RF VM1	When the measured value is set to V, $CT_6 \quad 20 \log \frac{V}{V_0}$			−45	dB
		CT_{6G}	A 7	↓	↓	C 8	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓							
		CT_{6B}	A 9	↓	↓	C 6	↓		↓	↓	↓	↓	↓	↓	↓	↓	↓							
52	DIG. input H level (R)	RV_{DH}	B 1	C 10					↓	↓	↓	↓	↓	↓	↓	↓	↓	MK1 9V / 0V MK2 0V / 9V MK3 9V / 0V Comp In 0V Variable	VM2	Threshold voltage of DIG. input H level	1.50	1.67	1.85	V
	DIG. input H level (G)	GV_{DH}	B 2	C 8					↓	↓	↓	↓	↓	↓	↓	↓	↓							
	DIG. input H level (B)	BV_{DH}	B 3	C 6					↓	↓	↓	↓	↓	↓	↓	↓	↓							
53	DIG. PIC. MAX (R)	$RV_{D\,max}$	B 1	C 10					↓	↓	↓	↓	↓	↓	↓	↓	↓		VM2	Obtain V_1 with the Comp. In amplitude at 3 Vp-p.	1.10	1.35	1.60	V
	DIG. PIC. MAX (G)	$GV_{D\,max}$	B 2	C 8					↓	↓	↓	↓	↓	↓	↓	↓	↓							
	DIG. PIC. MAX (B)	$BV_{D\,max}$	B 3	C 6					↓	↓	↓	↓	↓	↓	↓	↓	↓							
54	DIG. PIC. MAX correlation	$\Delta V_{D\,max\,1}$																		$\Delta V_{D\,max\,1}$ $RV_{D\,max} - GV_{D\,max}$				
	DIG. PIC. MAX correlation	$\Delta V_{D\,max\,2}$																		$\Delta V_{D\,max\,2}$ $GV_{D\,max} - BV_{D\,max}$	−170	0	170	mV
	DIG. PIC. MAX correlation	$\Delta V_{D\,max\,3}$																		$\Delta V_{D\,max\,3}$ $BV_{D\,max} - RV_{D\,max}$				
55	DIG. PIC. MIN (R)	$RV_{D\,min}$	B 1	C 10					↓	↓	↓	↓	0.3	↓	↓	↓	↓		VM2	Comp. In amplitude is 3Vp-p.	70	230	390	mV
	DIG. PIC. MIN (G)	$GV_{D\,min}$	B 2	C 8					↓	↓	↓	↓	↓	↓	↓	↓	↓							
	DIG. PIC. MIN (B)	$BV_{D\,min}$	B 3	C 6					↓	↓	↓	↓	↓	↓	↓	↓	↓							
56	DIG. PIC. MIN correlation	$\Delta V_{D\,min\,1}$																		$\Delta V_{D\,min\,1}$ $RV_{D\,min} - GV_{D\,min}$				
	DIG. PIC. MIN correlation	$\Delta V_{D\,min\,2}$																		$\Delta V_{D\,min\,2}$ $GV_{D\,min} - BV_{D\,min}$	−50	0	50	mV
	DIG. PIC. MIN correlation	$\Delta V_{D\,min\,3}$																		$\Delta V_{D\,min\,3}$ $BV_{D\,min} - RV_{D\,min}$				
57	DIG black level (R)	RB_D	B 1	C 10					↓	↓	↓	↓	↓	↓	↓	↓	↓		VM2	Measure V	70	230	390	mV
	DIG black level (G)	GB_D	B 2	C 8					↓	↓	↓	↓	↓	↓	↓	↓	↓							
	DIG black level (B)	BB_D	B 3	C 6					↓	↓	↓	↓	↓	↓	↓	↓	↓							
58	DIG black level correlation	Δ_{BD1}																		ΔV_{BD1} $RB_D - GB_D$				
	DIG black level correlation	Δ_{BD2}																		ΔV_{BD2} $GB_D - BB_D$	−50	0	50	mV
	DIG black level correlation	Δ_{BD3}																		ΔV_{BD3} $BB_D - RB_D$				

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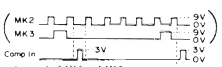
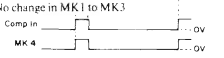
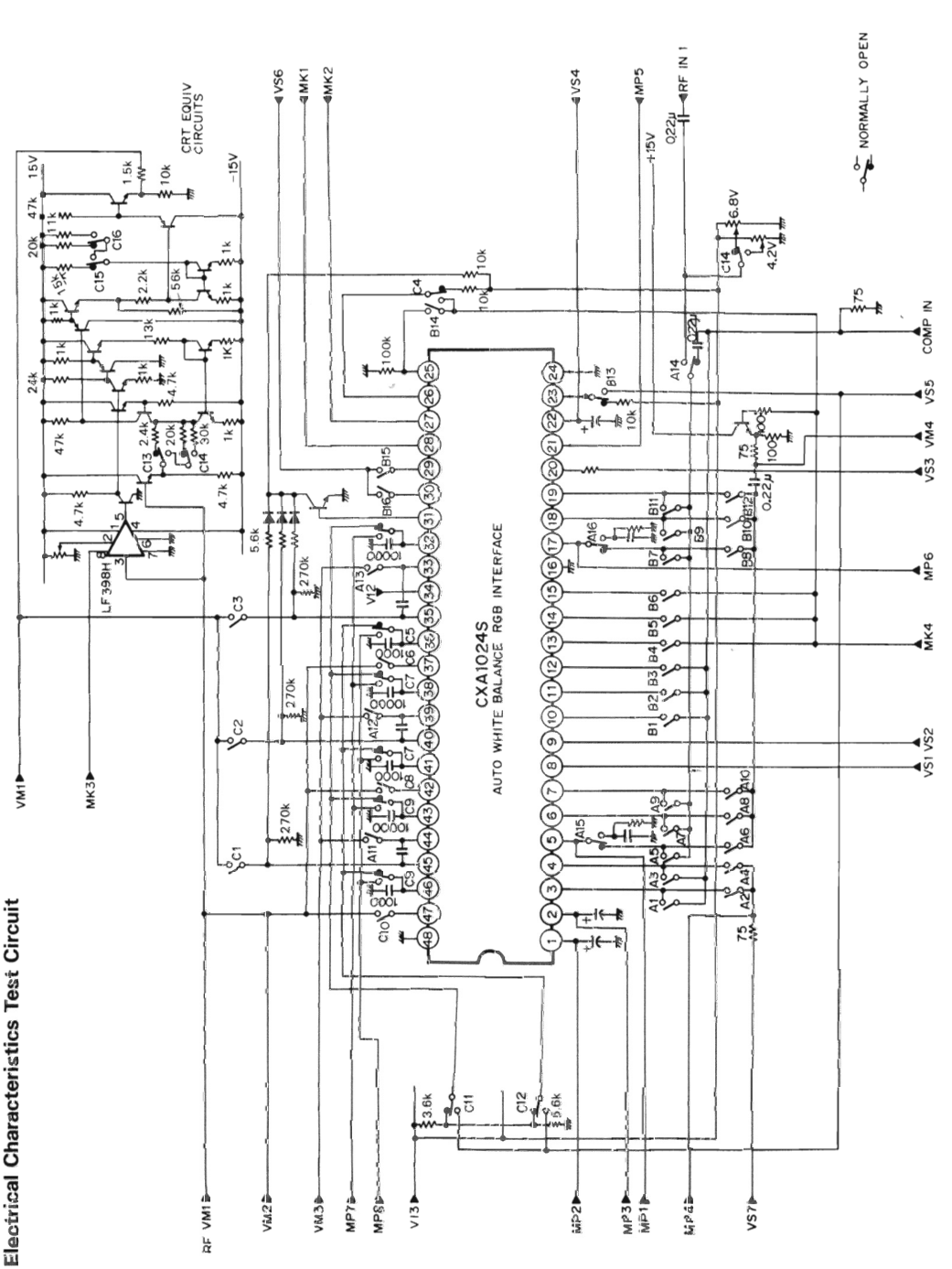
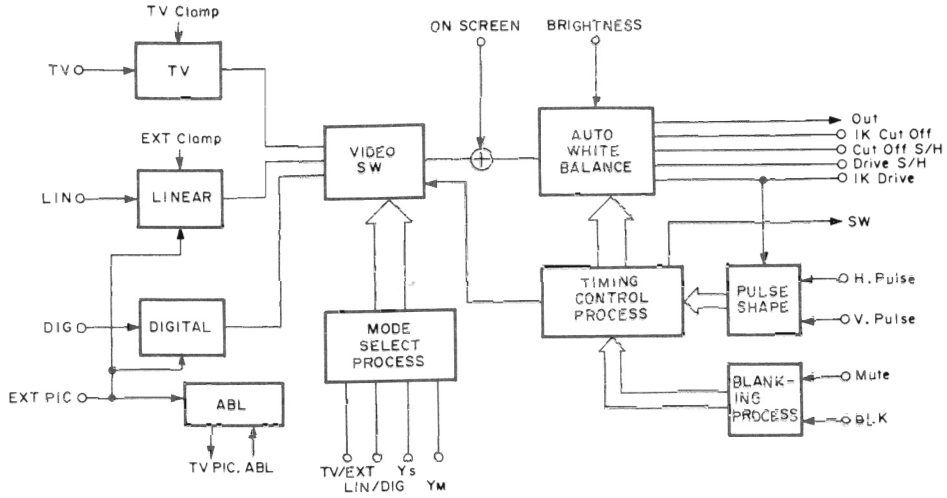
Test No.	Test item	Symbol	SW setting to ON	Bias condition (V) V1	V2	V3	VS1	VS2	VS3	VS4	VS5	VS6	VS7	Composit In and Markers	Test point	Description of output waveforms and test method	Min.	Typ.	Max.	Unit
59	TV clamp error (R)	V_{TCER}			9.0	9.0	0	0	0.3	4.5	2.0	4.5	4.5	No change in MK1 to MK3. Comp In from the preceding page. (However, Comp In amplitude is fixed at 3 Vp-p)		$V_{TCER} = RB_{TV} - RB_D$				
	TV clamp error (G)	V_{TCEG}														$V_{TCEG} = GB_{TV} - GB_D$		25	50	mV
	TV clamp error (B)	V_{TCEB}														$V_{TCEB} = BB_{TV} - BB_D$				
60	TV clamp error correlation	ΔV_{TCE1}														$\Delta V_{TCE1} = V_{TCER} - V_{TCEG}$				
	TV clamp error correlation	ΔV_{TCE2}														$\Delta V_{TCE2} = V_{TCEG} - V_{TCEB}$	−15	0	15	mV
	TV clamp error correlation	ΔV_{TCE3}														$\Delta V_{TCE3} = V_{TCEB} - V_{TCER}$				
61	LIN clamp error (R)	V_{LCER}														$V_{LCER} = RB_{LIN} - RB_D$				
	LIN clamp error (G)	V_{LCEG}														$V_{LCEG} = GB_{LIN} - GB_D$		25	50	mV
	LIN clamp error (B)	V_{LCEB}														$V_{LCEB} = BB_{LIN} - BB_D$				
62	LIN clamp error correlation	ΔV_{LCE1}														$\Delta V_{LCE1} = V_{LCER} - V_{LCEG}$				
	LIN clamp error correlation	ΔV_{LCE2}														$\Delta V_{LCE2} = V_{LCEG} - V_{LCEB}$	−15	0	15	mV
	LIN clamp error correlation	ΔV_{LCE3}														$\Delta V_{LCE3} = V_{LCEB} - V_{LCER}$				
63	DIG.BRT.MAX (R)	$RB_{D\,max}$	B 1 C 10	↓	↓	↓	↓	↓	6.5	↓	↓	↓		VM2		−120	−20	80	mV
	DIG.BRT.MAX (G)	$GB_{D\,max}$	B 2 C 8	↓	↓	↓	↓	↓	↓	↓	↓	↓								
	DIG.BRT.MAX (B)	$BB_{D\,max}$	B 3 C 6	↓	↓	↓	↓	↓	↓	↓	↓	↓								
64	DIG.BRT.MIN (R)	$RB_{D\,min}$	B 1 C 10	↓	↓	↓	↓	↓	2.5	↓	↓	↓		VM2		350	500	650	mV
	DIG.BRT.MIN (G)	$GB_{D\,min}$	B 2 C 8	↓	↓	↓	↓	↓	↓	↓	↓	↓								
	DIG.BRT.MIN (B)	$BB_{D\,min}$	B 3 C 6	↓	↓	↓	↓	↓	↓	↓	↓	↓								
65	DIG pulse response (R)	RT_D	B 1 C 10	↓	↓	↓	↓	9.0	4.5	↓	↓	↓		No change in MK1 to MK3 	VM2	Average value of time difference (rise and fall)		50	70	nsec
	DIG pulse response (G)	GT_D	B 2 C 8	↓	↓	↓	↓	↓	↓	↓	↓	↓								
	DIG pulse response (B)	BT_D	B 3 C 6	↓	↓	↓	↓	↓	↓	↓	↓	↓								
66	On-screen BLK threshold (R)	RS_{BL}	B 1 B 4 C 10	↓	↓	↓	↓	↓	↓	↓	↓	↓		No change in MK1 to MK3 	VM2	Blanking threshold voltage of on-screen input pin.	2.55	2.67	2.80	V
	On-screen BLK threshold (G)	GS_{BL}	B 2 B 5 C 8	↓	↓	↓	↓	↓	↓	↓	↓	↓								
	On-screen BLK threshold (B)	BS_{BL}	B 3 B 6 C 6	↓	↓	↓	↓	↓	↓	↓	↓	↓								
67	On-screen input H level (R)	RS_H	B 4 C 10	9.0	9.0	0	0	9.0	4.5	2.0	4.5	4.5		No change in MK1 to MK4. Comp In.	VM2	MK4 amplitude so that Vx becomes 4.0V	5.30	6.15	7.00	V
	On-screen input H level (G)	GS_H	B 5 C 8	↓	↓	↓	↓	↓	↓	↓	↓	↓								
	On-screen input H level (B)	BS_H	B 6 C 6	↓	↓	↓	↓	↓	↓	↓	↓	↓								

Electrical Characteristics Test Circuit



Description of Operation

Figure below shows the signal flow and control systems of the entire system.



All black levels of the three video input signals (TV, LIN and DIG) are clamped or exchanged with Vref1 and input to VIDEO SW. The reference signals (W-Drive, B-Cut OFF) for the Auto White Balance (AWB) is added with the insertion timing generated in the timing control process and output from the VIDEO SW. Here, the cut-off reference is fixed on Vref2, and the drive reference set to approx. 60 IRE with the internal resistance ratio.

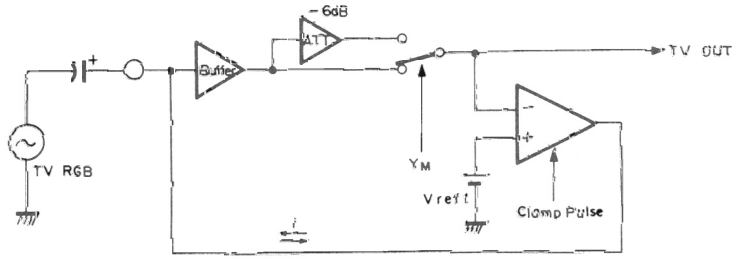
The output of VIDEO SW is input to the AWB PROCESS after ON SCREEN information is added.

In the AWB PROCESS, both gain control and level shift processing are done so that the IK amount input from the IK in pin becomes constant.

All of the timings are composed of H pulses and V pulses (V-Blanking). That is, with the TIMING CONTROL PROCESS, the drive and cutoff reference signals, the sampling hold signal in AWB, the video Blanking signal and the timing signal for IK SW are all generated.

In the BLANKING PROCESS, the Blanking signal for the power-on mute is generated. In the MODE SELECT PROCESS, video signal selection and YS/YM control signals are generated and are output to VIDEO SW or TV RGB.

1. TV RGB Input

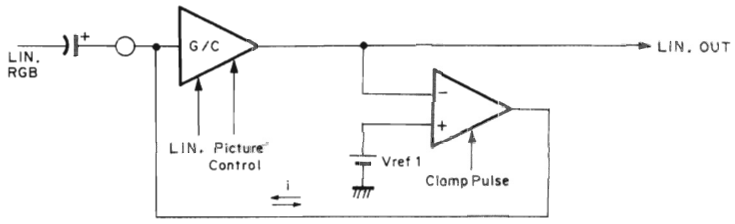


The input signal is compared with Vref1 during clamp pulse interval, fed back to the input pin and as a result, its black level is clamped and the clamped signal is output.

There are offsets of several tens of mVs while the Y/C IC goes through the RGB output. For this reason, the output does not correlate with the reference signal and it is not possible to make the color temperature for AWB regular. The input clamp regulates the RGB DC.

Therefore, the input TV RGB must be the one which sync portion has been exchanged with the black level.

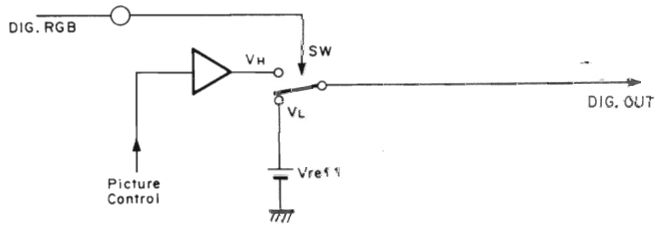
2. Linear (LIN) RGB Input



The linear input signal is, after being amplified by the gain control amplifier, compared with Vref1 during the clamp pulse interval, fed back to the input pin and its pedestal portion is clamped.

For the clamp pulse, the delayed sync pulse is used. This is because even some of the RGB signals used for some products, etc. may contain syncs causing malfunctions. The gain control amplifier can be set so that it can control the TV RGB signal for approx. 80% of all gains.

3. Digital (DIG) RGB Input



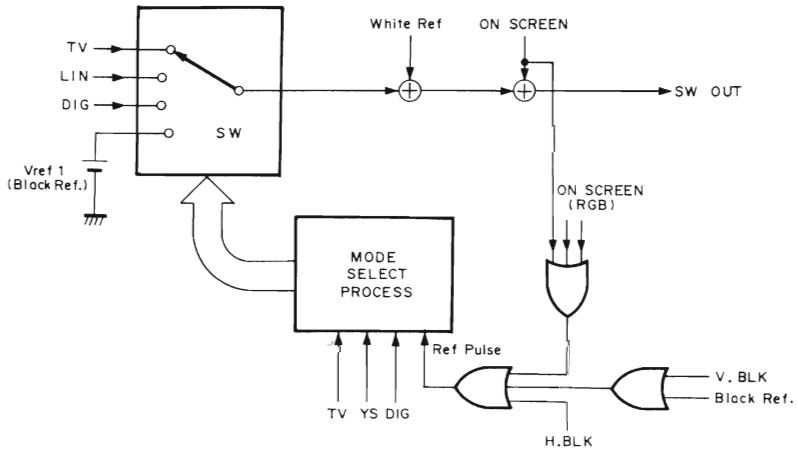
The input Digital RGB signal becomes the SW control signal and is output with the following:

LO : Vref1

HI : VH

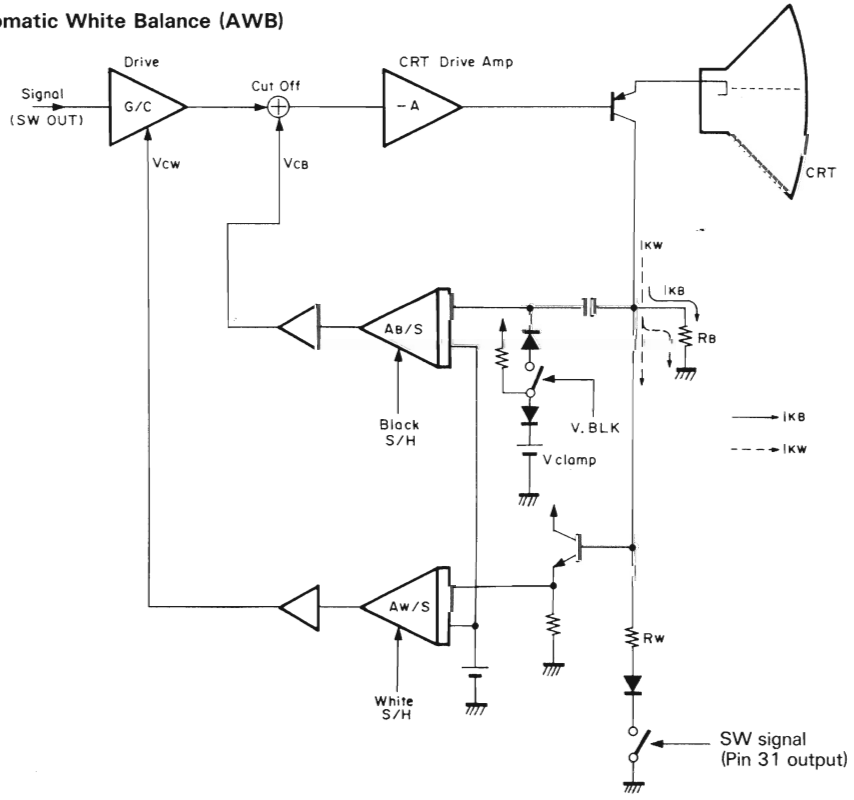
VH is controlled through Picture Control.

4. Video SW / ON SCREEN



When the ON SCREEN signal is input, the video signal is replaced by Black Ref. This is to prevent the video signal from masking the character signal (ON SCREEN input).

5. Automatic White Balance (AWB)



The video signal (See figure in page 17) with the AWB reference signal inserted is output with the gain of its drive side controlled and the level of its cutoff side shifted.

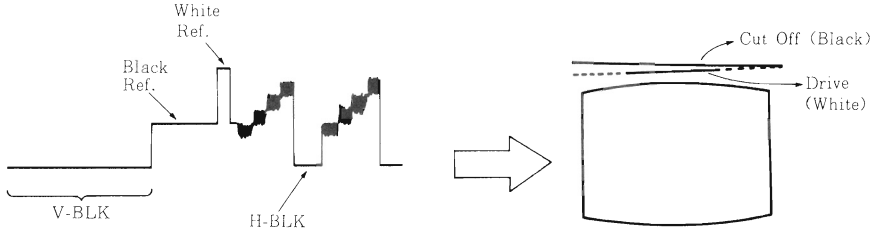
The signal amplified with the CRT drive amplifier drives the cathode with the PNP transistor emitter-follower and the transistor collector current becomes the cathode current. This cathode current is converted into voltage, compared with the internal reference voltage (Vref2) and fed back in the form of gain control and level shift.

The feedback system only works in portions where the reference signal is inserted. In other portions, gains and level shifts are held.

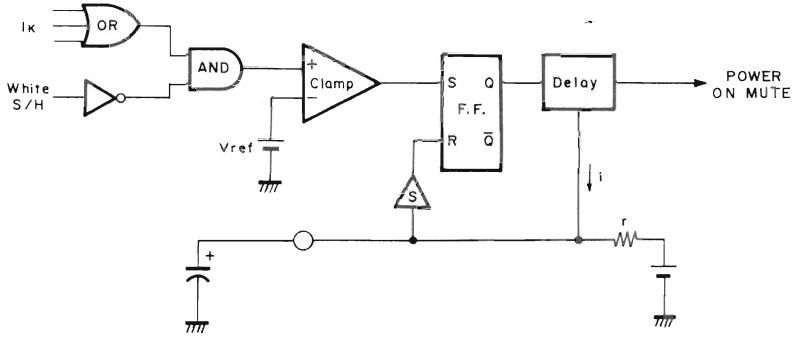
The cathode current is divided by means of the SW signal into two systems: I_{KB} in the cutoff portion (solid lines in the figure) and I_{KW} in the drive portion (dotted lines in the figure).

6. Timing Control/Pulse Shaping

All timing pulses are made from H pulses and V pulses. The H pulses are divided into NH pulses and H pulses by means of their input threshold. The NH pulse has a narrower pulse width than that of ordinary H pulses; it becomes the reference signal pulse for the Drive of the AWB. Therefore, the drive reference signal (white reference signal) becomes part of the H retrace portion (see Figure below).



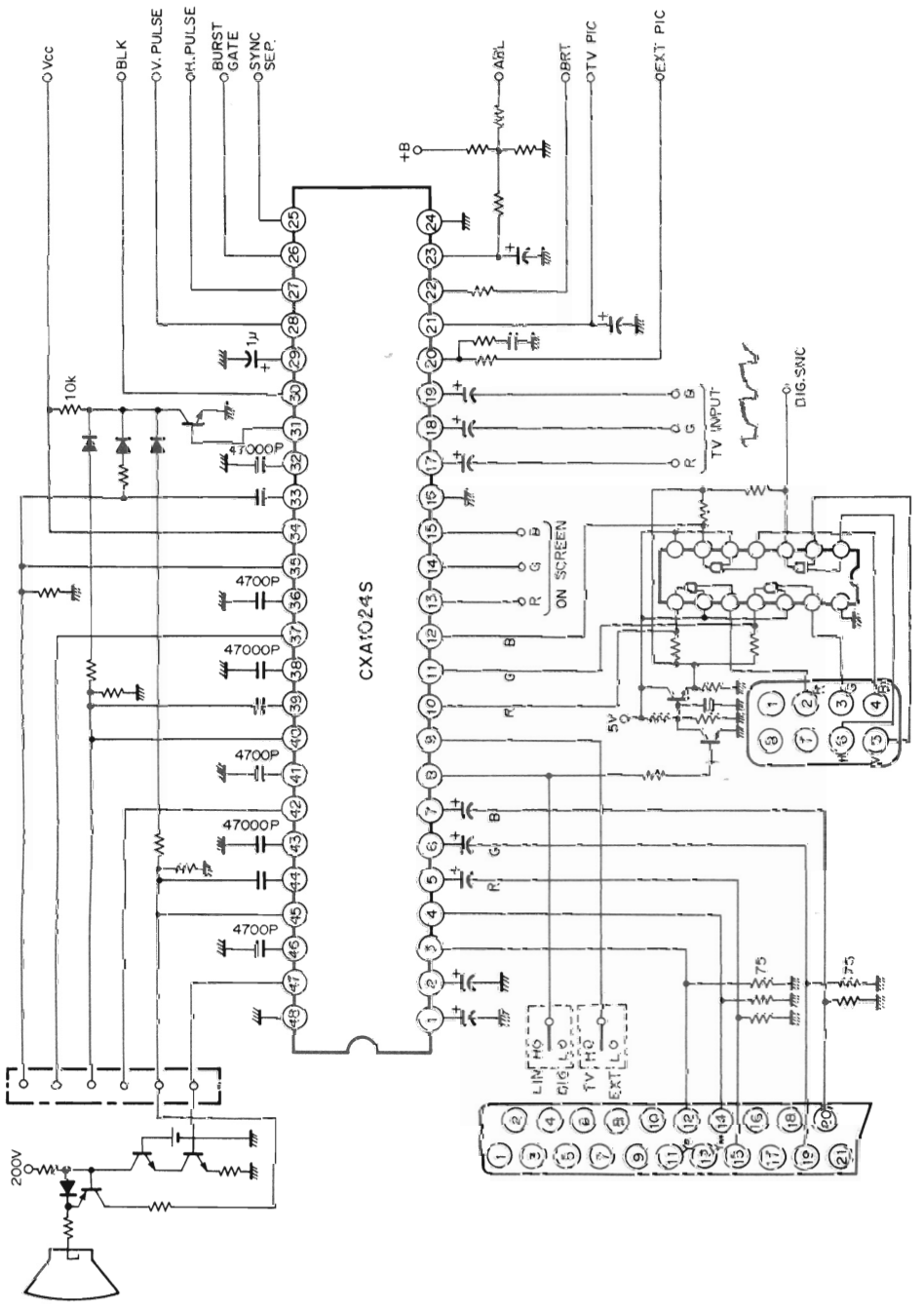
7. BLK Process



The RGB signal is input from the I_K pin. While AWB is not in operation, the signal remains 0 but the I_K return level of the white reference signal appears at the comparator input when I_K starts to flow. The cathode rise reaches completion when the white level has risen completely. It is assigned to the white reference portion not to be mistaken for the black reference.

When the signal peak overpasses Vref, the Flip Flop output becomes High. It is delayed by the time constant determined by an external capacitor and output as a power-on mute signal. As Flip Flop has to be reset at power on, an external capacitor is used.

Application Circuit



Notes on Application

1) Automatic White Balance (AWB)

The following constants must be determined when AWB is used:

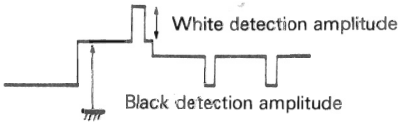
- CRT, VIDEO, AMP and GAIN
- Black detection resistance RB
- White detection resistance RW

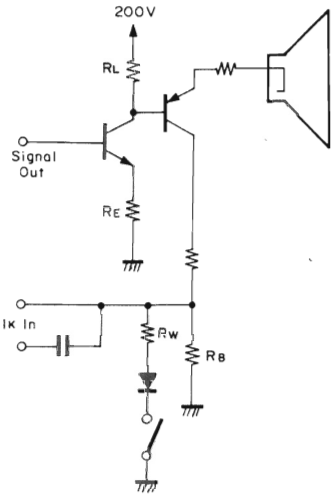
The variable range of AWB is as follows at Signal OUT.

Black detection voltage 1.3 to 4.3 VDC

White detection voltage 1.0 to 2.1 Vp-p

Therefore, the design center should take their average value.



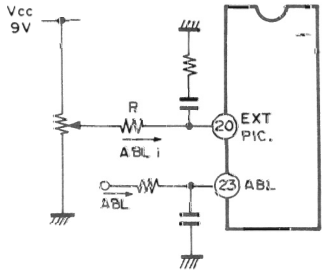


2) Picture (PIC) ABL

PIC ABL is designed to operate when the ABL pin (pin 23) DC voltage becomes less than 4.4V. The pin 20 input DC voltage is caused to drop by means of the ABL current that flows through resistance R and the gain starts to decrease. That is the ABL influence varies depending on the R value.

When R = 0, there is no PIC. ABL influence and only the BRT ABL works.

Input to pin 23 can be made by using a lug lead filter for instance and taking the ABL response into account. The ABL brightness is designed to operate when the ABL pin (pin 23) DC voltage becomes less than 3.5V.



3) Power On Mute

The time constant of the power-on mute can only be determined by the capacitance of the mute pin (pin 29). Select a constant that will not allow for any transient AWB results whether it starts cool or hot.

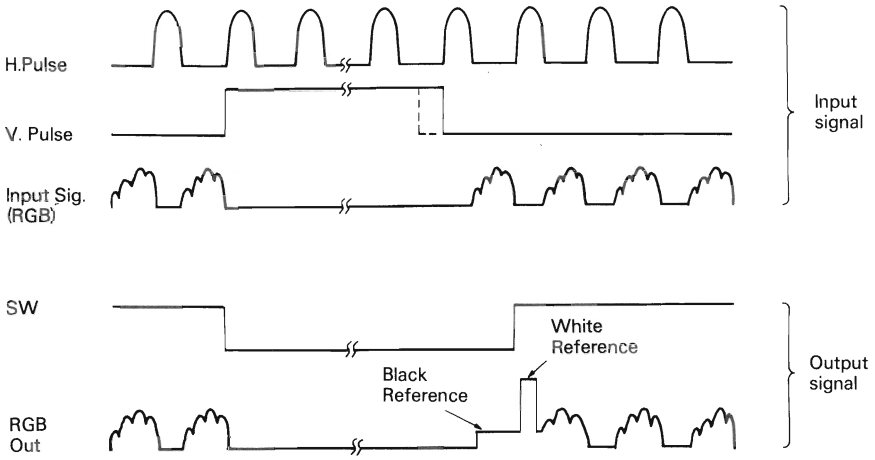
The sweeping speed of the AWB loop is determined by an external capacitor on Drive S/H and Cutoff S/H. A small capacitor will suffice as long as it does not vary with Vertical.

4) TV RGB input signal

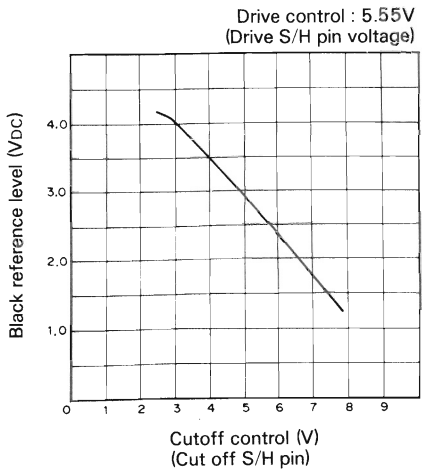
As described in "Description of Operation", the TV RGB signal must have its sync portion exchanged for a constant black level.

5) Others
5-1) Provide a capacitor to inhibit oscillations to Vref1 (pin 1) and Vref2 (pin 2).
5-2) Make the earth line as wide as possible.

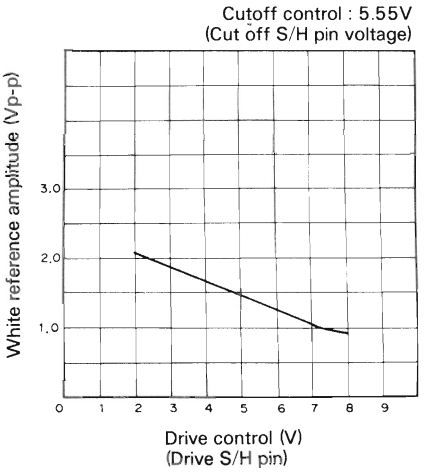
6) Timing chart



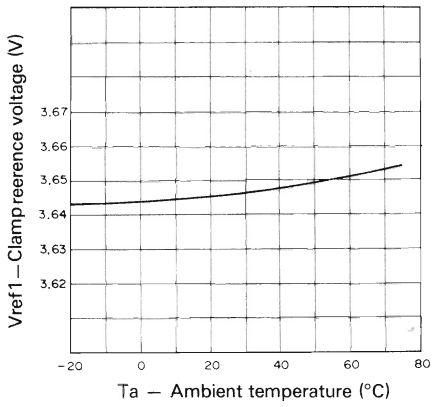
Cutoff control characteristics



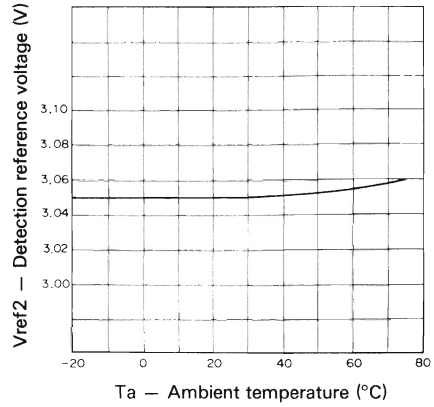
Drive control characteristics



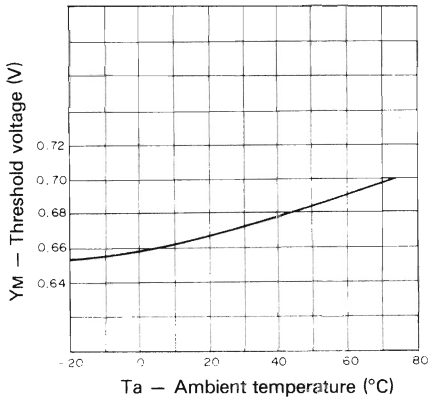
Clamp reference voltage vs. Ambient temperature



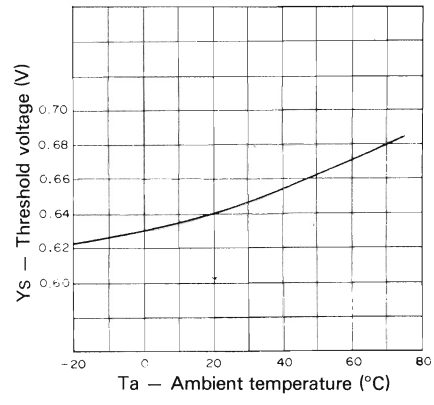
Detection reference voltage vs. Ambient temperature



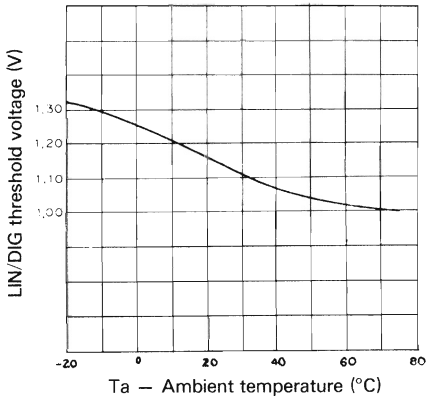
YM threshold vs. Ambient temperature



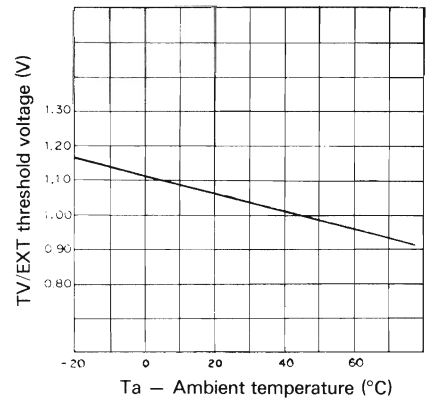
YS threshold vs. Ambient temperature



LIN/DIG threshold vs. Ambient temperature



TV/EXT threshold vs. Ambient temperature



SONY®

CXA1044P

RGB Interface for Ultra-High Resolution Display

Description

The CXA1044P is a bipolar IC designed for the RGB signal processing of ultra-high resolution displays.

Features

- 12 V single power supply operation
- Built-in wideband amplifier (with linear frequency response up to 30 MHz)
- External circuits can be simplified

Functions

- Brightness control and contrast control provided
- ABL, BLK and pedestal clamp provided

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	15	V
• Operating temperature	Topr	0 to 65	°C
• Storage temperature	Tstg	−55 to +150	°C
• Allowable power dissipation	PD	2190	mW

- Input voltage for each terminal (pin)

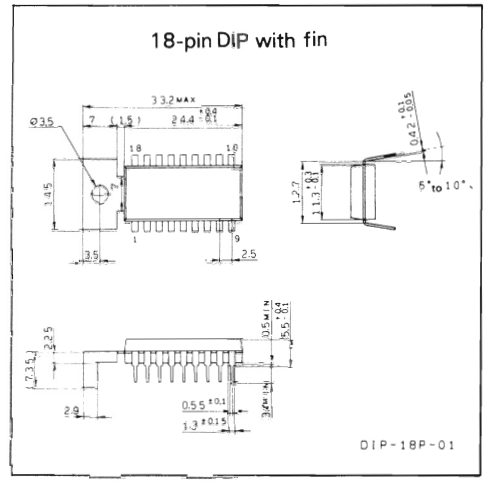
Pin name	Max. value	Pin name	Max. value
R IN	Vcc + 0.3V	R GND	5V
G IN	Vcc + 0.3V	G GND	5V
B IN	Vcc + 0.3V	B GND	5V
CONT CTL	Vcc + 0.3V		
CLAMP	Vcc + 0.3V		
BRIGHT	Vcc + 0.3V		
ABL	Vcc + 0.3V		
BLK	Vcc + 0.3V		

Recommended Operating Condition

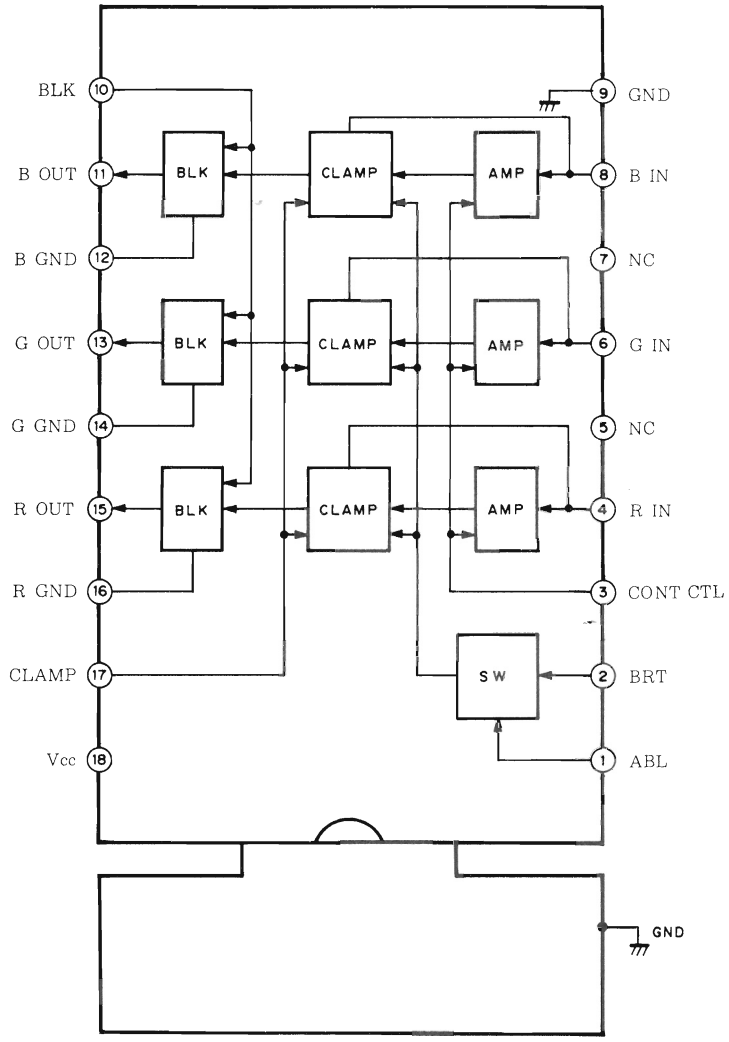
- Supply voltage Vcc 11 to 13 V

Package Outline

Unit: mm

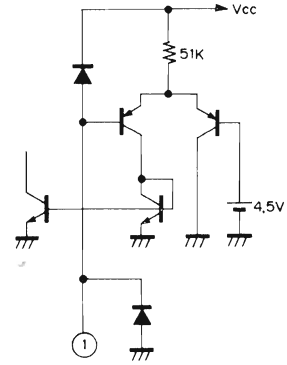
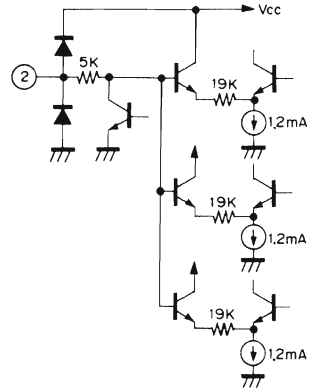
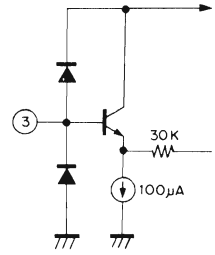


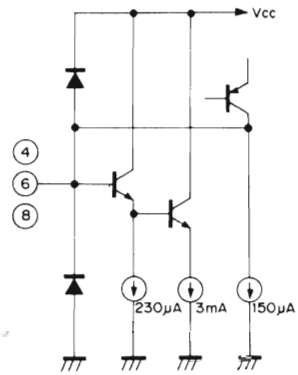
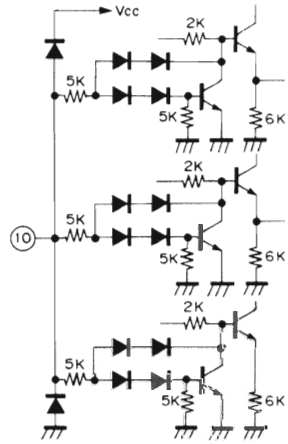
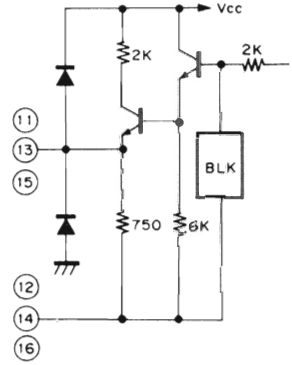
Block Diagram and Pin Configuration (Top View)

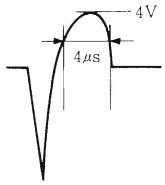
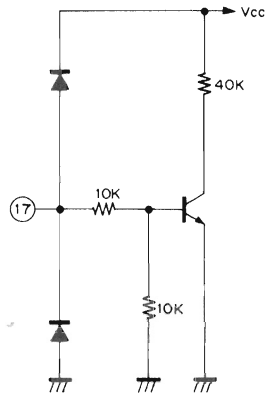


Pin Description

* External input voltage (DC voltage unless otherwise specified)

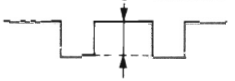
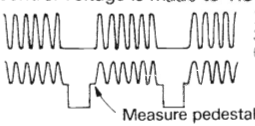
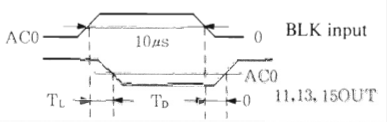
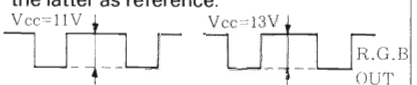
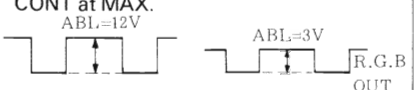
No.	Symbol	Voltage	Equivalent circuit	Description
1	ABL	* +12V		Pin for X-ray protection. With less than a threshold voltage, BRT CTL is made invalid and BRT level made minimum. Usually, +12V. ABL stands for Automatic Beam Limit.
2	BRT	* +4.5V		DC control pin for RGB primary color pedestal level
3	CONT CTL	* +8.1V		DC control pin for RGB primary color AC gain

No.	Symbol	Voltage	Equivalent circuit	Description
4 6 8	R IN G IN B IN	* 0.7V 0		Signal input pins. They are for clamp operations.
10	BLK	* 5V 0		Input pin for the composite BLK input. Reduce to the ground voltage when blanking RGB primary colors.
11 13 15	B OUT G OUT R OUT	4.8V 2.8 Vp-p 1.5V 0		Output pins for each of RGB primary colors.
12 14 16	B GND G GND R GND	* 0V		GND pins for each of the RGB outputs.

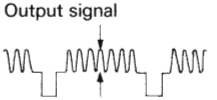
No.	Symbol	Voltage	Equivalent circuit	Description
17	CLAMP	* 		Clamp input pin. When high, they are for clamp operations.

Electrical Characteristics

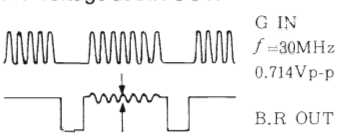
($Ta = 25°C$, $V_{CC} = 12V$, $*V_{CC} = 11V$ and $13V$ See the Electrical Characteristics Measuring Circuit.)

No.	Item	Symbol	BRT SW	CONT SW	ABL SW	Input switching SW R	G	B	Measurement contents and conditions	Min.	Typ.	Max.	Unit
1	BRT characteristics Lo	BRT_{LO}	1	2	1	2	2	2	Vary the BRT control voltage in three stages (1.8V, 4.5V and 12V) and measure the DC voltages at R.G.B. OUT.  Measure pedestal level of DC voltage.	0	0.7	1.0	V
	BRT characteristics CEN	BRT_{CEN}	2	2	1	2	2	2		0.8	1.1	1.5	V
	BRT characteristics MAX	BRT_{MAX}	3	2	1	2	2	2		2.0	2.5	3.1	V
2	Pedestal stability	ΔPED	2 2	1 3	1 1	1 1	1 1	1 1	Measure changes of pedestal level when CONT control voltage is made to 1.8V and 8.1V.  Measure pedestal voltage.	−300	0	+300	mV
3	BLK characteristics fall time	T_L	1	1	1	2	2	2	Measure at IC pins (11, 13, 15) the BLK pulse responses of RGB output waveform for a BLK input pulse. (so that no external buffer delay time is included). 	0	19	32	ns
	BLK characteristics rise time	T_D	1	1	1	2	2	2		0	47	100	ns
4	*Vcc characteristics	ΔV_{CC}	2	2	1	2	2	2	Measure difference of the R.G.B. OUT pedestal voltages when Vcc is switched between 13 and 11 V with the latter as reference. 	0	40	150	mV
5	ABL check	ABL	1 1	1 1	1 2	2 2	2 2	2 2	Measure difference of the R.G.B. OUT pedestal voltages when ABL voltage is switched between 12 and 3V with BRT CONT at MAX. 	1.6	1.9	2.4	Vp-p

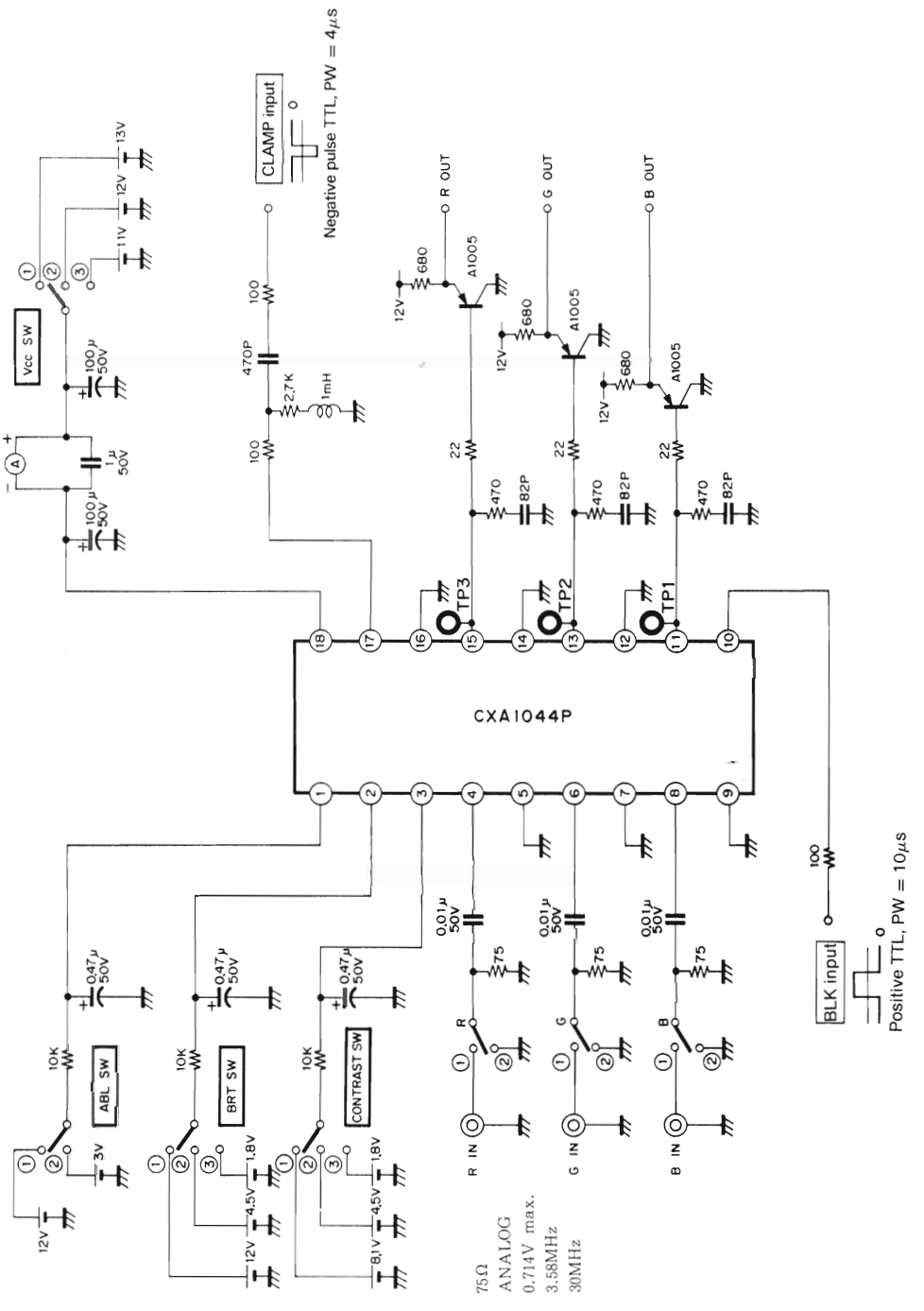
SONY

No.	Item	Symbol	BRT SW	CONT SW	ABL SW	Input switching SW R	Input switching SW G	Input switching SW B	Measurement contents and conditions	Min.	Typ.	Max.	Unit
6	ICC characteristics	Icc	1	1	1	2	2	2	Measure power consumption when BRT CONT is set at MAX.	46	53	62	mA
7	CONT characteristics (*See following page)	CONT MAX-MAX	1	1	1	1	1	1	Measure AC component of 3.58 Mz. Input signal R.G.B IN f = 3.58MHz 0.714Vp-p Output signal  R.G.B OUT Measure this voltage.	1250	1600	1900	mVp-p
		CONT MAX-CEN	1	2	1	1	1	1		700	890	1020	
		CONT MAX-MIN	1	3	1	1	1	1		250	340	410	
		CONT CEN-MAX	2	1	1	1	1	1		1300	1560	1800	
		CONT CEN-CEN	2	2	1	1	1	1		700	860	1000	
		CONT CEN-MIN	2	3	1	1	1	1		250	330	400	
		CONT MIN-MAX	3	1	1	1	1	1		1300	1480	1700	
		CONT MIN-CEN	3	2	1	1	1	1		700	840	1000	
		CONT MIN-MIN	3	3	1	1	1	1		250	330	400	

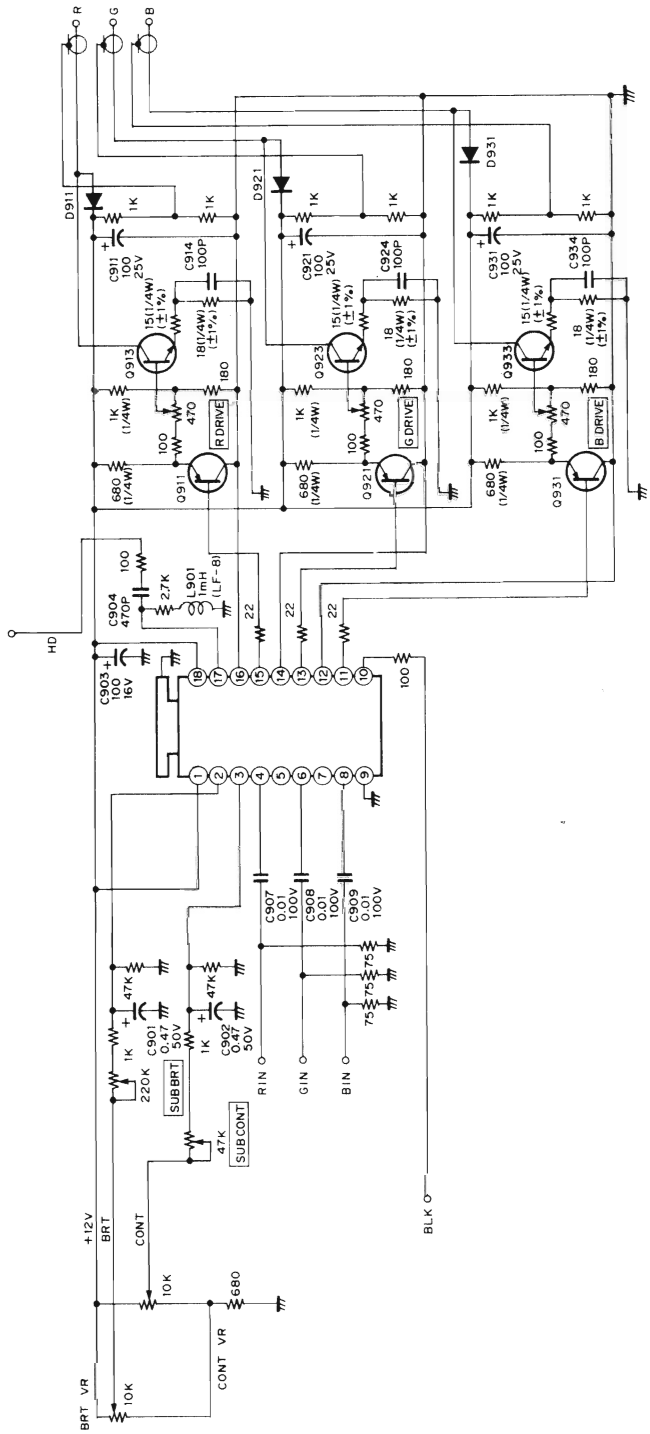
SONY

No.	Item	Symbol	BRT SW	CONT SW	ABL SW	Input switching SW R	G	B	Measurement contents and conditions	Min.	Typ.	Max.	Unit
	CONT characteristics*	f_{CONT} MAX-MAX	1	1	1	1	1	1	Then, measure AC component of 30 MHz and compare with that of 3.58 MHz.	− 1.50	0.45	2.50	dB
		f_{CONT} MAX-CEN	1	2	1	1	1	1		− 2.00	0.15	1.50	
		f_{CONT} MAX-MIN	1	3	1	1	1	1		− 1.00	1.30	2.80	
		f_{CONT} CEN-MAX	2	1	1	1	1	1		− 2.0	0.2	2.0	
		f_{CONT} CEN-CEN	2	2	1	1	1	1		− 2.0	− 0.2	1.5	
		f_{CONT} CEN-MIN	2	3	1	1	1	1		− 0.5	1.0	2.8	
		f_{CONT} MIN-MAX	3	1	1	1	1	1		− 1.5	0	1.2	
		f_{CONT} MIN-CEN	3	2	1	1	1	1		− 2.2	− 0.5	1.0	
		f_{CONT} MIN-MIN	3	3	1	1	1	1		− 1.0	0.7	2.4	
8	Crosstalk	CROS	1	1	1	2	1	2	Apply signal only on G IN with BRT CONT at MAX and measure crosstalk AV voltage at B.R OUT.  Measure crosstalk AC component		10	20	mVp-p

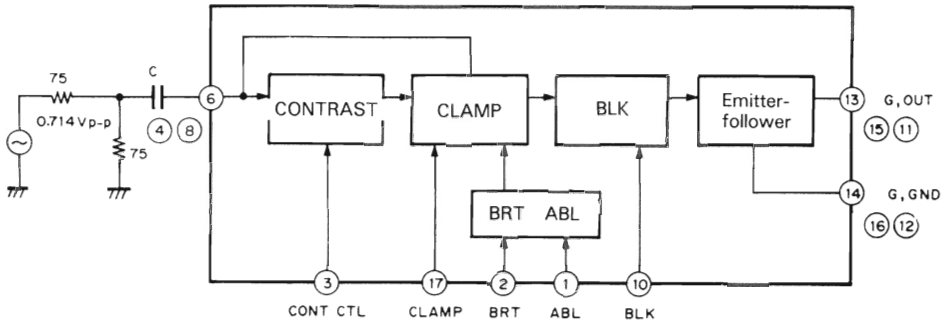
Electrical Characteristics Measuring Circuit



Application Circuit



Description of Operation



1) Contrast
Gains of the RGB signal (0.714Vp-p Max.) input with a signal source impedance of 75 Ω are controlled using a voltage externally input from the CONT CTL pin.

2) Pedestal clamp and brightness control
The pedestal clamp keeps clamping the pedestal level while pin 17 is HIGH. The brightness control controls the pedestal level with the DC control voltage which is externally input from the BRT pin.

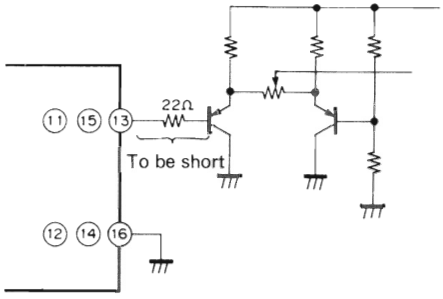
3) Setting of blanking
Blanking is made with COMPOSITE BLK externally input from the BLK pin and when the RGB signal is output with the emitter-follower.

4) Safety function
A BRT CTL protection circuit is activated by ABL when a circuit operation failure occurs (due to X ray).

Notes on Applications

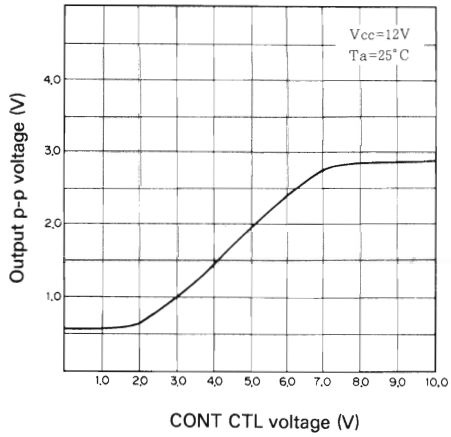
As this IC incorporates a wideband amplifier and since oscillation may result, be careful on the following points in preparing printed circuit board artworks.

1) As the R.G.B. OUT (pins 11, 13 and 15) must be connected to an emitter-follower, insert a small resistor (22 Ω) for oscillation prevention and connect to the next stage in a short pattern.

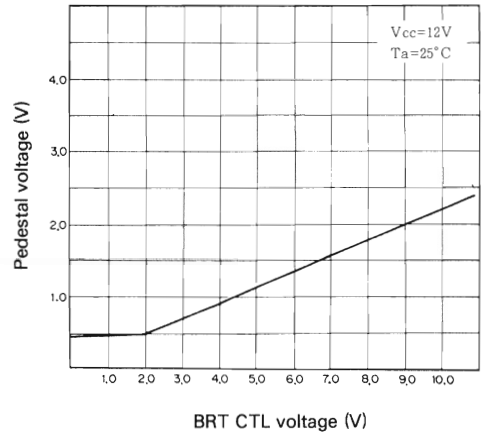


2) Check the IC oscillation not only at ambient temperature but also at low temperature when processing a board.

CONT Characteristics
(BRT Control Voltage = 4.5V)



BRT Characteristics
(CONT Control Voltage = 8.0V)



SONY

CXD1053S

Picture-in-Picture Memory Control IC for TV

Description

The CXD1053S is a picture-in-picture or multi-picture memory control IC designed for TV. It is used in combination with CXD1054S.

Functions

Memory control, read/write address generation, interface with an external CPU, control of CXD1054S

Structure

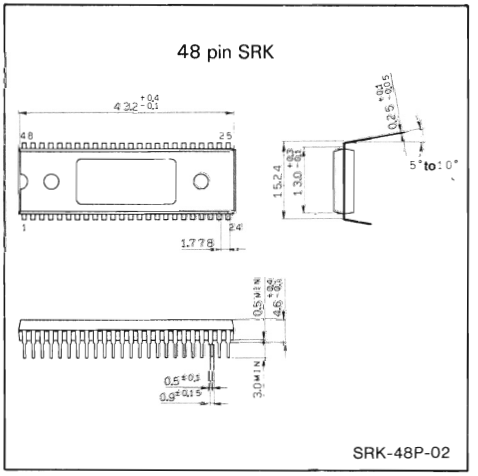
Silicon gate CMOS IC

Applications

Picture-in-picture TV
Multi-picture TV

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

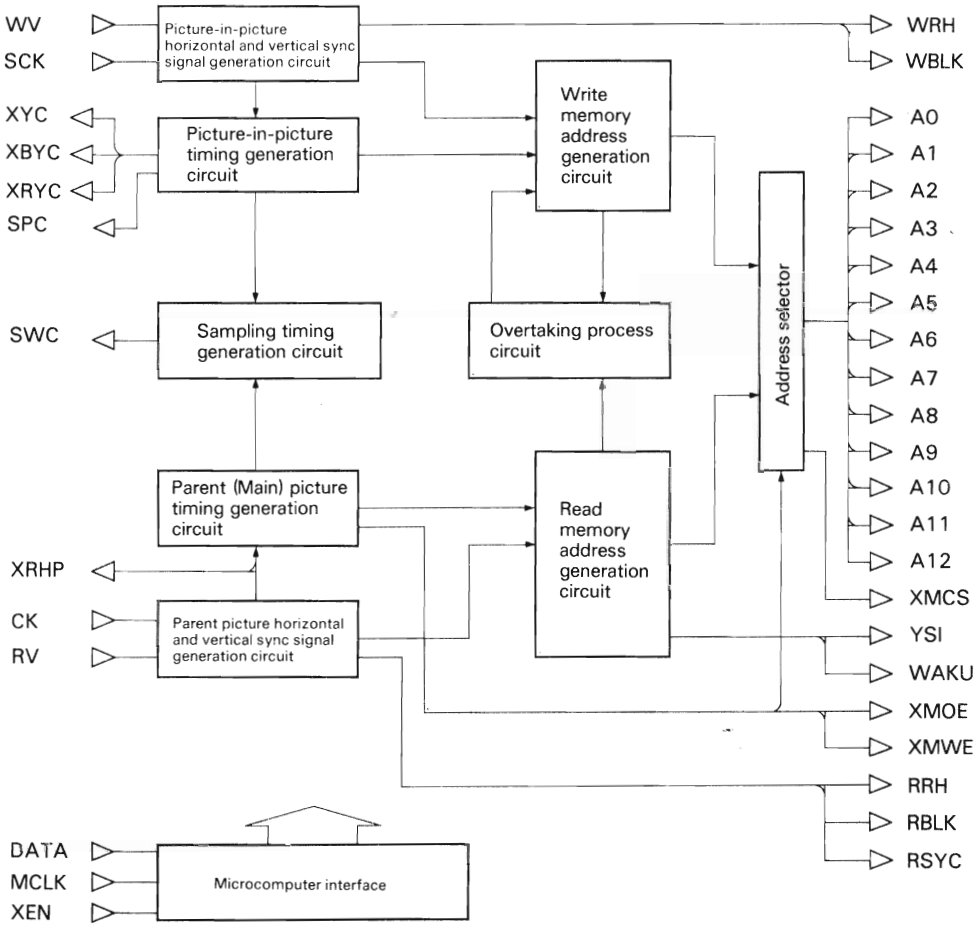
• Supply voltage	V_{DD}	V_{SS}*	−0.3 to +7.0	V
• Input voltage	V_I	V_{SS}*	−0.3 to V_{DD}+0.3	V
• Output voltage	V_O	V_{SS}*	−0.3 to V_{DD}+0.3	V
• Operating temperature	Topr		−20 to +75	°C
• Storage temperature	Tstg		−55 to +150	°C

*Note) V_{SS} = 0V

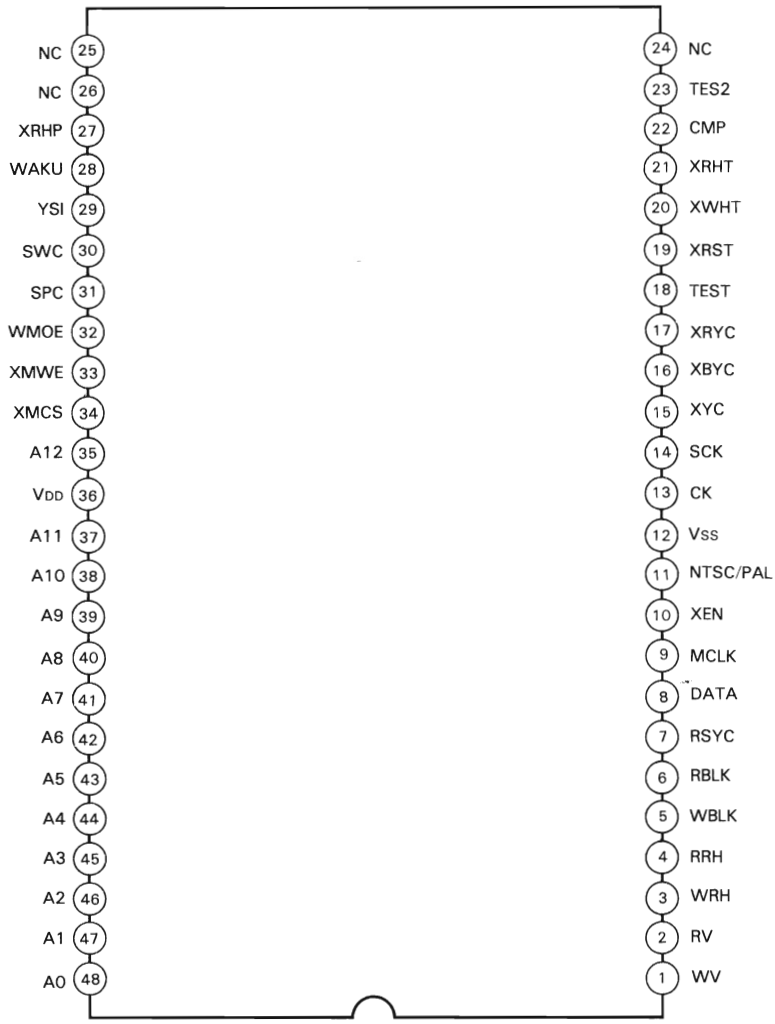
Recommended Operating Conditions

• Supply voltage	V_{DD}	5.0 ± 0.5	V
• Operating temperature	Topr	−20 to +75	°C

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	WV	I	Vertical sync signal input for picture-in-picture
2	RV	I	Vertical sync signal input for parent picture
3	WRH	O	Horizontal reference output for picture-in-picture AFC. Output with SCK frequency divided by 303.
4	RRH	O	Horizontal reference output for parent picture. Output with CK frequency divided by 455.
5	WBLK	O	Horizontal blanking output for picture-in-picture
6	RBLK	O	Horizontal blanking output for parent picture
7	RSYC	O	Horizontal sync signal output for parent picture
8	DATA	I	Data input from control microcomputer
9	MCLK	I	Clock input from control microcomputer
10	XEN	I	Enable input from control microcomputer
11	NTSC/PAL	I	NTSC/PAL switching. "H" = NTSC. "L" = PAL.
12	V_{SS}	–	GND
13	CK	I	Clock input for parent picture
14	SCK	I	Clock input for picture-in-picture
15	XYC	O	Y-signal select output controlling analog switches
16	XBYC	O	B-Y signal select output controlling analog switches
17	XRYC	O	R-Y signal select output controlling analog switches
18	TEST	I	Input for testing. Usually, set to "L".
19	XRST	I	Input for resetting. Usually, set to "H".
20	XWHT	I	Input for testing. Usually, set to "H".
21	XRHT	I	Input for testing. Usually, set to "H".
22	CMP	O	Output for testing
23	TES2	I	Input for testing. Usually, set to "H".
24	NC	–	
25	NC	–	
26	NC	–	
27	XRHP	O	Horizontal reset pulse output for parent picture, connected to CXD1054S.
28	WAKU	O	WAKU (frame) signal output, connected to CXD1054S.
29	YSI	O	Signal output for switching parent/subsidiary pictures, connected to CXD1054S.
30	SWC	O	Clock output for converting samples, connected to CXD1054S.
31	SPC	O	Clock output for serial/parallel converting, connectd to CXD1054S.
32	XMOE	O	Memory OE (Output Enable) signal output
33	XMWE	O	Memory WE (Write Enable) signal output
34	XMCS	O	Memory CS (Chip Select) signal output
35	A12	O	Memory address output. Most significant bit.
36	V_{DD}	–	Power supply pin
37	A11	O	Memory address outout
38	A10	O	Memory address output
39	A9	O	Memory address output
40	A8	O	Memory address output

Pin Description

No.	Symbol	I/O	Description
41	A7	O	Memory address output
42	A6	O	Memory address output
43	A5	O	Memory address output
44	A4	O	Memory address output
45	A3	O	Memory address output
46	A2	O	Memory address output
47	A1	O	Memory address output
48	A0	O	Memory address output. Least significant bit.

Electrical Characteristics

DC Characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, Topr = −20 to +75°C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply current		I_{DD}			15		mA
		I_{DDS}	Static state $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$			0.1	mA
Output voltage	H level	V_{OH}	I_{OH} = −0.4 mA	4.0		V_{DD}	V
	L level	V_{OL}	I_{OL} = 2.0 mA	V_{SS}		0.4	V
Input voltage	H level	V_{IH}		2.2			V
	L level	V_{IL}				0.8	V
Input leakage current		I_{IL}	V_I = 0V to V_{DD}	−10		10	μA

Input/Output Capacity

$V_{DD} = V_I$ = 0V, f = 1 MHz

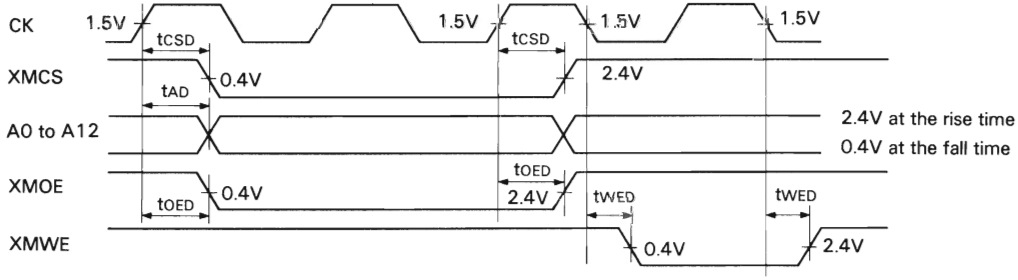
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF

AC Characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, Topr = −20 to +75°C, C_L = 60 pF

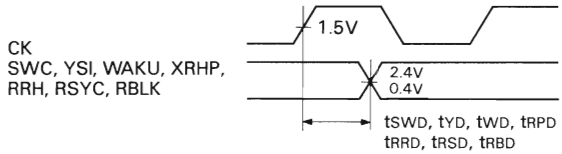
Item	Symbol	Min.	Max.	Unit
Parent picture clock frequency	f_{CK}		7.5	MHz
Picture-in-picture clock frequency	f_{SCK}		5.0	MHz
Output delay time, CK → XMCS	t_{CSD}		95	ns
Output delay time, CK → A0 to A12	t_{AD}		95	ns
Output delay time, CK → XMOE	t_{OED}		95	ns
Output delay time, CK → XMWE	t_{WED}		65	ns
Output delay time, CK → SWC	t_{SWD}		70	ns
Output delay time, CK → YSI	t_{YD}		70	ns
Output delay time, CK → WAKU	t_{WD}		70	ns
Output delay time, CK → XRHP	t_{RPD}		95	ns
Output delay time, CK → RRH	t_{RRD}		70	ns
Output delay time, CK → RSYC	t_{RSD}		70	ns
Output delay time, CK → RBLK	t_{RBD}		70	ns
Output delay time, SCK → XYC, XBYC, XRYC	t_{YCD}, t_{BYD}, t_{RYD}		70	ns
Output delay time, SCK → SPC	t_{SPD}		70	ns
Output delay time, SCK → WRH	t_{WRD}		70	ns
Output delay time, SCK → WBLK	t_{WBD}		70	ns
Microcomputer interface, clock width	t_{WH}	250		ns
Microcomputer interface, data set-up time	t_{DS}	250		ns
Microcomputer interface, data hold time	t_{DH}	250		ns
Microcomputer interface, enable set-up time	t_{ES}	250		ns
Microcomputer interface, enable hold time	t_{EH}	250		ns
Microcomputer interface, enable inhibitive time	t_{ER}		250	ns

Memory Relationship

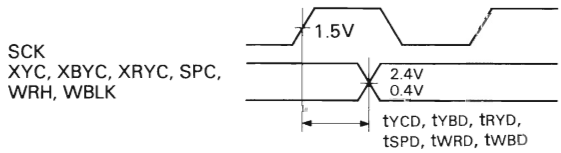


* t_{AD} is specified at A0 to A12 when switching read/write address.
It is specified at A0 to A4 during address counting up.

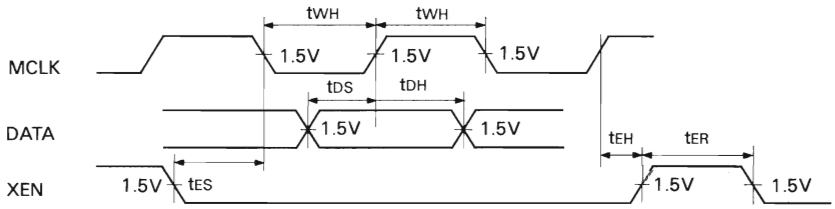
Delay from CK



Delay from SCK



Microcomputer Interface



Description of Functions

The CXD1053S and CXD1054S are ICs designed to execute the TV picture-in-picture or multi-picture function. These two ICs constitute the system in combination with an A/D converter, D/A converter and static RAM.

(1) System function

The picture-in-picture refers to a small inset picture in the usual TV picture. While watching a TV program, another TV channel can be watched in the inset picture. Here, we refer to the usual TV picture as "parent picture" and to the inset picture as "picture-in-picture" or "subsidiary picture". "Multi-picture" means several inset pictures displayed at the same time on the screen. The system using CXD1053S and CXD1054S has the following functions.

- Multi-picture (4-picture) display

  All subsidiary pictures can be still-pictures, or they can be 3 still-pictures and one motion picture. The parent picture is always in motion.

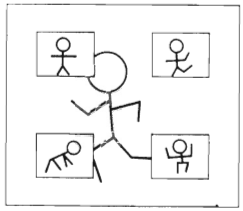
- Vertical 3-picture display

  The subsidiary pictures can be all still-pictures or 2 still-pictures and 1 motion picture. The 3-picture display location can be shifted either to the right or left.

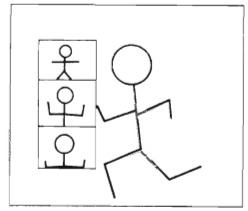
- Picture-in-picture (single picture) display

  The single subsidiary picture can be either still or in motion. It can be displayed in any corner of the parent picture.

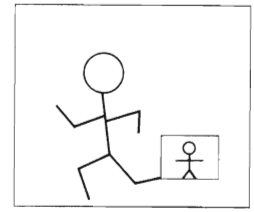
Multi-picture display



Vertical 3-picture display



Picture-in-picture display



(2) Resolution of the subsidiary pictures

The inset pictures have the following resolutions.

- Y signal 96 dots (horizontal) × 64 dots (vertical)
- R-Y signal 48 dots (horizontal) × 64 dots (vertical)
- B-Y signal 48 dots (horizontal) × 64 dots (vertical)
- Gradation 5-bit resolution
- Picture size Approx. 1/9 of the parent picture (in area)

(3) System configuration and operation

This system requires, in addition to the CXD1053S and CXD1054S, the A/D and D/A converter circuits, sync signal generating AFC circuit and the static RAM for storing data.

The A/D and D/A converters require 5-bit resolution and the static RAM requires four 2K × 8 bit for the picture-in-picture function and four 8K × 8 bit for the multi-picture function. The following is a description of operations along the inset picture signal flow.

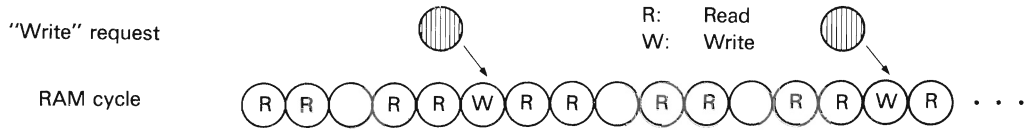
The inset picture image signals (analog Y signal, R-Y signal and B-Y signal) are time-divided and multiplexed by the switch circuit prior to the A/D converter. The converter changes the signals into 5-bit digital data and they are input to the CXD1054S. Through internal serial/parallel conversion, 6 samples (6 × 5 bit = 30 bit) of the 5-bit digital data are output together by the CXD1054S and written to the RAM. The RAM data is read out in 30 bits at a time with appropriate timing, and input to the CXD1054S again; then they are parallel/serial converted internally and output with Y, B-Y, R-Y signals, each in 5-bit data. The outputs are specified data at locations other than the inset display screen. The boundary between the parent picture and the inset is circled by a specified color and gradation line called "WAKU" (frame).

The CXD1054S controls data and the CXD1053S generates the reference timing signal, RAM address signal and control signals. The picture display mode is switched by setting the control switch incorporated in the CXD1053S.

(4) Operation of CXD1053S

The CXD1053S is called a memory control LSI as it generates the control signals required for the CXD1054S, A/D and D/A converters and RAM address.

RAM is not able to write and read simultaneously. With a clock reference, time can be preprogrammed to proceed in an order of "write", "read", "read", "write", "read" ... for example. The read is given priority over the write and a write has to wait sometimes until the next turn even when the write is required. This is possible because, in terms of the RAM access cycle, a write (an operation of writing data on the RAM — data made by A/D conversion of the inset picture signal) is executed slower than a read (the inset picture data are D/A converted and superimposed on the parent picture). This is described in the following schematic diagram.



As the write address generating circuit is provided separately from the read address generating circuit, a proper picture is displayed even if the write address is different from the read address, i.e. even if the inset picture's horizontal and vertical syncs are not in sync with those of the parent picture.

(5) Microcomputer interface

The CXD1053S has the internal (8-bit) control register and it is able to write the control data using three signal lines, DATA, MCLK and XEN. The 8-bit data is read serially in the IC shift register with the rise of MCLK.

The shift register operates only while the XEN is "L" and the shift register content is latched with the rise of XEN. Each bit has the following meaning.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Motion picture select		Still picture Motion picture	Inset picture display No display	Mode, location switching			Not in use

D_3	D_2	D_1	(Mode)	(Inset location)
0	0	0	Picture-in-picture	Bottom right
0	0	1	Picture-in-picture	Top right
0	1	0	Picture-in-picture	Bottom left
0	1	1	Picture-in-picture	Top left
1	0	0	Vertical 3-picture	Right
1	1	0	Vertical 3-picture	Left
1	1	1	Multi-picture	4 insets

D_5: 1 Still picture, 0 Motion picture

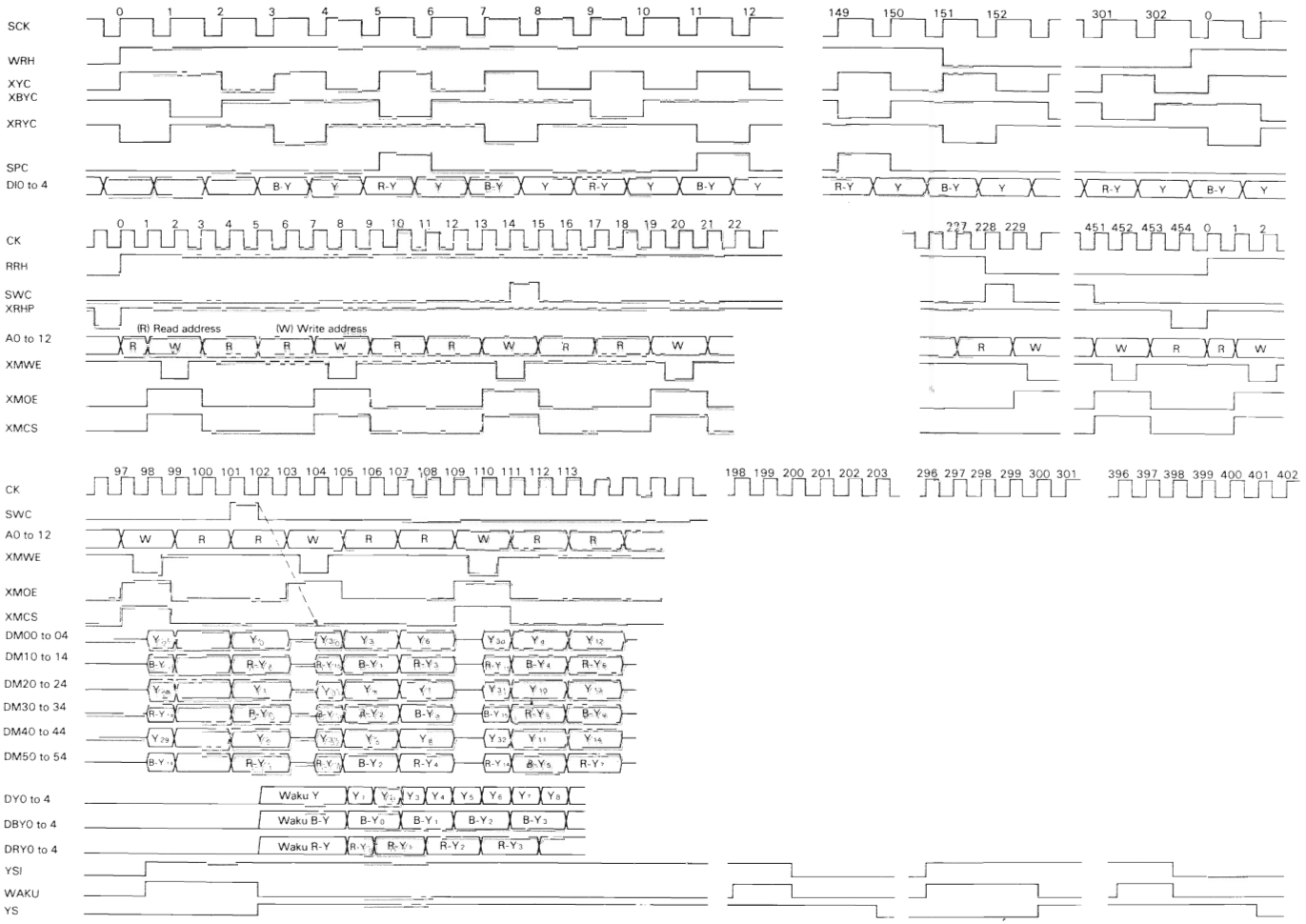
D_4: 1 Inset display, 0 No inset display

D_7	D_6	(Motion picture location)
0	0	Bottom right
0	1	Top right
1	0	Bottom left
1	1	Top left
1	1	Top
1	0	Center
0	0	Bottom

* Motion picture when selected with D_6 or D_7. Still pictures when selected with others.
(In the multi-picture mode)

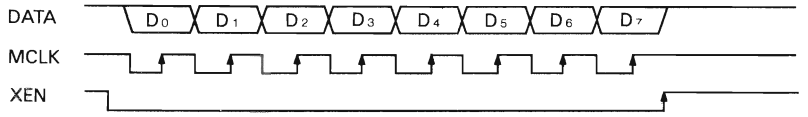
(In the vertical 3-picture mode)

Timing Chart

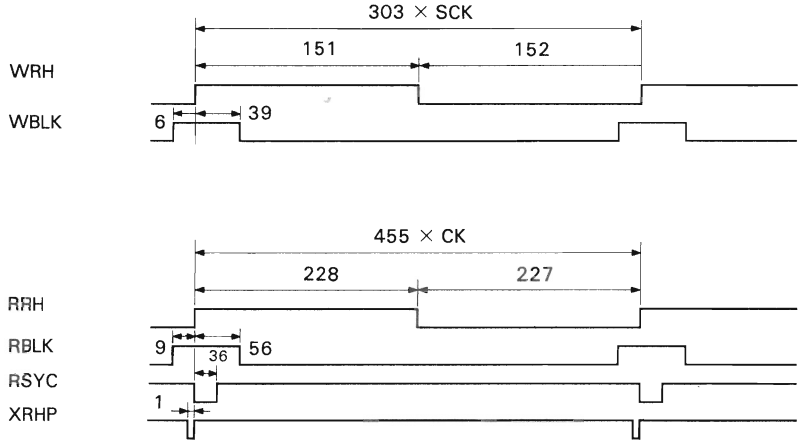


SONY

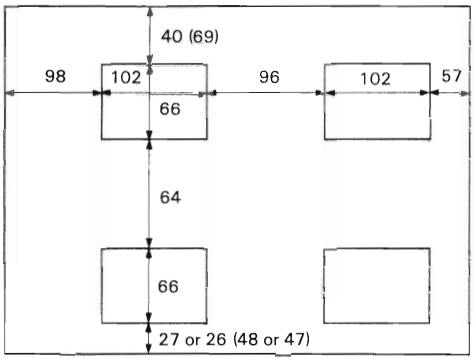
Microcomputer Interface



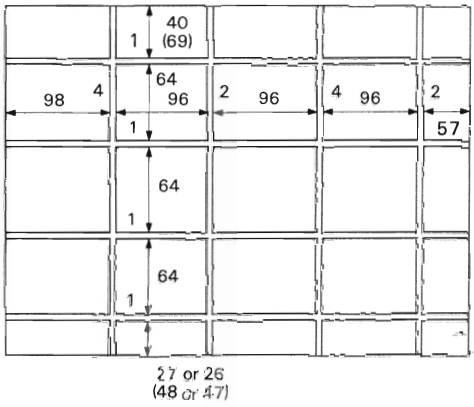
Phase Relationship of Horizontal Sync Signals



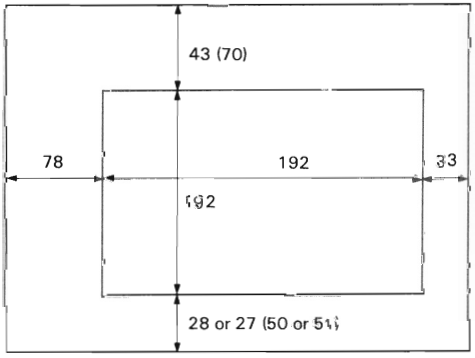
YSI Timing



WAKU Timing

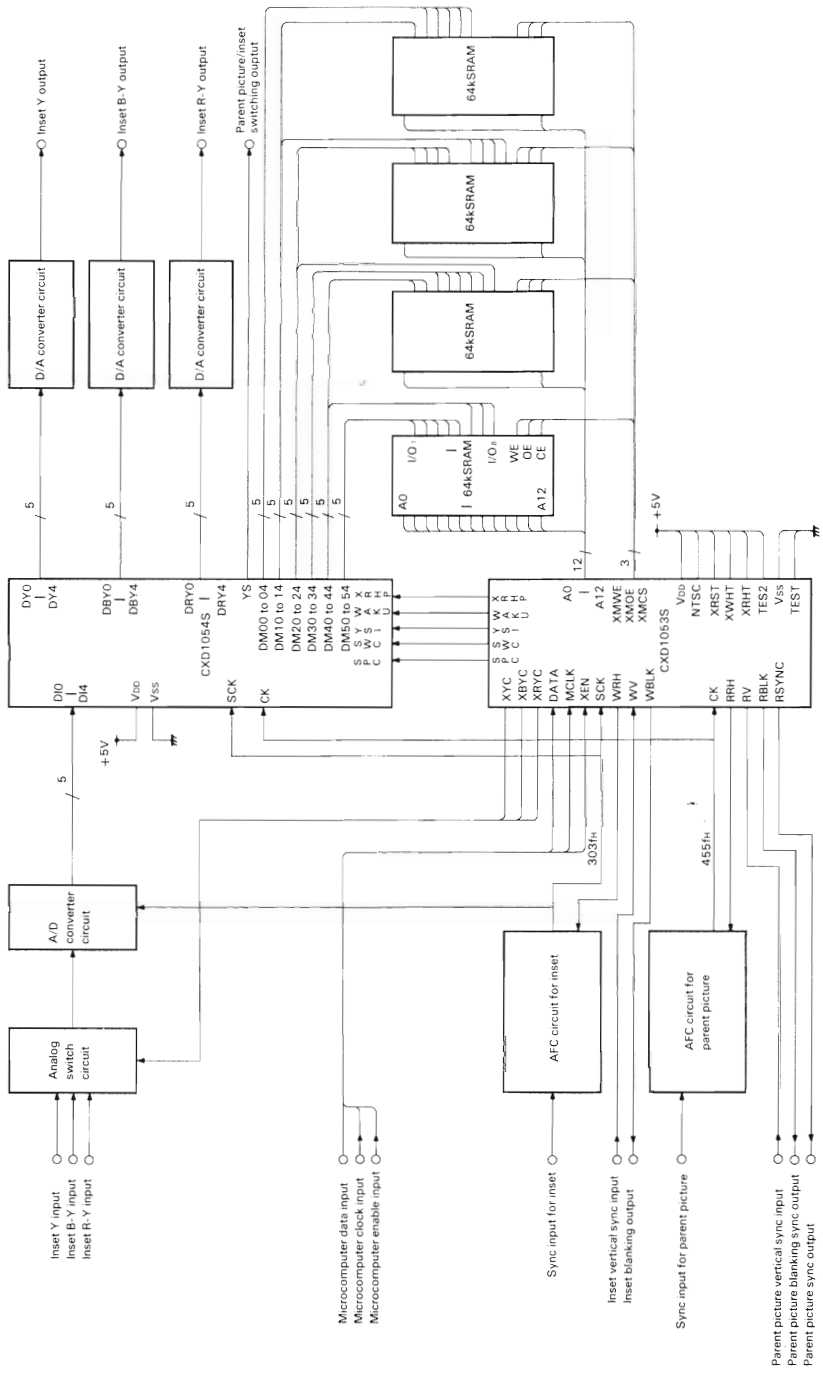


Write Area



* Values are indicated in the NTSC mode. The PAL mode values are shown in ( ).

Application Circuit



Picture-in-Picture Data Control IC for TV

Description

The CXD1054S is a TV data control IC designed for picture-in-picture or multi-picture functions. It is used in combination with the CXD1053S

Functions

Serial/parallel, parallel/serial conversions of video data

Structure

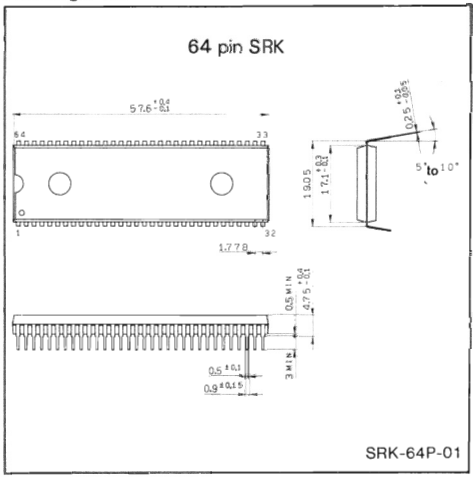
Silicon gate CMOS IC

Applications

Picture-in-picture TV
Multi-picture TV

Package Outline

Unit: mm



Absolute Maximum Ratings (Ta = 25°C)

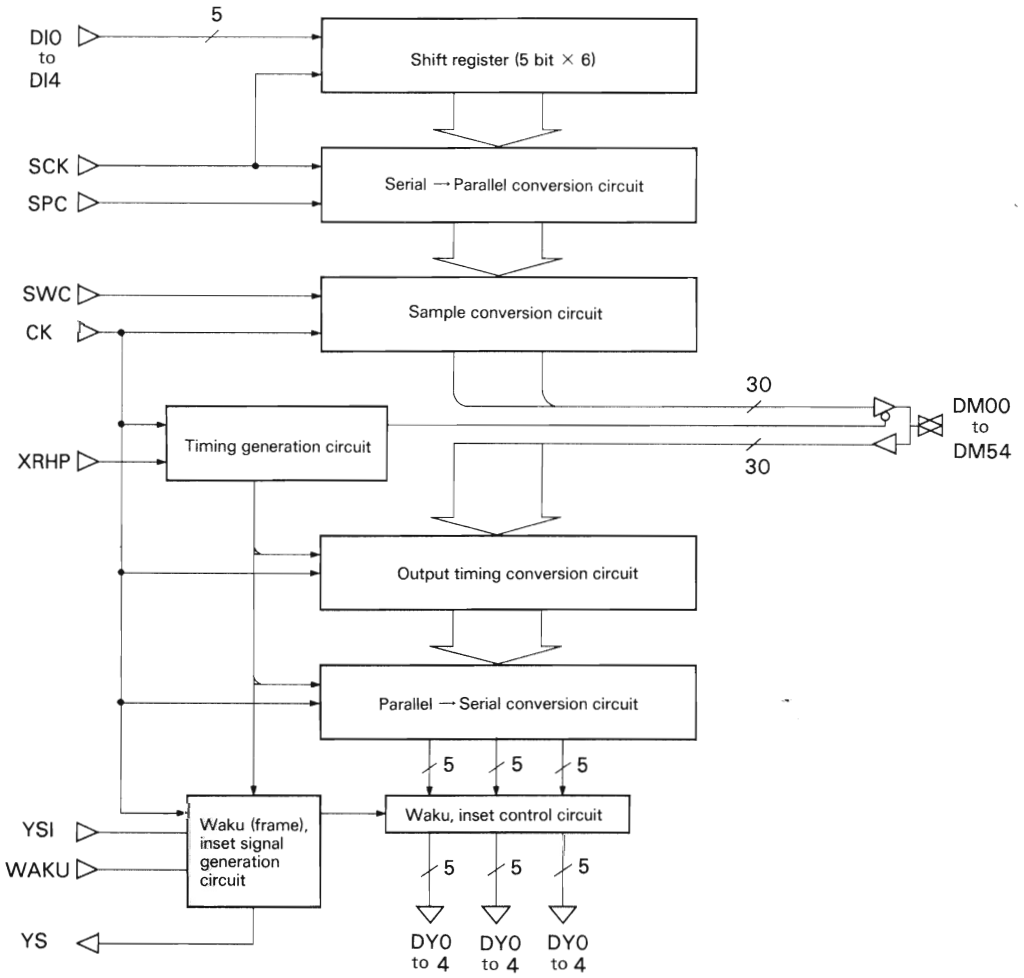
• Supply voltage	V_{DD}	V_{SS}*	−0.3 to 7.0	V
• Input voltage	V_I	V_{SS}*	−0.3 to V_{DD}+0.3	V
• Ootput voltage	V_O	V_{SS}*	−0.3 to V_{DD}+0.3	V
• Operating temperature	Topr		−20 to +75	°C
• Storage temperature	Tstg		−55 to +150	°C

*Note) V_{SS} = 0V

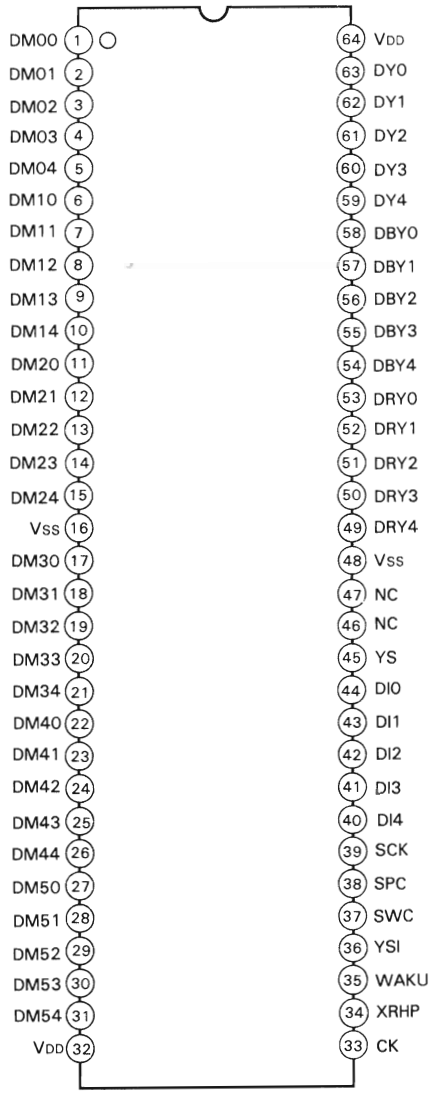
Recommended Operating Conditions

• Supply voltage	V_{DD}	5.0 ± 0.5	V
• Operating temperature	Topr	−20 to +75	°C

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	I/O	Description
1	DM00	I/O	Data pin connecting with external memory. Luminance signal data.
2	DM01	I/O	Data pin connecting with external memory. Luminance signal data.
3	DM02	I/O	Data pin connecting with external memory. Luminance signal data.
4	DM03	I/O	Data pin connecting with external memory. Luminance signal data.
5	DM04	I/O	Data pin connecting with external memory. Luminance signal data.
6	DM10	I/O	Data pin connecting with external memory. Luminance signal data.
7	DM11	I/O	Data pin connecting with external memory. Luminance signal data.
8	DM12	I/O	Data pin connecting with external memory. Luminance signal data.
9	DM13	I/O	Data pin connecting with external memory. Luminance signal data.
10	DM14	I/O	Data pin connecting with external memory. Luminance signal data.
11	DM20	I/O	Data pin connecting with external memory. Luminance signal data.
12	DM21	I/O	Data pin connecting with external memory. Luminance signal data.
13	DM22	I/O	Data pin connecting with external memory. Luminance signal data.
14	DM23	I/O	Data pin connecting with external memory. Luminance signal data.
15	DM24	I/O	Data pin connecting with external memory. Luminance signal data.
16	V_{SS}	—	GND
17	DM30	I/O	Data pin connecting with external memory. Color difference data.
18	DM31	I/O	Data pin connecting with external memory. Color difference data.
19	DM32	I/O	Data pin connecting with external memory. Color difference data.
20	DM33	I/O	Data pin connecting with external memory. Color difference data.
21	DM34	I/O	Data pin connecting with external memory. Color difference data.
22	DM40	I/O	Data pin connecting with external memory. Color difference data.
23	DM41	I/O	Data pin connecting with external memory. Color difference data.
24	DM42	I/O	Data pin connecting with external memory. Color difference data.
25	DM43	I/O	Data pin connecting with external memory. Color difference data.
26	DM44	I/O	Data pin connecting with external memory. Color difference data.
27	DM50	I/O	Data pin connecting with external memory. Color difference data.
28	DM51	I/O	Data pin connecting with external memory. Color difference data.
29	DM52	I/O	Data pin connecting with external memory. Color difference data.
30	DM53	I/O	Data pin connecting with external memory. Color difference data.
31	DM54	I/O	Data pin connecting with external memory. Color difference data.
32	V_{DD}	—	Power supply pin
33	CK	I	Clock input for parent (main) picture
34	XRHP	I	Horizontal reset pulse input for parent picture, connected with CXD1053S.
35	WAKU	I	Waku (frame) signal input, connected with CXD1053S.
36	YSI	I	Signal input for switching parent/inset picture, connected with CXD1053S.
37	SWC	I	Sample conversion signal input, connected with CXD1053S.
38	SPC	I	Serial/parallel conversion signal input, connected with CXD1053S.
39	SCK	I	Clock input for picture-in-picture
40	DI4	I	Data input from A/D converter (MSB)
41	DI3	I	Data input from A/D converter
42	DI2	I	Data input from A/D converter

No.	Symbol	I/O	Description
43	DI1	I	Data input from A/D converter
44	DI0	I	Data input from A/D converter (LSB)
45	YS	O	Parent (main) picture/inset switching signal output
46	NC	–	
47	NC	–	
48	V_{SS}	–	GND pin
49	DRY4	O	R-Y signal output (MSB)
50	DRY3	O	R-Y signal output
51	DRY2	O	R-Y signal output
52	DRY1	O	R-Y signal output
53	DRY0	O	R-Y signal output (LSB)
54	DBY4	O	B-Y signal output (MSB)
55	DBY3	O	B-Y signal output
56	DBY2	O	B-Y signal output
57	DBY1	O	B-Y signal output
58	DBY0	O	B-Y signal output (LSB)
59	DY4	O	Y signal output (MSB)
60	DY3	O	Y signal output
61	DY2	O	Y signal output
62	DY1	O	Y signal output
63	DY0	O	Y signal output (LSB)
64	V_{DD}	–	Power supply pin

Electrical Characteristics

DC Characteristics

V_{DD} = 5V ± 10%, V_{SS} = 0V, Topr = −20 to +75°C

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current		I_{DD}			15		mA
		I_{DDS}	Static state $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$			0.1	mA
Output voltage	H level	V_{OH}	I_{OH} = −0.4 mA	4.0		V_{DD}	V
	L level	V_{OL}	I_{OL} = 2.0 mA	V_{SS}		0.4	V
Input voltage	H level	V_{IH}		2.2			V
	L level	V_{IL}				0.8	V
Input leakage current		I_{IL}	V_I = 0V to V_{DD}	−10		10	μA
Output leakage current Three-state pin HIGH state		I_{LZ}		−10		10	μA

Input/Output Capacity

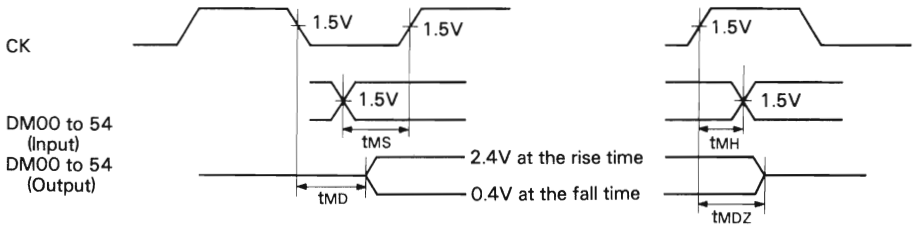
$V_{DD} = V_I = 0V, f = 1$ MHz

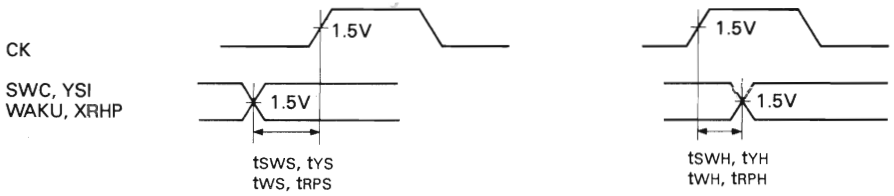
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF
Input/output pin	$C_{I/O}$			12	pF

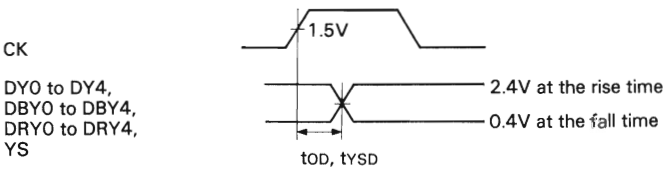
AC Characteristics

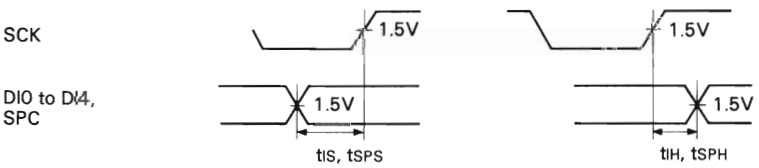
$V_{DD} = 5V \pm 10\%, V_{SS} = 0V, Topr = -20$ to $+75°C, C_L = 60$ pF

Item	Symbol	Min.	Typ.	Max.	Unit
Parent picture clock frequency	f_{CK}			7.5	MHz
Picture-in-picture Clock frequency	f_{SCK}			5.0	MHz
Memory data, input set-up time	t_{MS}	35			ns
Memory data, input hold time	t_{MH}	20			ns
Memory data, output delay time (C_L = 80 pF)	t_{MD}			105	ns
Memory data, output delay time	t_{MDZ}			140	ns
Digital data, input set-up time	t_{IS}	10			ns
Digital data, input hold time	t_{IH}	25			ns
Digital data, output delay time	t_{OD}			95	ns
SWC, input set-up time	t_{SWS}	40			ns
SWC, input hold time	t_{SWH}	10			ns
YSI, input set-up time	t_{YS}	50			ns
YSI, input hold time	t_{YH}	20			ns
XRHP, input set-up time	t_{RPS}	30			ns
XRHP, input hold time	t_{RPH}	20			ns
SPC, input set-up time	t_{SPS}	40			ns
SPC, input hold time	t_{SPH}	10			ns
WAKU, input set-up time	t_{WS}	50			ns
WAKU, input hold time	t_{WH}	20			ns
YS, output delay time	t_{YSD}			95	ns


CK
DM00 to 54 (Input)
DM00 to 54 (Output)
1.5V
1.5V
1.5V
tMS
2.4V at the rise time
0.4V at the fall time
tMD
1.5V
1.5V
tMH
tMDZ


CK
SWC, YSI
WAKU, XRHP
1.5V
1.5V
tSWS, tYS
tWS, tRPS
1.5V
1.5V
tSWH, tYH
tWH, tRPH


CK
DY0 to DY4,
DBY0 to DBY4,
DRY0 to DRY4,
YS
1.5V
2.4V at the rise time
0.4V at the fall time
tOD, tYSD


SCK
DI0 to DI4,
SPC
1.5V
1.5V
tIS, tSPS
1.5V
1.5V
tIH, tSPH

Description of Functions

The CXD1053S and CXD1054S are ICs designed to execute the TV picture-in-picture or multi-picture function. These two ICs constitute the system in combination with an A/D converter, D/A converter and static RAM.

(1) System function

The picture-in-picture refers to a small inset picture in the usual TV picture. While watching a TV program, another TV channel can be watched in the inset picture. Here, we refer to the usual TV picture as "parent picture" and to the inset picture as "picture-in-picture" or "subsidiary picture". "Multi-picture" means several inset pictures displayed at the same time on the screen. The system using the CXD1053S and CXD1054S has the following functions.

- Multi-picture (4-picture) display

  All subsidiary pictures can be still-pictures, or they can be 3 still-pictures and one motion picture. The parent picture is always in motion.

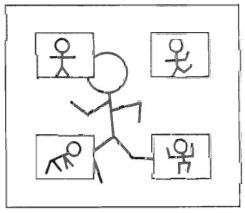
- Vertical 3-picture display

  The subsidiary pictures can be all still-pictures or 2 still-pictures and 1 motion picture. The 3-picture display location can be shifted either to the right or left.

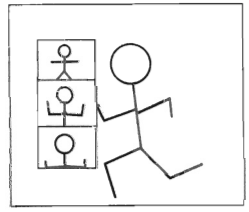
- Picture-in-picture (single picture) display

  The single subsidiary picture can be either still or in motion. It can be displayed in any corner of the parent picture.

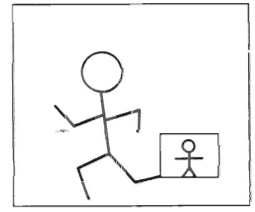
Multi-picture display



Vertical 3-picture disply



Picture-in-picture display



(2) Resolution of the subsidiary pictures

The inset pictures have the following resolutions.

- Y signal — 96 dots (horizontal) × 64 dots (vertical)
- R-Y signal — 48 dots (horizontal) × 64 dots (vertical)
- B-Y signal — 48 dots (horizontal) × 64 dots (vertical)
- Gradation — 5-bit resolution
- Picture size — Approx. 1/9 of the parent picture (in area)

(3) System configuration and operation

This system requires, in addition to the CXD1053S and CXD1054S, the A/D and D/A converter circuits, sync signal generating AFC circuit and the static RAM for storing data.

The A/D and D/A converters requires 5-bit resolution and the static RAM requires four 2K × 8 bit for the picture-in-picture function and four 8K × 8 bit for the multi-picture function. The following is a description of operations along the inset picture signal flow.

The inset picture image signals (analog Y signal, R-Y signal and B-Y signal) are time-divided and multiplexed by the switch circuit prior to the A/D converter. The converter changes the signals into 5-bit digital data and they are input to the CXD1054S. Through internal serial/parallel conversion, 6 samples (6 × 5 bit = 30 bit) of the 5-bit digital data are output together by the CXD1054S and written in the RAM. The RAM data is read out in 30 bits at a time with appropriate timing, and input to the CXD1054S again; then they are parallel/serial converted internally and output with Y, B-Y, R-Y signals, each in 5-bit data. The outputs are specified data at locations other than the inset display screen. The boundary between the parent picture and the inset is circled by a specified color and gradation line called "WAKU" (frame).

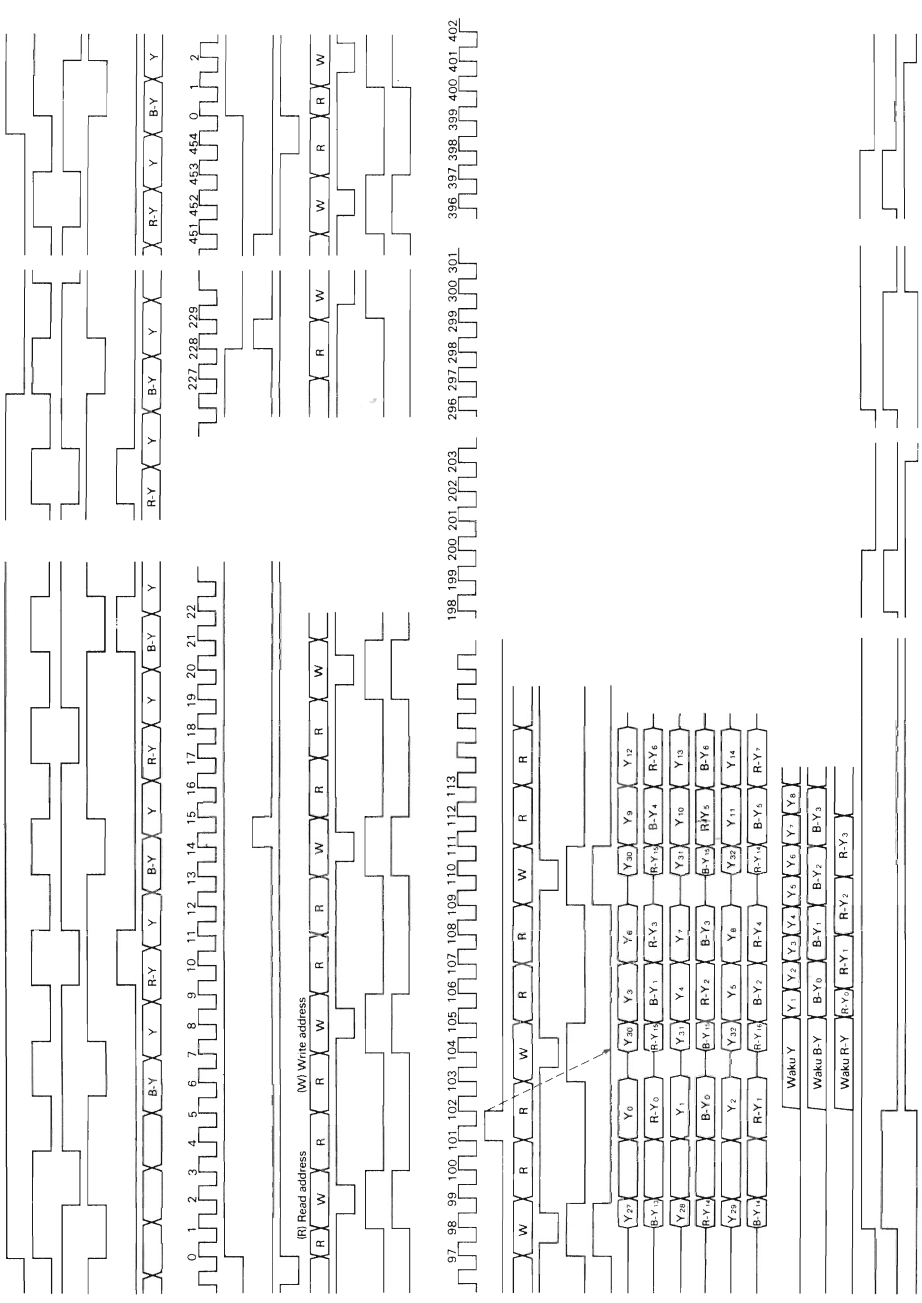
The CXD1054S controls data and the CXD1053S generates the reference timing signal, RAM address signal and control signals. The picture display mode is switched by setting the control switch incorporated in the CXD1053S.

(4) Operation of CXD1054S

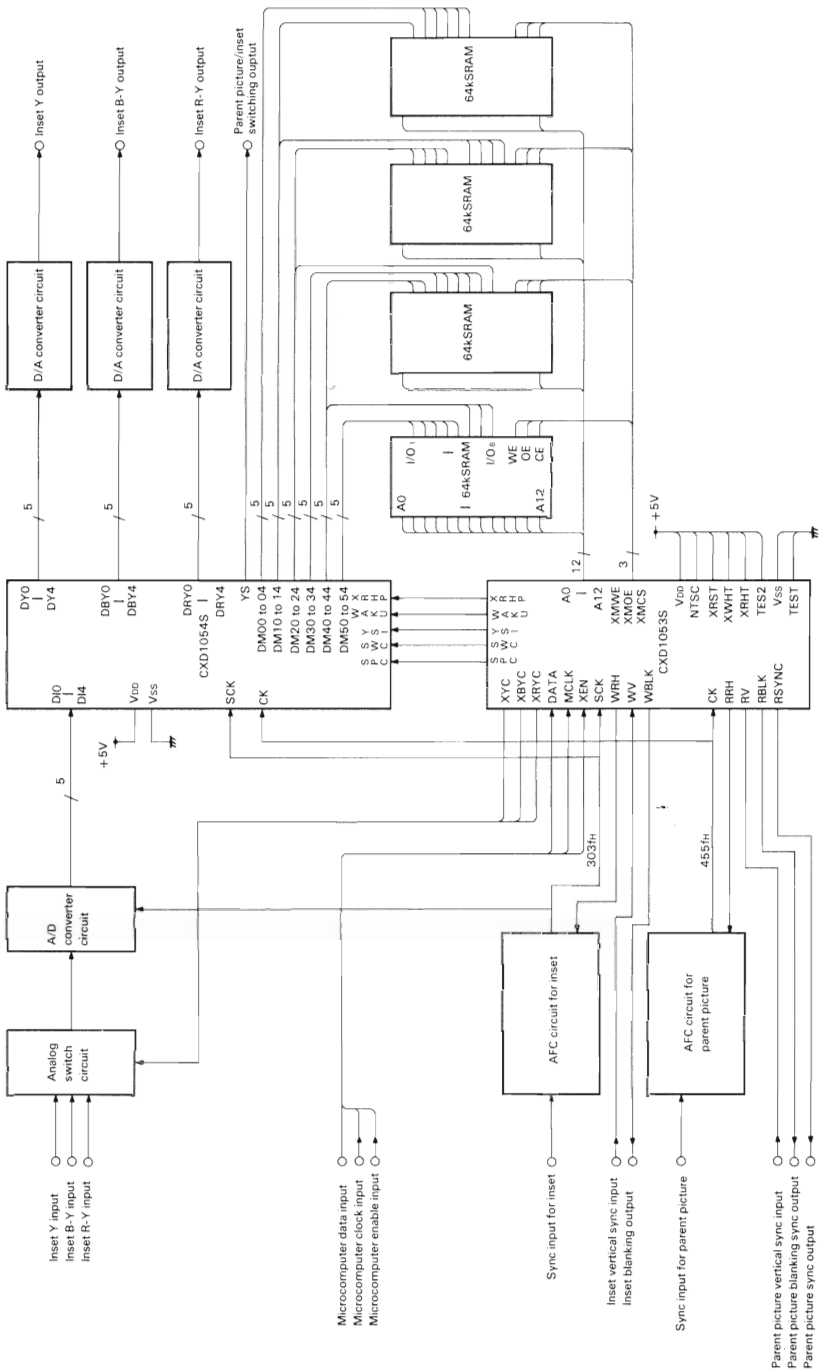
As the CXD1054S serial/parallel converts the video data, it is called a data control IC. 5-bit Y, R-Y, Y, B-Y, Y, R-Y (in this order) video data, time-divided by the A/D converter, are input. All 30-bit (5 bits × 6) data is written to RAM simultaneously in sync with the inset horizontal and vertical signals. Further, the 30-bit data is read at one time from RAM in sync with the parent picture's horizontal and vertical sync signals, and the Y, R-Y and B-Y signals are converted to parallel, each in 5 bits, to be output to the D/A converter. These 5-bit outputs are fixed as follows, except for the inset pictures.

	(Y)	(B-Y)	(R-Y)
	DY4 to DY0	DBY4 to DBY0	DRY4 to DRY0
'Parent picture'	00000	10000	10000
'Waku'	11000	10000	10000

Timing Chart



Application Circuit



SONY

CXK1201P

Double Scan Converter

Preliminary

Description

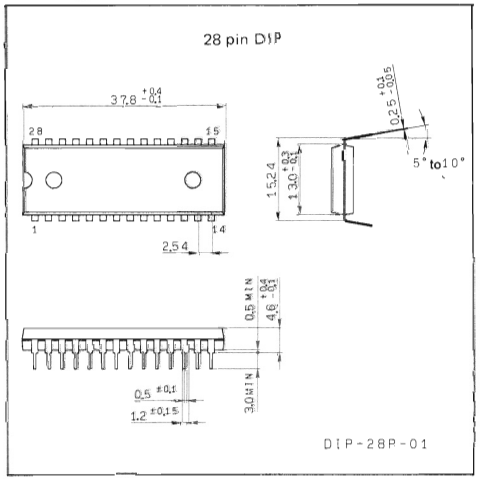
The CXK1201P is a digital line memory for non-interlace TV 8-bit structure which employs silicon gate CMOS process. It is enabled to perform line interpolation and scan conversion of horizontal frequency.

Features

- Most suitable to the digital TV system of its sampling frequency of 4 fsc (NTSC).
- Incorporates H sync, H blanking, clock for A/D converter and clear signal generation circuit to synchronize with external circuit.
- Memory structure 910×8×2 bit
- High speed cycle time
  - Minimum write cycle time 66 ns
  - Minimum read cycle time 33 ns
- I/O level Compatible with TTL level
- Data output three states
- 5V single power supply
- Low power consumption 200 mW (typ.)

Package Outline

Unit: mm



Function

Double scan conversion

Structure

Silicon gate CMOS

Application

Double scan monitor

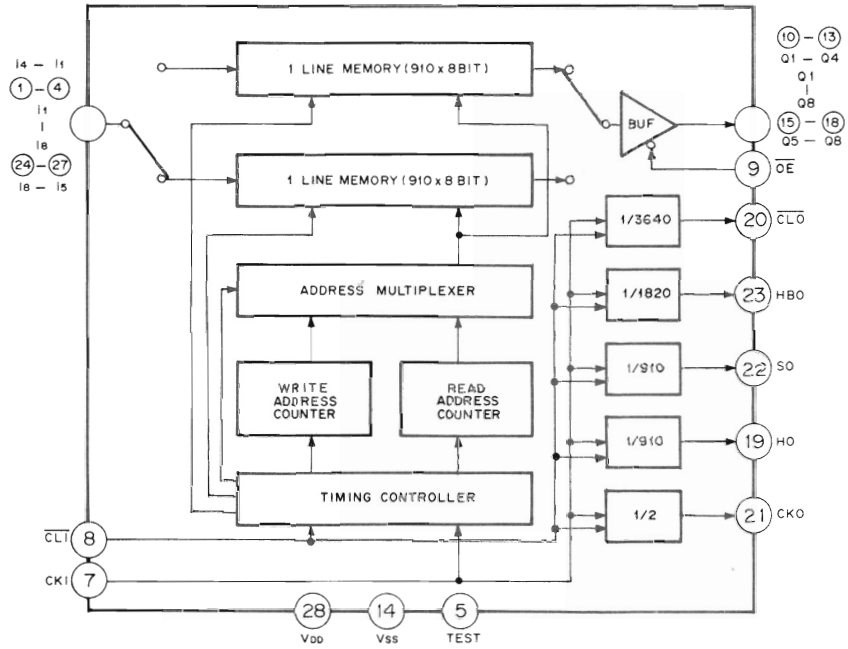
Absolute Maximum Ratings

• Supply voltage	V_{DD}	−0.3 to +7.0	V
• Input voltage	V_{IN}	−0.3 to +7.0	V
• Operating temperature	Topr	−10 to +85	°C
• Storage temperature	Tstg	−55 to 150	°C
• Allowable power dissipation	P_D	500	mW

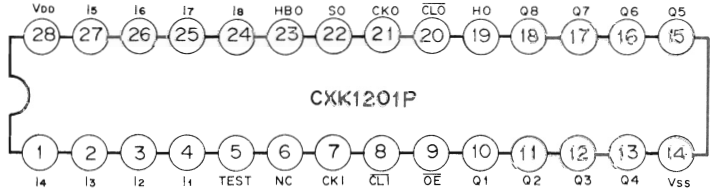
Recommended Operating Conditions (Ta=0 to +70°C)

• Supply voltage	V_{DD}	4.5 to 5.5	V (5.0V Typ.)
• Supply voltage	Vss	0	V
• Input voltage "H" level	V_{IH}	2.4 to V_{DD}+0.3	V
• Input voltage "L" level	V_{IL}	−0.3 to +0.8	V

Block Diagram



Pin Configuration (Top View)



Pin Description

No.	Symbol	Description
1 – 4	I4 – I1	Data input
5	TEST	Test signal input
6	NC	Non-connection
7	CKI	Clock input
8	$\overline{CLI}$	Clear input
9	$\overline{OE}$	Output enable input
10 – 13	Q1 – Q4	Data output
14	V_{SS}	Ground
15 – 18	Q5 – Q8	Data output
19	HO	2H output (The same frequency as H sync, duty 50%)
20	$\overline{CLO}$	Clear output
21	CKO	Clock output (Frequency is 1/2 of CKi)
22	SO	H sync output
23	HBO	H blanking output
24 – 27	I8 – I5	Data input
28	V_{DD}	Power supply (+5V)

Pin Function

(1) I1 to I8 (Input)
The data inputs. The data set up time and hold time are determined from the rising edge of the clock.

(2) Q1 to Q8 (Output)
The data outputs. The access time is determined from the rising edge of the clock.

(3) CKI (Input)
A lock input. The I/O timing of the respective signals are defined against the clock which has been input from this pin.

(4) $\overline{CLI}$ (Input)
A clear input. The input which is used in order to initialize the write address and read address. When it is necessary to synchronize with the externals (data inputs), there are two ways, the one is to use this clear input and the other is to use the H blanking signal which will be described later in this description.

(5) $\overline{OE}$ (Input)
An output enable. When it is at "L" level, the data outputs (Q1 to Q8) become into output mode. When at "H" level, they become into high impedance state.

(6) $\overline{CLO}$ (Output)
A clear output. When plural numbers of this LSI are used in parallel, it is possible to synchronize with the respective LSIs by inputting the clear output of which is specified as the reference, to the clear inputs of other LSIs.

(7) CKO (Output)
A clock output pin. The frequency is 1/2 that of the input colck signal and is possible to be used as clock of the A/D converter.

(8) SO (Output)
An H SYNC signal output pin. It is possible to be used as a signal to synchronize the data output and monitor. However, this signal is an H SYNC signal during double speed (The frequency is twice as much as that of normal.)

(9) HO (Output)
A signal output pin which outputs the signal of 50% duty and whose frequency is equivalent to the H SYNC signal.

(10) HBO (Output)
A H blanking signal output pin. It is possible to be used as a synchronizing signal with the data input signal.

(11) TEST (Input)
A test signal input pin. It is a pin used during the test of LSI and is normally used at "H" level.

(12) V_{DD}
The power supply pin. (+5V)

(13) V_{SS}
The grounding pin.

Electrical Characteristics

DC characteristics

V_{DD}=5.0V, Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Power supply current (active)	I_{DD}	—	—	70	mA	
Input leakage current	I_{IL}	−2	—	2	μA	V_{IN}=0V − V_{DD}
Output leakage current	I_{OL}	−2	—	2	μA	V_{OUT}=0V − V_{DD}
Output voltage "H" level	V_{OH}	2.7	—	—	V	I_{OH}=−400μA
Output voltage "L" level	V_{OL}	—	—	0.4	V	I_{OL}=4.0mA

AC characteristics

V_{DD}=4.5V to 5.5V, Ta=0°C to 70°C
(See the timing chart on next page)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Data set up time	t_{dsu}	0			ns	
Data hold time	t_{dh}	25			ns	
$\overline{CLI}$ set up time	t_{csu}	10			ns	
$\overline{CLI}$ hold time	t_{ch}	5			ns	
Clock pulsewidth	t_{ckw}	15			ns	Low or high

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency	f			30	MHz	C_L=30pF
From clock input to determination of Q1 – Q8	t_{pda}	7		25	ns	
From $\overline{OE}$ input to determination of Q1 – Q8	t_{pdb}	7		25	ns	
From clock input to determination of CKO	t_{pdc}	7		25	ns	
From clock input to determination of $\overline{CLO}$	t_{pdd}	7		25	ns	
From clock input to determination of SO	t_{pde}	7		25	ns	
From clock input to determination of HBO	t_{pdf}	7		25	ns	
From clock input to determination of HO	t_{pdg}	7		25	ns	
Output disable time (from $\overline{OE}$)	t_{pdh}	7		25	ns	
Output enable time (from $\overline{OE}$)	t_{pdi}	7		25	ns	

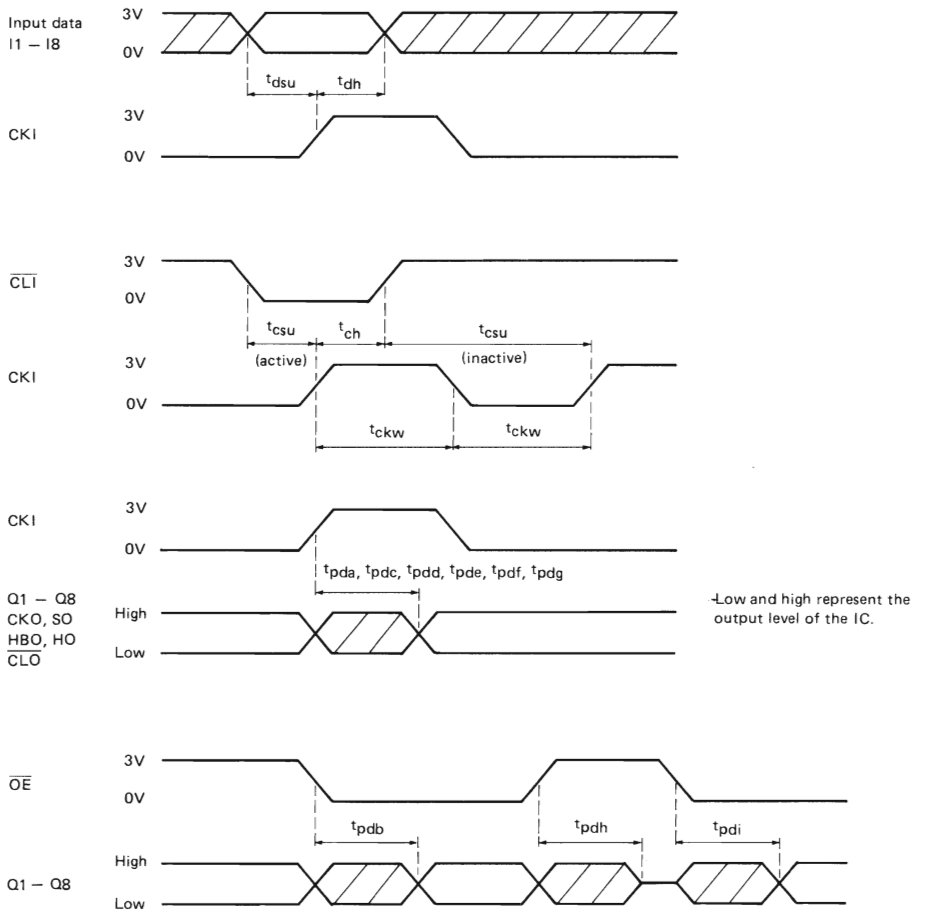
Pin capacitance

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Input capacitance	C_{IN}			7	pF	Ta=25°C, f=1MHz
Output capacitance	C_{OUT}			10	pF	V_{IN}=V_{OUT}=0V

Timing chart

(1) Input signal levels are at the low level = 0V and at the high level = 3V, and 5 ns for both rising and falling time.

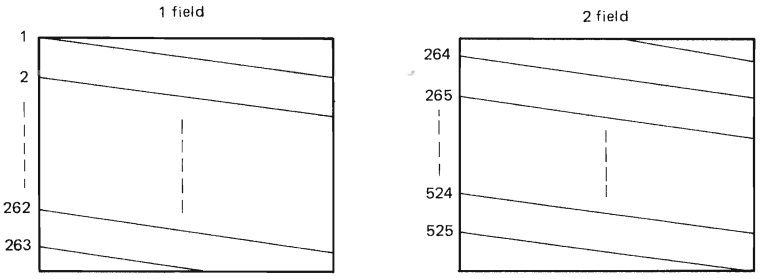
(2) The voltage judging levels of both low and high are 1.5V.



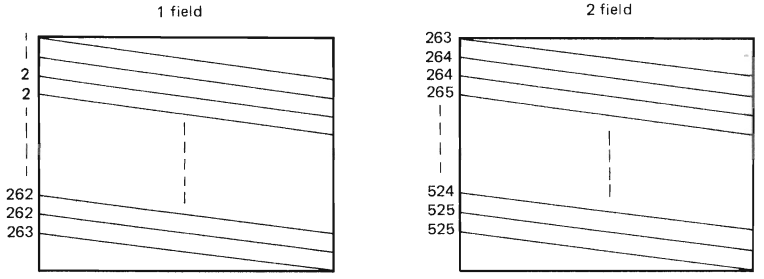
Description of Operation

The video signal of the NTSC format performs interlacing with one field 525/2 scanning lines. Accordingly, to perform scan conversion of horizontal frequency (one field 525 scanning lines), it is required to make line interpolation and the horizontal scanning frequency twice as much. The conceptual diagrams when performing the scan conversion by using a CXK1201P are as shown below.

NTSC format video signal



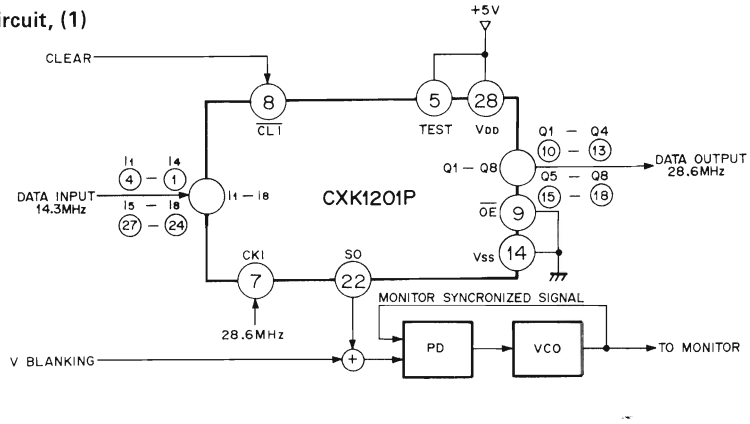
Video signal after being converted into scan conversion



An application example, which is provided as a reference in order to operate the converter in the manner as shown in the conceptual diagrams, is as shown in Fig. 1, and its timing chart is as shown in Fig. 2. At first, initialize the write address and read address of the CXK1201P by inputting clear signal. After that, by inputting the digital data having been sampled by $4f_{SC}$ (14.3 MHz), the data having been converted by double speed can be obtained in synchronization with the clock at $8f_{SC}$ (28.6 MHz).

Moreover, to synchronize with the monitor, carry out the phase comparison with the composite sync signal which is provided by adding the H sync signal generated from the CXK1201P and the V blanking signal extracted from the input data and the composite sync signal within the monitor, and by changing the frequency and phase of the composite sync signal within the monitor so as to make no differences in the phases.

Application circuit, (1)



PD : Phase Detector
VCO : Voltage Controlled Oscillator

Fig. 1

Double Speed Conversion Timing Chart

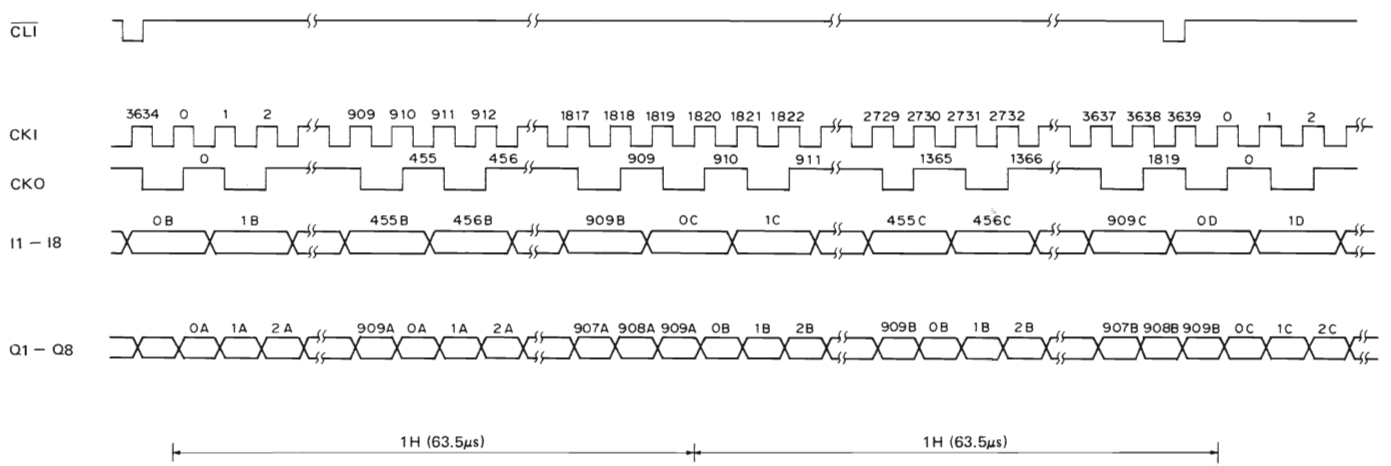


Fig. 2

Moreover, an application example when the clear input is not used is as shown in Fig. 3. In this case, extract the H sync signal from the input video signal and make the sync signal having the same frequency as the input H sync by the H blanking signal and HO signal from the CXK1201P. Perform the phase comparison of thus provided sync signal and change the frequency and phase of the clock (28.6 MHz) so as to make no difference in the phase.
In addition, the method to synchronize it with the composite signal of the monitor, the same procedures as using the clear input mentioned above should be taken.

Application circuit, (2)

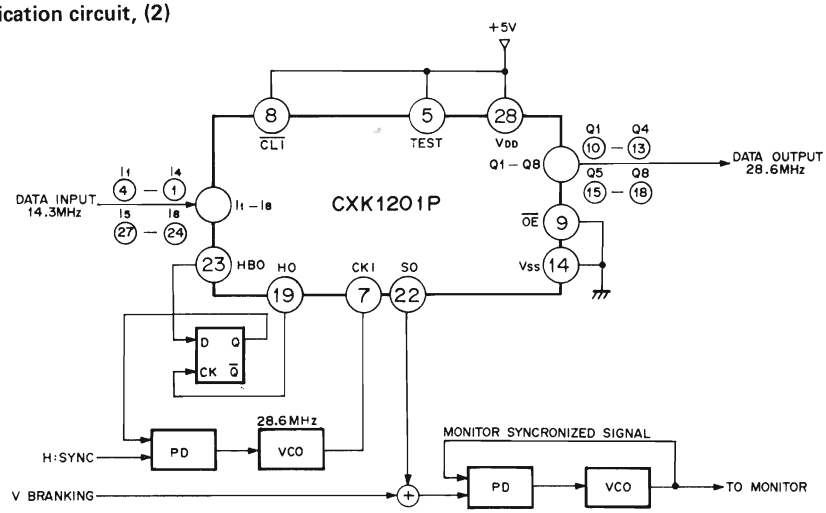


Fig. 3

The CXK1201P generates various kinds of synchronizing signals in order to synchronize with the external signals. The phase relationship between the synchronizing signals and their respective timings are shown in Figs. 4 and 5 respectively.

The phase relationship between the respective outputs

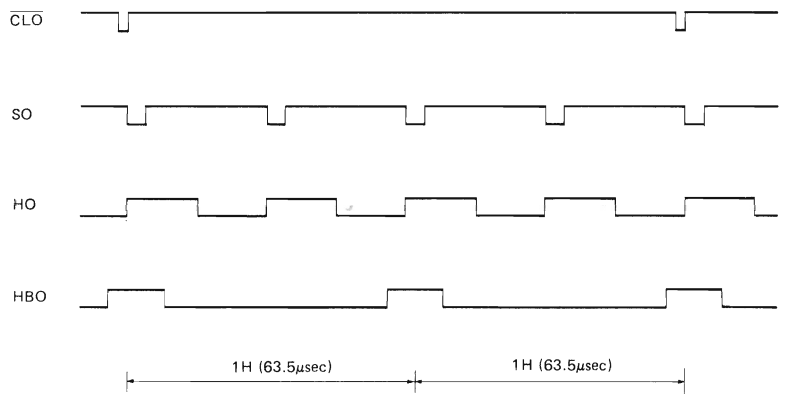


Fig. 4

The respective output timings against the input CKI

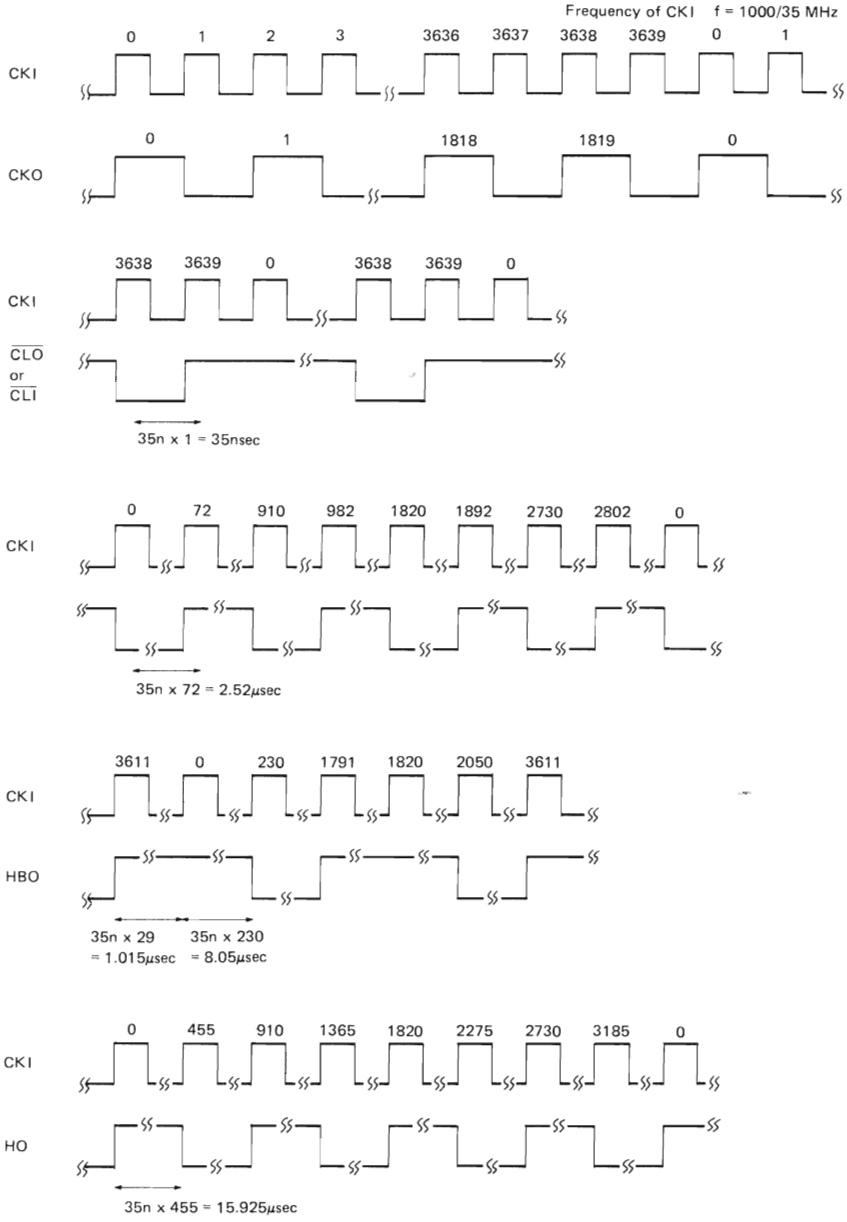


Fig. 5

SONY BX-1330/BX-1396

Infrared Ray Remote Control Receiver

Description

The BX-1330/BX-1396 is a highly sensitive infrared ray remote control receiver using the receiving preamplifier IC CX20106A for remote control.

Features

- The circuit function is combined into 1 block.
- Externally attached components are not necessary.
- It operates at low voltage and low power consumption.

Structure

Hybrid IC

Application

It can be used for TVs, VTRs, audio equipments, air conditioners, car stereo radios, toys, home computers and all other equipments requiring remote control.

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	6.3	V
• Storage temperature	Tstg	−20 to +60	°C

Recommended Operating Conditions

• Supply voltage	V_{CC}	4.7 to 5.3	V
• Operating temperature	Topr	−10 to +60	°C

Electrical Characteristics

(Ta=25°C, Vcc=5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	Icc	Non-signal input	1.1		2.5	mA
Arrival distance	L	*1. At optical axis	8.0	10.0		m
		As the light receiving side at the apex, against the optical axis	6.5			
		of within the range of 30° of the cone	5.0			
		of within the range of 45° of the cone				
Low level output voltage	VL	*2. At a distance of 30cm on the optical axis			0.5	V
High level output voltage	VH	*2. At a distance of 30cm on the optical axis	4.5			V
Low level pulse width	TWL	*1. Specifies with the TWL period width of the output within the range of 5cm to the arrival distance	410	660	910	μs
High level pulse width	TWH	*1. Specifies with the TWH period width of the output within the range of 5cm to the arrival distance	290	540	790	μs

Product name	Carrier wave frequency fo(kHz)*
BX-1330	40
BX-1396	38

* See the equivalent circuit and test circuit.
(The carrier wave frequency is possible to be matched to the fo of the transmitter side and shipped.)

*1. Within the arrival distance, the specified pulse width is satisfied under the following condition.

① Standard transmitter

With the output waveform indicated in Fig.1, and the transmitter output adjusted so that it becomes Vo=400 mVp-p by the measuring method shown in Fig.2, is called the standard transmitter.

However, the infrared LED for transmitter use should be λpeak=940 nm and Δλ=60 nm.

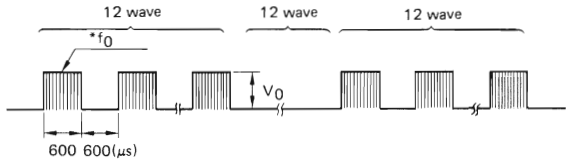


Fig. 1 Output waveform

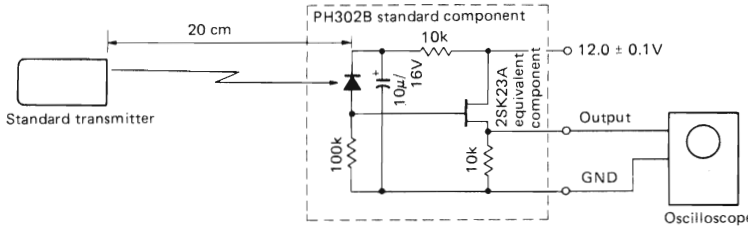


Fig. 2 Measuring method

② Pulse width measuring condition

By using the above-mentioned standard transmitter, it specifies the TWL period and the TWH period of the output pulse.

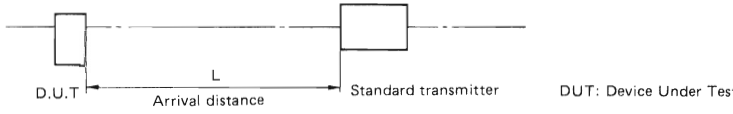


Fig. 3 Measuring condition

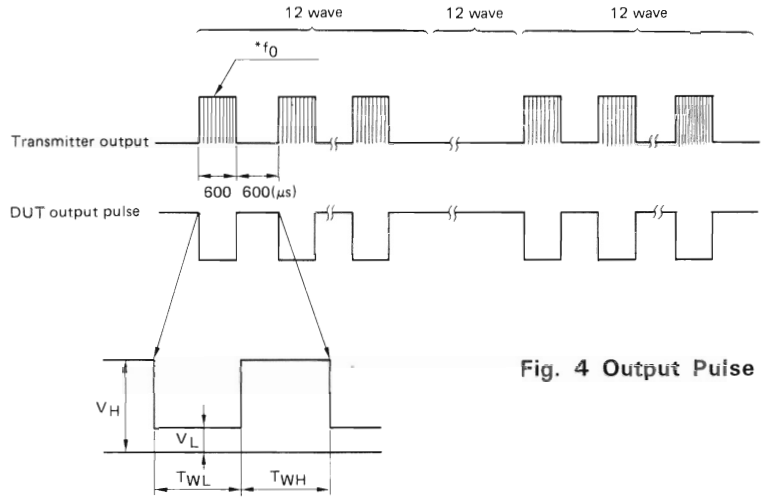
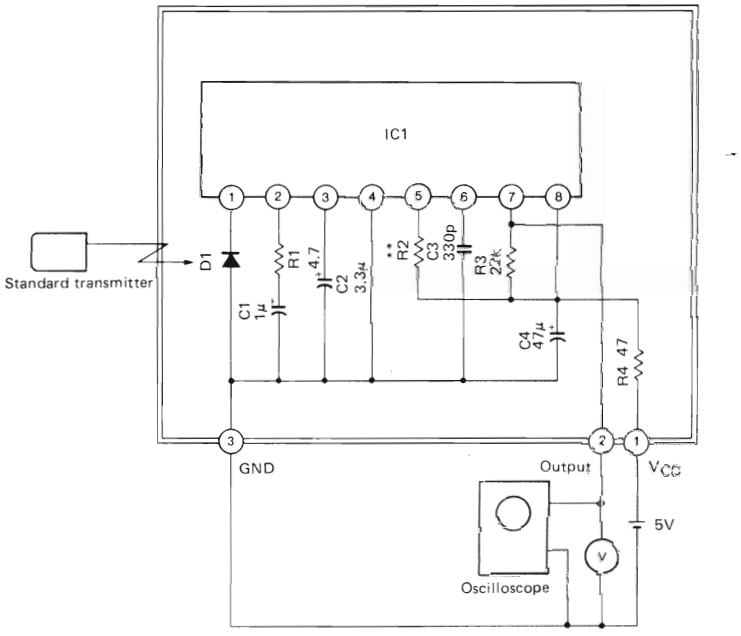


Fig. 4 Output Pulse

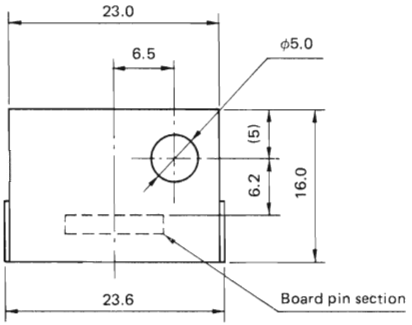
*2. The standard transmitter is the one determined by *1. The voltmeter used is Z=1.0 MΩ

Equivalent Circuit and Test Circuit

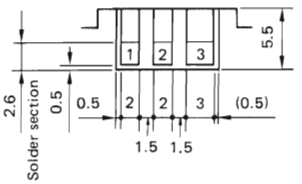


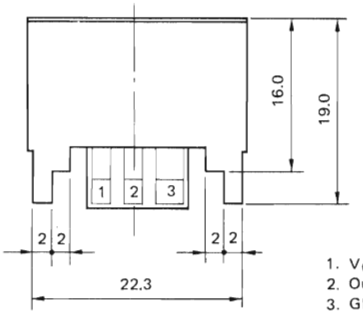
IC1:	CX20106A	1. V_{CC}
D1:	PIN photo diode	2. Output
C1, C2 and C4:	Electrolytic aluminum capacitor	3. GND
C3:	SL characteristics ± 5%	
R2:	± 1% (Adjusted resistor)	
R (Other than above):	± 5%	

Package Outline and Indication

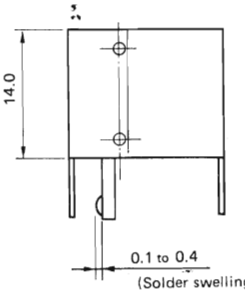


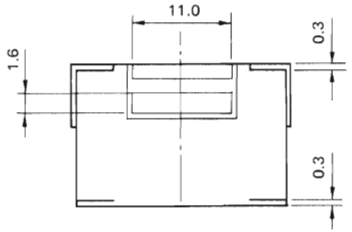
Unit: mm
General tolerance: ± 0.3

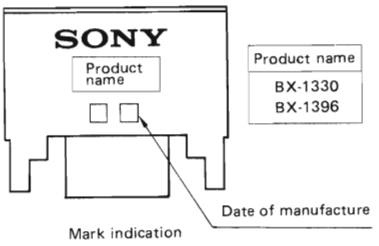




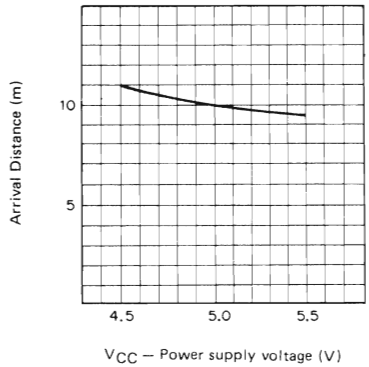
1. V_{CC}
2. Output
3. GND



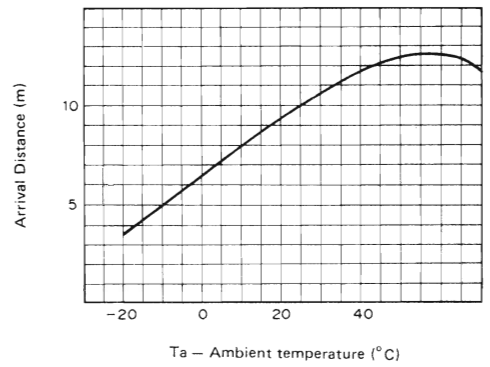




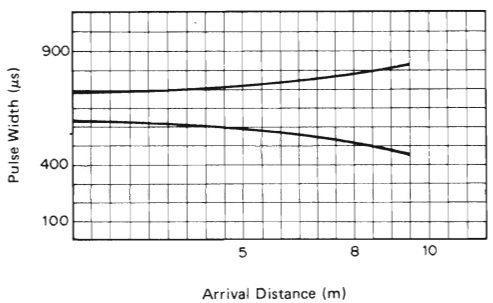
Arrival distance vs. Power supply voltage



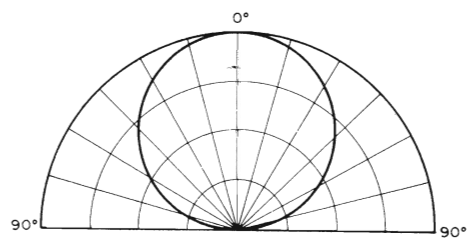
Arrival distance vs. Ambient temperature



Distribution of Arrival Distance and Pulse Width



Directivity



SONY BX-1387/BX-1407

Infrared Remote Control Receiver

Description

The BX-1387/BX-1407 is a small type infrared remote control system receiver which has been developed and designed by utilizing the latest hybrid technology .

It is a single unit type module which incorporates a pin photo diode and a receiving preamplifier IC (CX20106A).

Features

- A cubic type easy to handle small module
  - —The receiving preamplifier CX20106A which has been developed by SONY Corp. and a pin photo diode are mounted into a single unit type.
  - —Enable to be installed directly to the set panel.
- Externally attached parts are unnecessary.
- It can be operated by low voltage and low power consumption.

Structure

Hybrid IC

Application

- It can be used for TV, VTR, acoustic devices, air conditioners, car stereo units, home computers, interior controlling appliances, and all other appliances which require remote controlling.

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	6.3	V
• Storage temperature	Tstg	−20 to +60	°C
• Operating temperature	Topr	−10 to +60	°C

Recommended Operating Condition

• Supply voltage	V_{CC}	4.7 to 5.3	V

Electrical Characteristics

(Ta=25°C, Vcc=5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	Icc	No signal input	1.1		2.5	mA
Arrival distance	L	*1. At the ray axis	8.0	10.0		m
		The ray receiving surface being at a vertex and against the ray axis: In the range of the cone of 30°	6.5			
		In the range of the cone of 45°	5.0			
Low level output voltage	VL	*2. In the distance of 30 cm on the ray axis			0.5	V
High level output voltage	VH	*2. In the distance of 30 cm on the ray axis	4.5			V
Low level pulse width	TWL	*1. Specified by the TWL period of output within the range of 5 cm to the arrival distance.	410	660	910	μs
High level pulse width	TWH	*1. Specified by the TWH period of output within the range of 5 cm to the arrival distance.	290	540	790	μs

Product name	Carrier wave frequency fo(kHz)*
BX-1387	40
BX-1407	38

* See the equivalent circuit and test circuit.
(The carrier wave frequency is possible to be matched to the fo of the transmitter side and shipped.)

*1. Within the arrival distance, it satisfies the specified pulse width under the following conditions.

① Standard transmitter

The transmitter whose output is so adjusted as to become Vo=400 mVp-p by the output waveform as shown in Fig. 1 and using the measuring method as shown in Fig. 2 is specified as the standard transmitter.

However, the infrared photo diode to be used for the transmitter should be λpeak=940 nm, Δλ=60 nm.

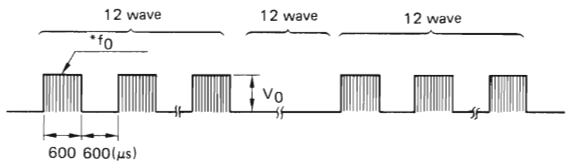


Fig. 1 Output waveform

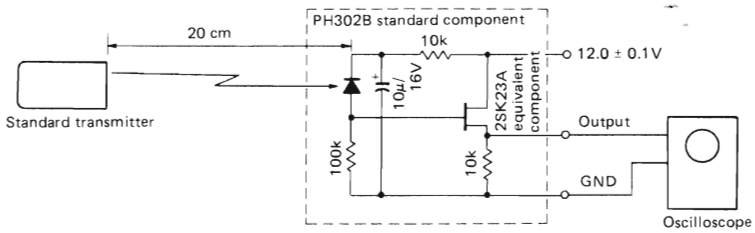


Fig. 2 Measuring method

② Pulse width measuring condition
Specifies at the T_{WL} period and the T_{WH} period of the output pulse by using the aforementioned standard transmitter.

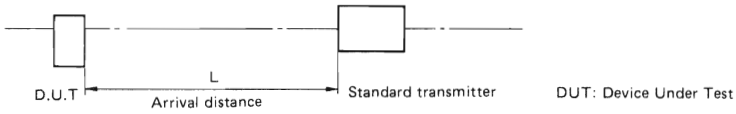


Fig. 3 Measuring condition

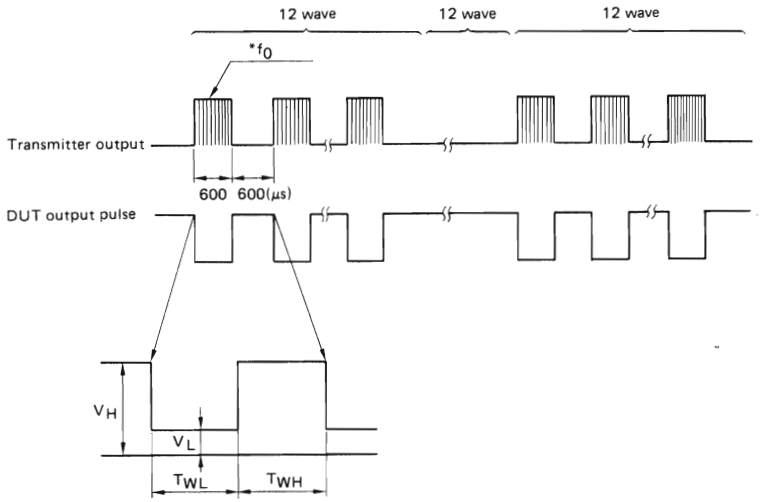
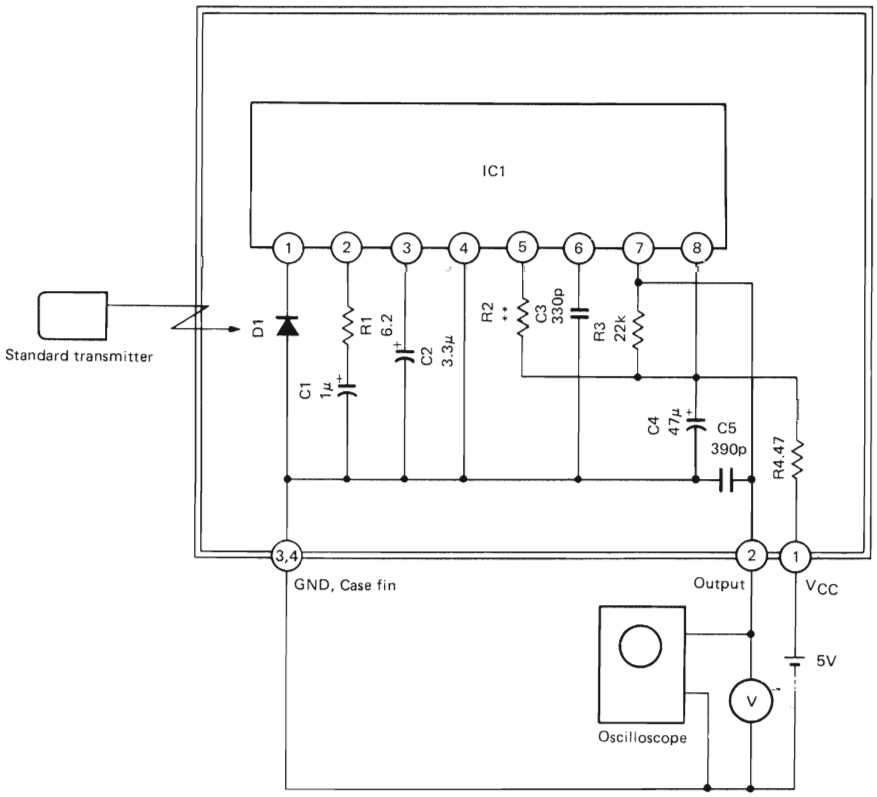


Fig. 4 Output pulse

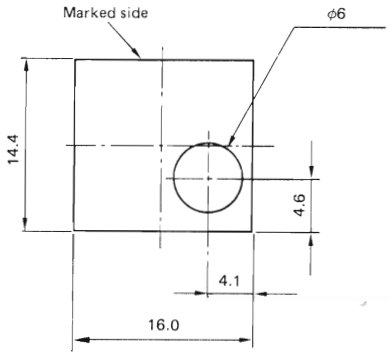
*2. The standard transmitter should be the one specified by *1.
The voltmeter to be used is Z=1.0 MΩ.

Equivalent Circuit and Test Circuit

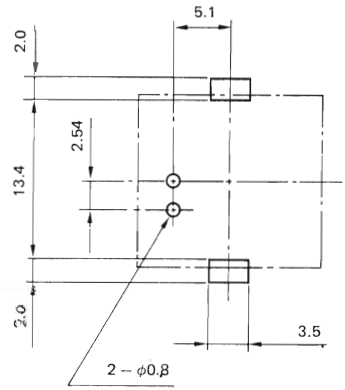


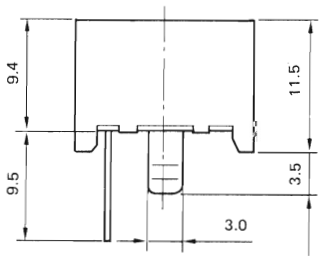
IC1:	CX20106A chip	1. V_{CC}
D1:	PIN photo diode chip	2. Output
C1, C2, C4:	Aluminum electrolytic capacitor	3. GND, Case fin
C3, C5:	SL characteristics, ±5%	4. GND, Case fin
R2:	±1% (Adjusted resistor)	
R (Other than above):	±5%	

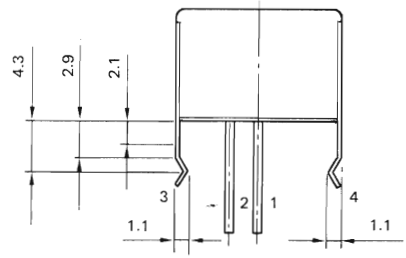
Package Outline and Mark Indication



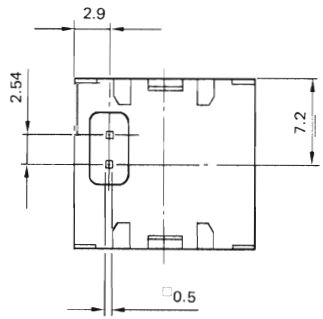
Recommended installation dimension diagram

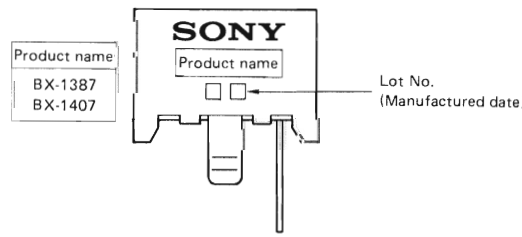






1. V_{CC}
2. Output
3. GND, Case fin
4. GND, Case fin

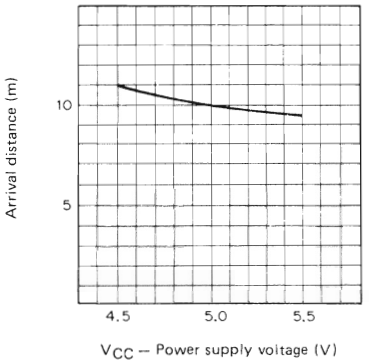




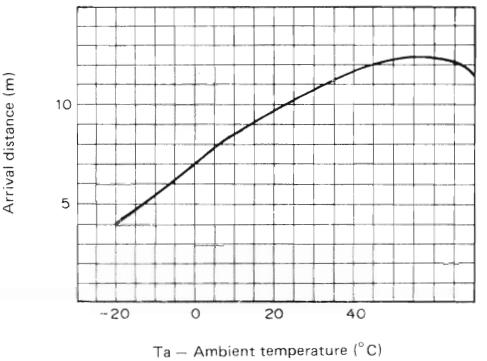
Mark indication

General tolerance: ±0.3 Unit: mm

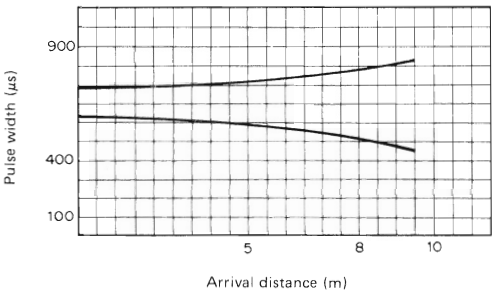
Arrival distance vs. Power supply voltage



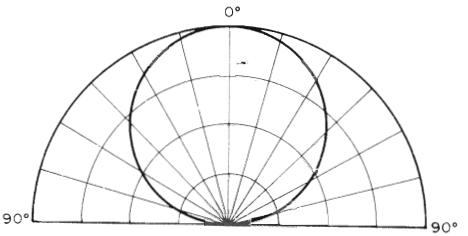
Arrival distance vs. Ambient temperature



Distribution of arrival distance and Pulse width



Directivity



SONY BX-1393/BX-1408

Infrared Remote Control Receiver

Description

The BX-1393/BX-1408 is an ultra miniaturized and highly reliable infrared remote control receiver which has been developed and designed by utilizing the latest hybrid techniques.

It is a can type package which incorporates a pin photo diode and a receiving preamplifier IC (CX20106A).

Features

- Easy to handle ultra miniature type
  Can shaped ultra miniaturized type (equivalent to TO-5), which is 1/4 of the conventional type capacity (0.57 cm^3) has been realized.
- High reliability
  Hermetic seal is employed.
- It can be operated by low voltage and low power consumption.

Structure

Hybrid IC

Applicaiton

- It can be used for TV, VTR, acoustic devices, air conditioners, car stereo units, home computers, and interior controllers.
- High density devices such as 8mm VTR, compact disc etc.
- Vehicle mounting equipments, and outdoor equipments such as garage door opening and closing devices, etc.

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	Vcc	6.3	V
• Storage temperature	Tstg	−40 to +85	°C
• Operating temperature	Topr	−20 to +75	°C

Recommended Operating Condition

• Supply voltage	Vcc	4.7 to 5.3	V

Electrical Characteristics

(Ta=25°C, Vcc=5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	Icc	No signal input	1.1		2.5	mA
Arrival distance	L	*1. At the ray axis	8.0	10.0		m
		The ray receiving surface being at a vertex and against the ray axis: In the range of the cone of 30°	6.5			
		In the range of the cone of 45°	5.0			
Low level output voltage	VL	*2. In the distance of 30 cm on the ray axis			0.5	V
High level output voltage	VH	*2. In the distance of 30 cm on the ray axis	4.5			V
Low level pulse width	TWL	*1. Specified by the TWL period of output within the range of 5 cm to the arrival distance.	410	660	910	μs
High level pulse width	TWH	*1. Specified by the TWH period of output within the range of 5 cm to the arrival distance.	290	540	790	μs

Product name	Carrier wave frequency fo(kHz)*
BX-1393	40
BX-1408	38

* See the Equivalent circuit and Test circuit.
(The carrier wave frequency is possible to be matched to the fo of the transmitter side and shipped.)

*1. Within the arrival distance, it satisfies the specified pulse width under the following conditions.

① Standard transmitter

The transmitter whose output is so adjusted as to become Vo=400 mVp-p by the output waveform as shown in Fig. 1 and using the measuring method as shown in Fig. 2 is specified as the standard transmitter.

However, the infrared photo diode to be used for the transmitter should be λpeak=940 nm, Δλ=60 nm.

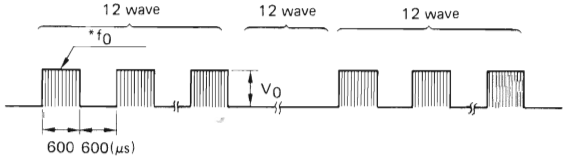


Fig. 1 Output waveform

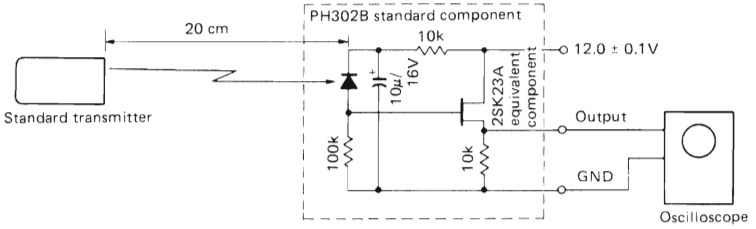


Fig. 2 Measuring method

② Pulse width measuring condition

Specifies at the TWL period and the TWH period of the output pulse by using the aforementioned standard transmitter.

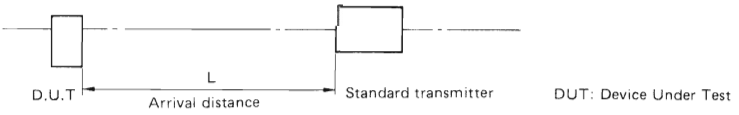


Fig. 3 Measuring condition

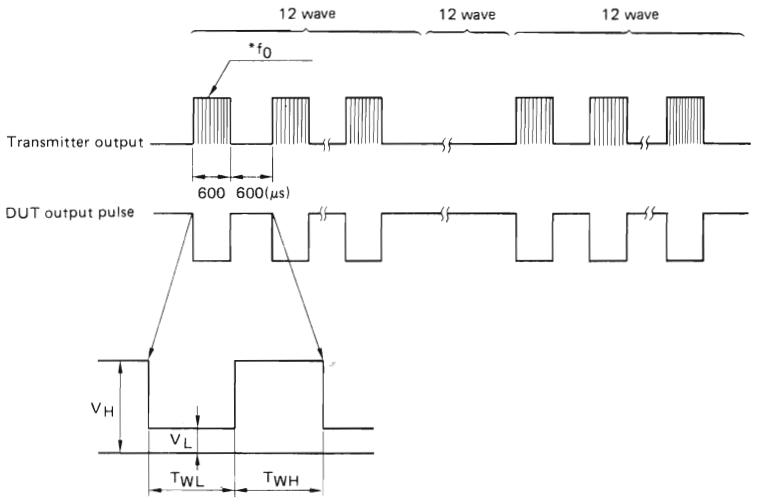
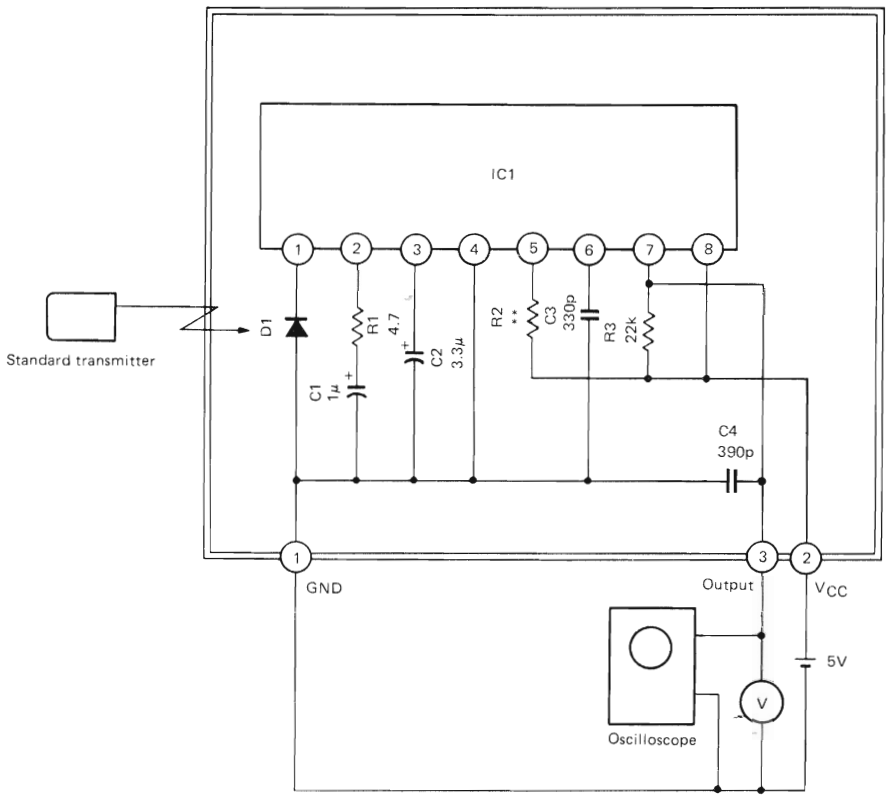


Fig. 4 Output pulse

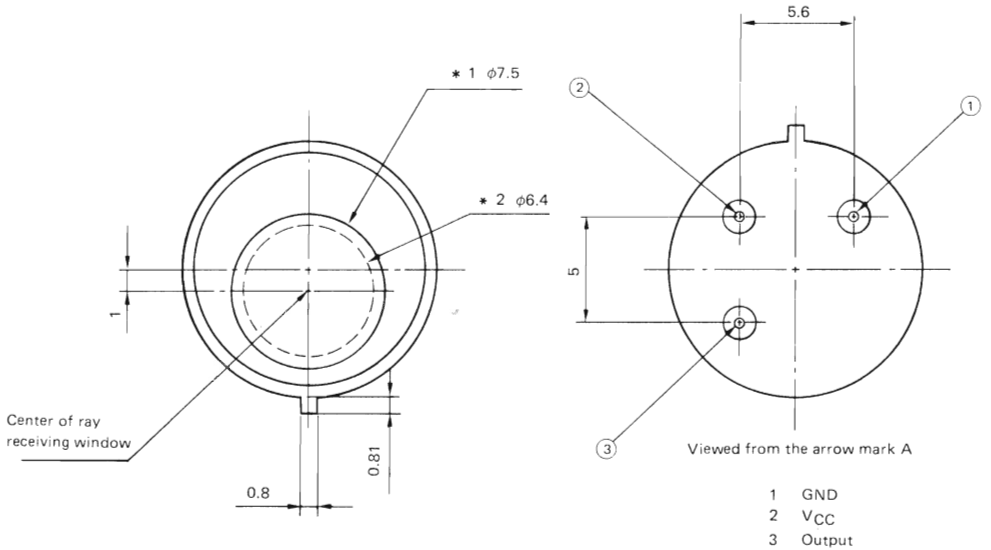
*2. The standard transmitter should be the one specified by *1.
The voltmeter to be used is Z=1.0 MΩ.

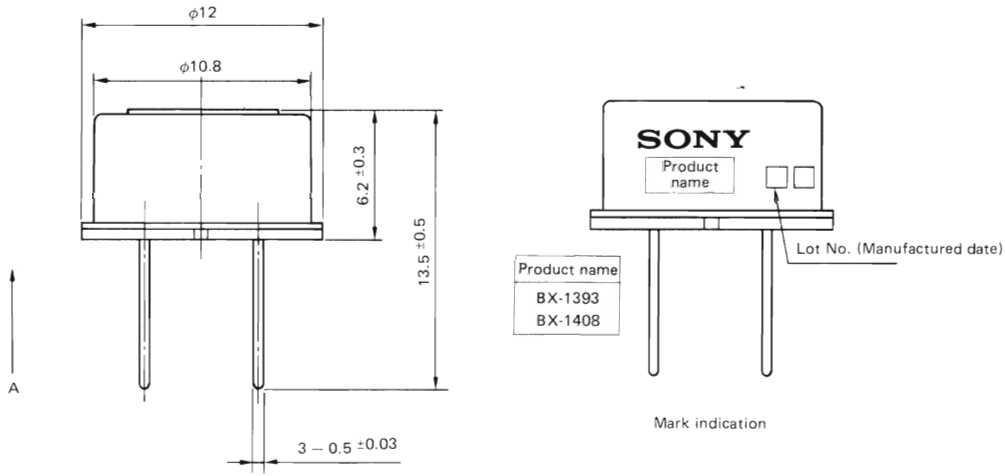
Equivalent Circuit and Test Circuit



IC1:	CX20106A chip	1. GND
D1:	PIN photo diode chip	2. V_{CC}
C1, C2:	Tantalum chip capacitor	3. Output
C3, C4:	SL characteristics, ±5%	
R2:	±1% (Adjusted resistor)	
R (Other than above):	±5%	

Package Outline and Mark Indication





Note * 1 Filter film
* 2 Cavity of ray receiving window

General tolerance: ±0.3

Unit: mm

SONY BX-1398/BX-1409

Infrared Remote Control Receiver

Description

The BX-1398/BX-1409 is a small type infrared remote control system receiver which has been developed and designed by utilizing the latest hybrid technology.

It is a single unit type module which incorporates a pin photo diode and a receiving preamplifier IC (CX20106A).

Features

- A cubic type easy to handle small module
  1) The receiving preamplifier CX20106A which has been developed by Sony Corp. and a pin photo diode are mounted into a single unit type.
  2) Enable to be installed directly as the ray receiving surface is positioned perpendicularly against the mother board.
- Externally attached parts are unnecessary.
- It can be operated by low voltage and low power consumption.

Structure

Hybrid IC

Application

- It can be used for TV, VTR, acoustic devices, air conditioners, car stereo units, home computers, interior controlling appliances, and all other appliances which require remote controlling.

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{CC}	6.3	V
• Storage temperature	Tstg	−20 to +60	°C
• Operating temperature	Topr	−10 to +60	°C

Recommended Operating Condition

• Supply voltage	V_{CC}	4.7 to 5.3	V

Electrical Characteristics

(Ta=25°C, Vcc=5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	Icc	No signal input	1.1		2.5	mA
Arrival distance	L	*1. At the ray axis	8.0	10.0		m
		The ray receiving surface being at a vertex and against the ray axis: In the range of the cone of 30°	6.5			
		In the range of the cone of 45°	5.0			
Low level output voltage	VL	*2. In the distance of 30 cm on the ray axis			0.5	V
High level output voltage	VH	*2. In the distance of 30 cm on the ray axis	4.5			V
Low level pulse width	TWL	*1. Specified by the TWL period of output within the range of 5 cm to the arrival distance.	410	660	910	μs
High level pulse width	TWH	*1. Specified by the TWH period of output within the range of 5 cm to the arrival distance.	290	540	790	μs

Product name	Carrier wave frequency fo(kHz)*
BX-1398	40
BX-1409	38

* See the Equivalent circuit and Test circuit.
(The carrier wave frequency is possible to be matched to the fo of the transmitter side and shipped.)

*1. Within the arrival distance, it satisfies the specified pulse width under the following conditions.

① Standard transmitter

The transmitter whose output is so adjusted as to become Vo=400 mVp-p by the output waveform as shown in Fig. 1 and using the measuring method as shown in Fig. 2 is specified as the standard transmitter.

However, the infrared photo diode to be used for the transmitter should be λpeak=940 nm, Δλ=60 nm.

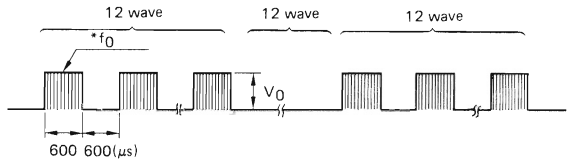


Fig. 1 Output waveform

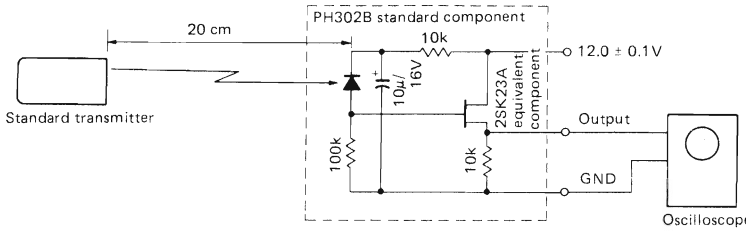


Fig. 2 Measuring method

② Pulse width measuring condition

Specifies at the TWL period and the TWH period of the output pulse by using the aforementioned standard transmitter.

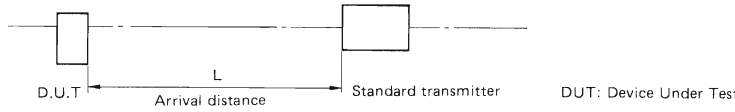


Fig. 3 Measuring condition

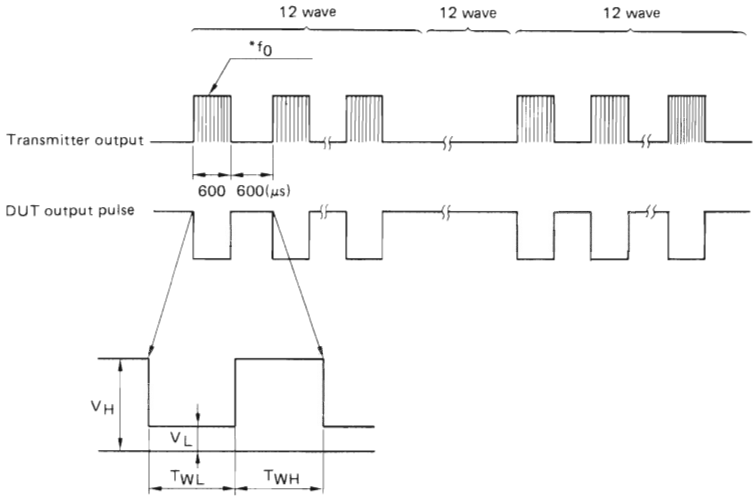
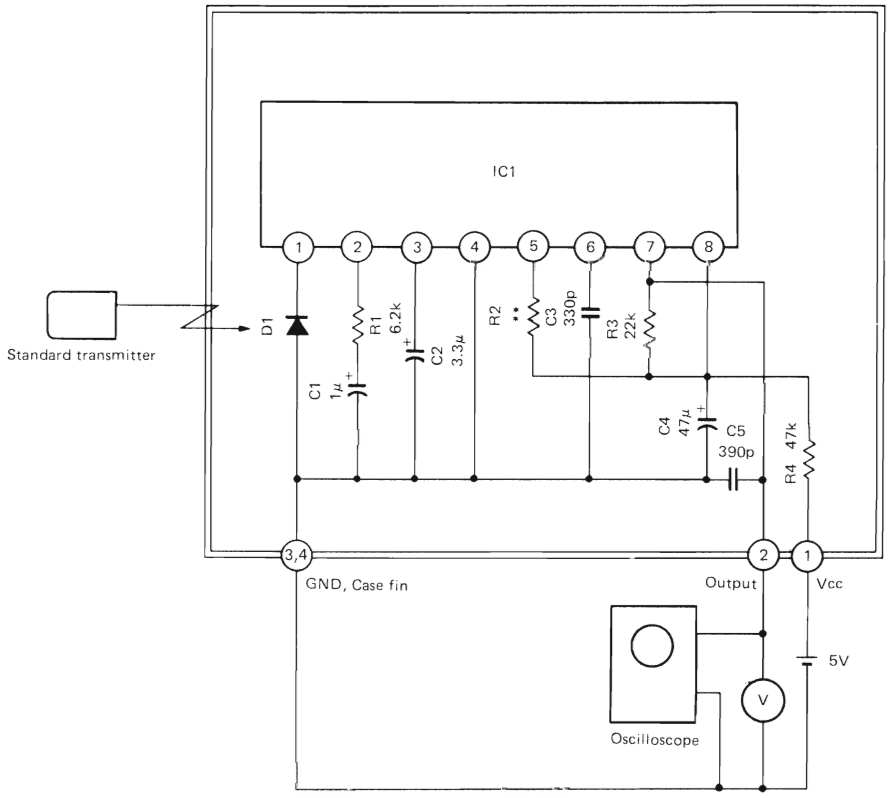


Fig. 4 Output pulse

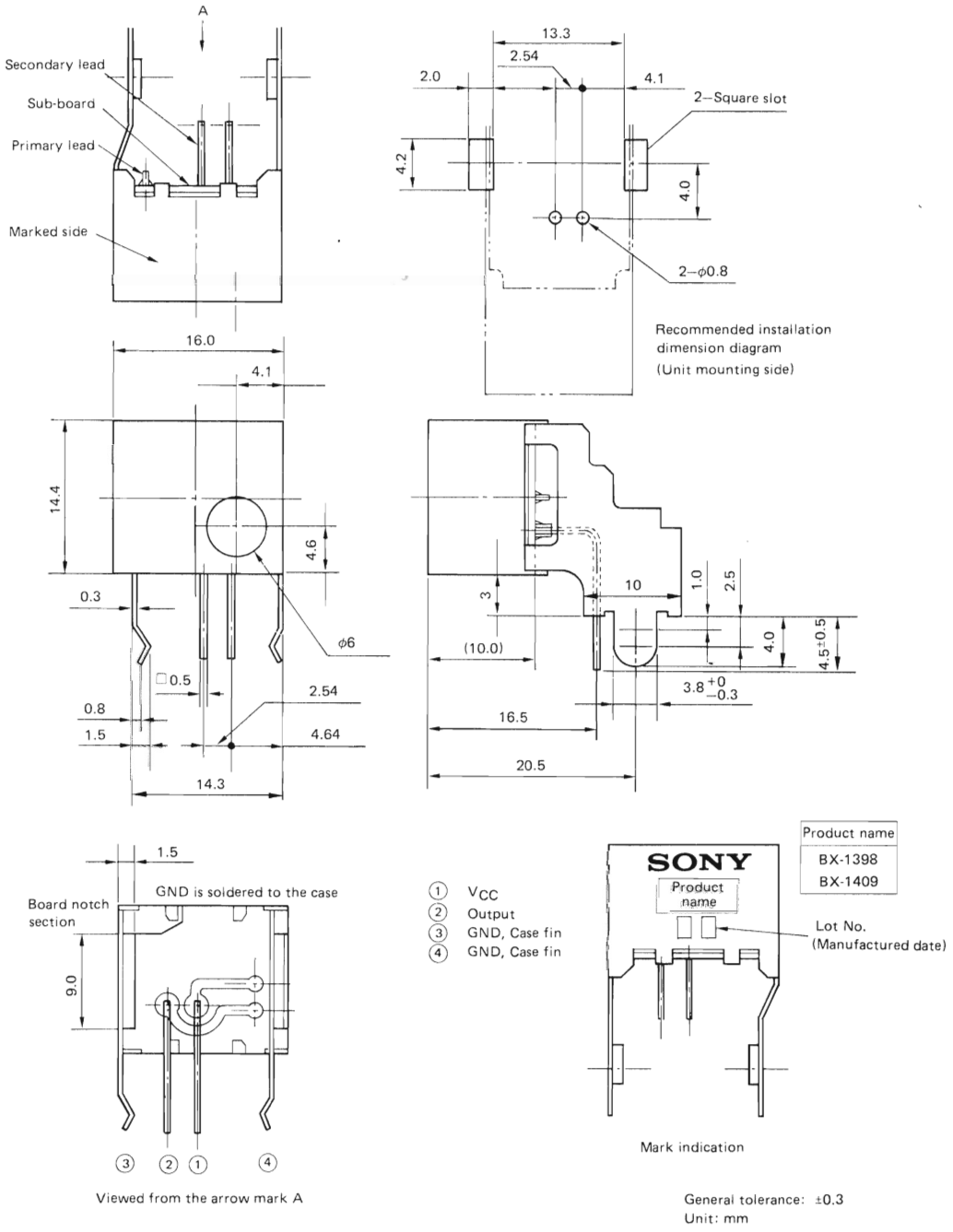
*2. The standard transmitter should be the one specified by *1.
The voltmeter to be used is Z=1.0 MΩ.

Equivalent Circuit and Test Circuit



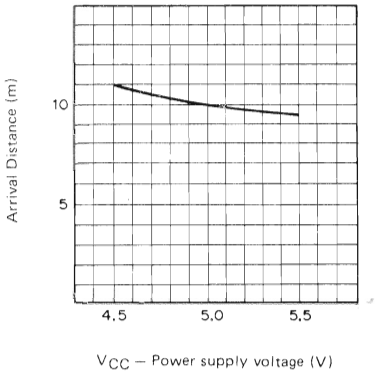
IC1:	CX20106A chip	1. V_{CC}
D1:	PIN photo diode chip	2. Output
C1, C2, C4:	Aluminum electrolytic capacitor	3. GND, Case fin
C3, C5:	SL characteristics, ±5%	4. GND, Case fin
R2:	±1% (Adjusted resistor)	
R (Other than above): ±5%		

Package Outline and Mark Indication

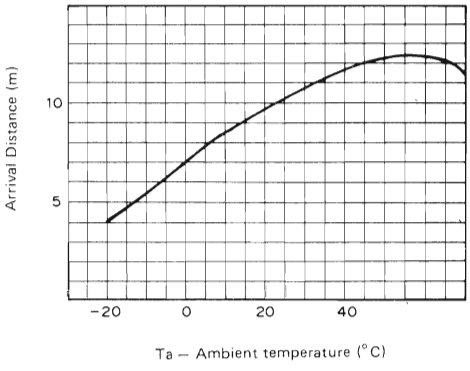


General tolerance: ±0.3
Unit: mm

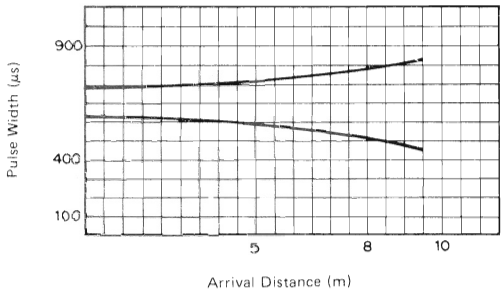
Arrival distance vs. Power supply voltage



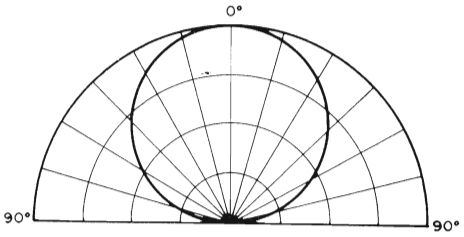
Arrival distance vs. Ambient temperature



Distribution of Arrival Distance and Pulse Width



Directivity

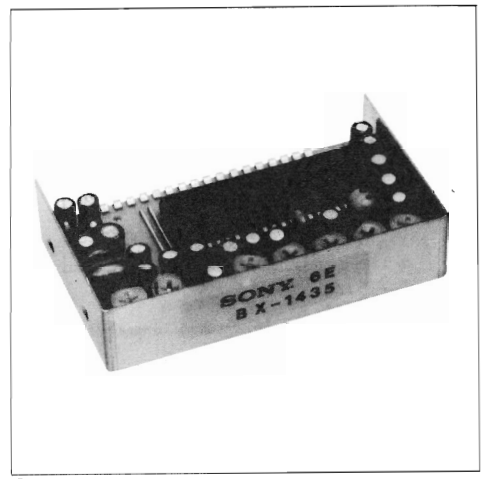


SONY BX-1435

US Multiplex Sound Decoder Module

Description

BX-1435 is the US multiplex sound decoder module for TV set. It consists of CX20112 multiplex sound decoder, CXA1011M-dbx Noise Reduction IC (NR), and all peripheral parts.



See page 8

Features

- All volumes are adjusted. No adjustment is necessary.
- Space saving
- Easy to mount on TV set in production
- SAP (Separate Audio Program) Mute, Mute, Indicating Drive

Functions

- Stereo demodulation
- SAP (Separate Audio Program) demodulation
- MAIN/SAP/BOTH mode selection
- MUTE/SAP MUTE Indicator drive outputs

Structure

Hybrid IC

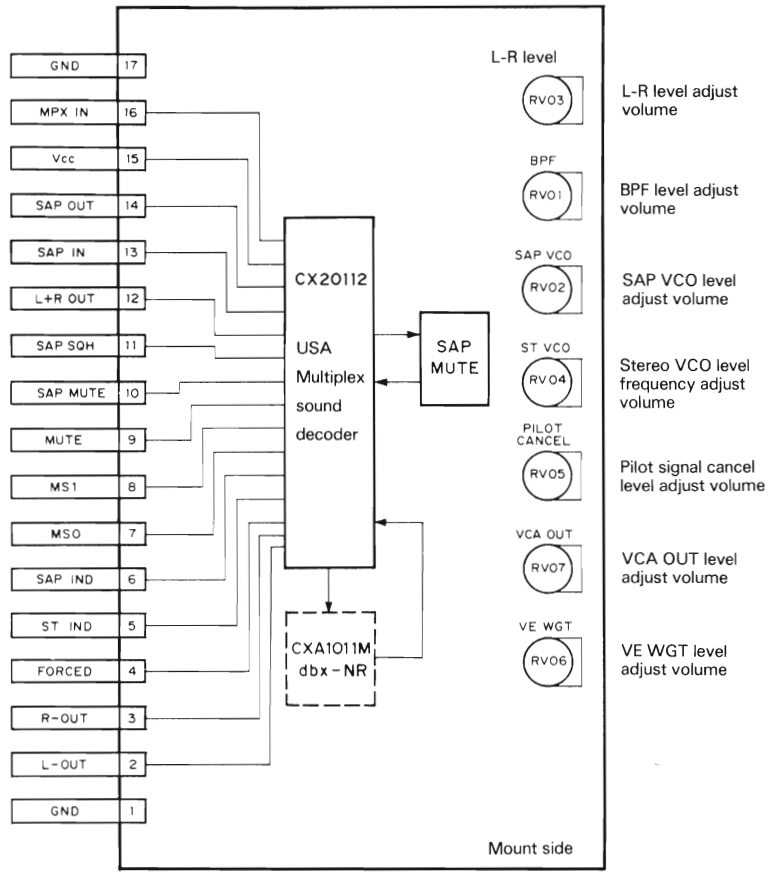
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	17	V
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−40 to +80	°C
• Control input pins	Vcc	4 , 7 , 8 , 9 , 10 , 11	V
• LED drive current	I·LED	40	mA

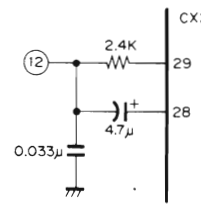
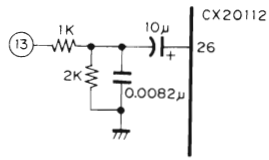
Recommended Operating Condition

• Supply voltage	Vcc	8.7 to 9.3	V

Block Diagram



All volume are adjusted

No.	Symbol	Equivalent circuit	Description
12	L+R OUT		An output pin of L+R. The deemphasis circuit connected between this pin and pin 29 of CX20112.
13	SAP IN		Input the output of pin 14 SAP OUT to this pin. Either one signal of L-R which is L-R signal or this signal is selected by SW, and it is output to pin 24 after going through the low-pass filter.

Electrical Characteristics

(Ta = 25° Vcc = 9.0V ± 0.1V)

	Item	Symbol	SW condition 1	2	3	4	5	6	7	8	9	1*	Test condition: Input signal	Test condition: Test method	Min.	Typ.	Max.	Unit
1	Supply current	I_{CC}										C	No Signal		—	—	60	mA
2	Stereo output level	VST • L	○		○	○			○			A	LCH 100% DSB 400Hz* (1)		− 5.5	− 4.5	− 3.5	dBm
3	SAP output level	VSAP	○	○		○			○			A	SAP 400Hz 100% MOD* (2)		− 5.5	− 4.5	− 3.5	dBm
4	L+R output level	VL+R	○		○	○					○	A	400Hz 0.7Vp-p		− 5.5	− 4.5	− 3.5	dBm
5	Channel balance	△VCB	○		○	○				○		A	RCH 100% DSB 400Hz	(2) — (5)	− 1.0	0	+ 1.0	dBm
6	S/N SAP	VSAP • N	○	○		○			○			A	S 400Hz 100% MOD N 0% MOD* (3)	"A" weight (S) — (N)	54	60	—	dB
7	S/N stereo	VST • N	○		○	○			○			A	S LCH 100% DSB 400Hz N 0% DSB* (4)	"A" weight (S) — (N)	54	60	—	dB
8	S/N monaural	VMN • N	○			○			○			A	S 400Hz 0.7Vp-p N No Signal	"A" weight (S) — (N)	54	60	—	dB
9	SAP distortion level	THD SAP	○	○		○			○			B	SAP 1kHz 100% MOD			1.0	2.0	%
10	Stereo distortion level	THD ST	○		○	○			○			B	LCH 100% DSB 1kHz			0.5	1.0	%
11	Monaural distortion level	THD MN	○			○			○			B	1kHz 0.7Vp-p			0.5	1.0	%
12	400 Hz separation	SEP A	○		○	○			○→○			A	(LCH 30% 400Hz / RCH 30% 2kHz) + fH (0.14Vp-p)	(L) — (R)	30	—	—	dB
13	2 kHz separation	SEP B	○		○	○			○→○			A	(LCH 30% 400Hz / RCH 30% 2kHz) + fH (0.14Vp-p)	(R) — (L)	25	—	—	dB
14	Stereo mute	VMT • ST	○		○	○	○					A	LCH 100% DSB 400Hz	"A" weight			−70	dBm
15	SAP mute	VMT • SAP	○	○		○		○				A	SAP 400Hz 100% MOD	"A" weight			−70	dBm

Note) 1* = Test point

*(1) LCH 100% DSB 400 Hz : 400 Hz DSB (2 f_H 0.7 Vp-p) + f_H (0.14 Vp-p) + 400 Hz (0.35 Vp-p)

*(2) SAP 400 Hz 100 MOD : 5 f_H ± 10 kHz FM modulation 0.42 Vp-p

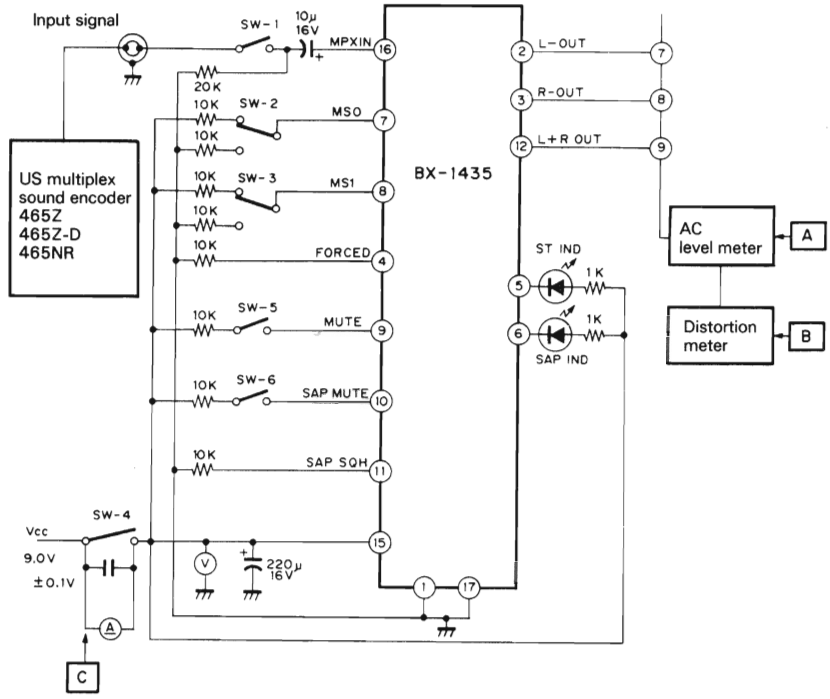
*(3) SAP 0% MOD : 5 f_H 0.42 Vp-p

*(4) LCH 0% MOD : 0% modulation

*During setting test condition, this IC is not active, but it will be active when measurement is done.

SONY

Test Circuit



A = Test point

Mode Matrix

MODE FUNCTION

No.		LINE OUT	
⑦	⑧	L	R
L	L	L+R	SAP
L	H	L	R
H	L	SAP	SAP
H	H	(MUTE)	

FORCED MONAURAL FUNCTION

No.	LINE OUT		STEREO
④	L	R	INDICATOR
L	L	R	ON
M	L+R	L+R	ON
H	L+R	L+R	OFF

SAP SQH (squelch) INHIBIT FUNCTION

No.		SAP
⑪	SQH	INDICATOR
L	ON	ON
M	OFF	ON
H	OFF	OFF

Description of Operation

This IC is USA TV audio multiplexing decoder which has the baseband spectrum as shown in Fig. 1. The flows of the signals are roughly separated into 3; namely L+R (MAIN), L−R (SUB) and SAP as shown in Fig. 2.

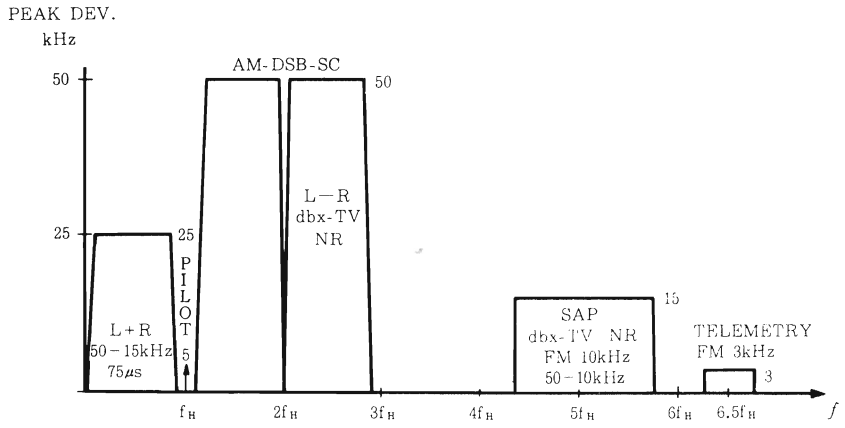


Fig. 1 Baseband spectrum

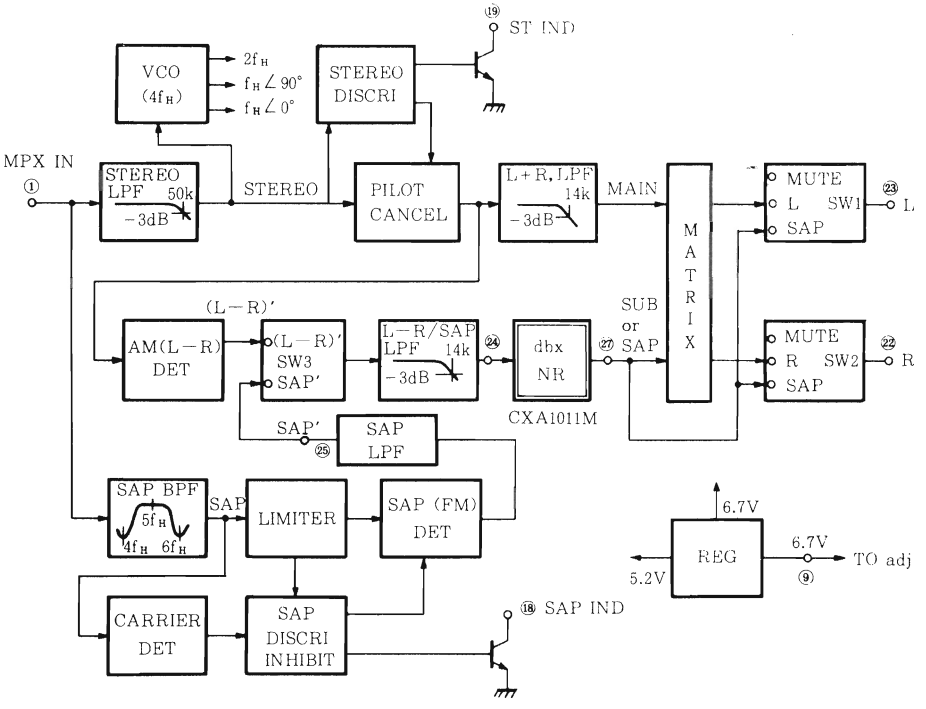


Fig. 2 Block diagram

A. L+R (MAIN)
MPX signal is input from pin 1, and SAP and TELEMETRY are eliminated with stereo LPF. Then, pilot cancellation is carried out. Finally, L−R is eliminated with L+R LPF and L+R only is selected to be input to the matrix.

B. L−R (SUB)
Up to the pilot cancellation, similar to L+R. Since L−R is an AM-DSB, amplitude modulation is carried out. At this point, up to 15 kHz there exists L−R on the signal spectrum and also signals remain in the high frequency band. The signal is being encoded with dbx, therefore, it is represented as (L−R)' in Fig. 2. Then, select (L−R)' and SAP', and they are input to SW3 allows to use LPF and dbx noise reducton circuits to be used commonly, and the residual signals in the high frequency band are eliminated with L−R/SAP LPF. As L−R is being applied to dbx NR, connect dbx noise reduction decoder between pins 24 and 27. After this, it is input to the matrix as L−R (SUB).

C. SAP is FM signal whose carrier is of 5 fH therefore, eliminates only the SAP signal is eliminated by using a BPF of 5 fH. It is input to SW3 after it is FM detected. The rear stage from SW3 is a combined use with L−R. SAP, in the figure means SAP' signal which is being encoded with dbx.

D. In addition to the above, there is a mode discriminating circuit. Discrimination of stereo is carried out by detecting the amplitude of the pilot signal. Discrimination of SAP is carried out by detecting the carier of 5 fH. VCO generates 4 fH with PLL and provides 2 fH, fH <90°, and fH <0° by dividing it with a flip-flop. 2 fH is used for AM detection, fH <90° for PLL, and fH <0° to extract the pilot signal. The regulator provides voltages of 6.7V and 5.2V and those are supplied to the individual circuits within the IC, 6.7V is also output to pin 9 which is used as a regulation voltage.
L+R and L−R are separated into L and R with the matrix, and they are input to SW1 and SW2. SW1 and SW2 are used with mode selection pins to allocate the outputs of pin 23 L and pin 22 R to either one of L+R, SAP, MUTE, L and R.

Notes on Application

1. The pilot cancellation amount can be improved by connecting a variable resistance between pins 30 and 31 .
The adjusting method is to input 15.734 kHz, 0.14 Vp-p to pin 1 first, then observe the level from pin 40 through the 15.734 kHz BPF, and adjust with the volume so that it becomes minimum.

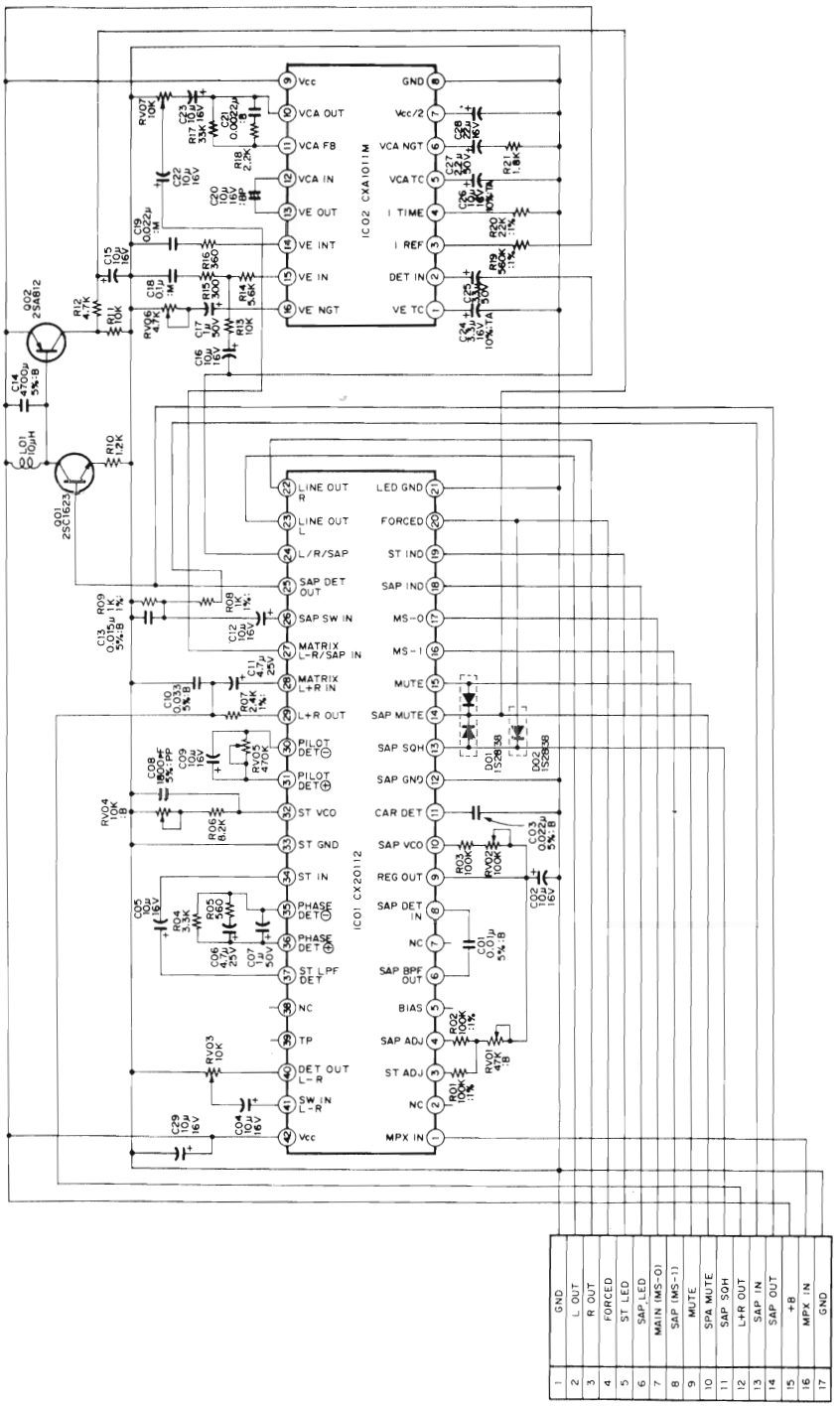
2. The DC loop gain can be reduced by connecting a resistance between pins 36 and 35. (Makes it possible to change the capture range)

3. L and R level adjustment (pins 40 to 41)
Input a signal of 400 Hz, pre-emphasis off, VR off and SUB 100%. Set the mode of the IC into stereo (set pin 17 to V×L and pin 16 to V×H). At this point, adjust the level of NR IN so that it becomes 100% of the level that is specified with NR.

4. SAP adjustment (pins 25 to 26)
Input a signal of 400 Hz, noise reduction off, and SAP 100% modulated. Set the mode of IC into SAP mode (set pin 17 to V×H and pin 16 to V×L). At this point, adjust the level of NR IN so that it becomes 100% of the level that is specified with NR.

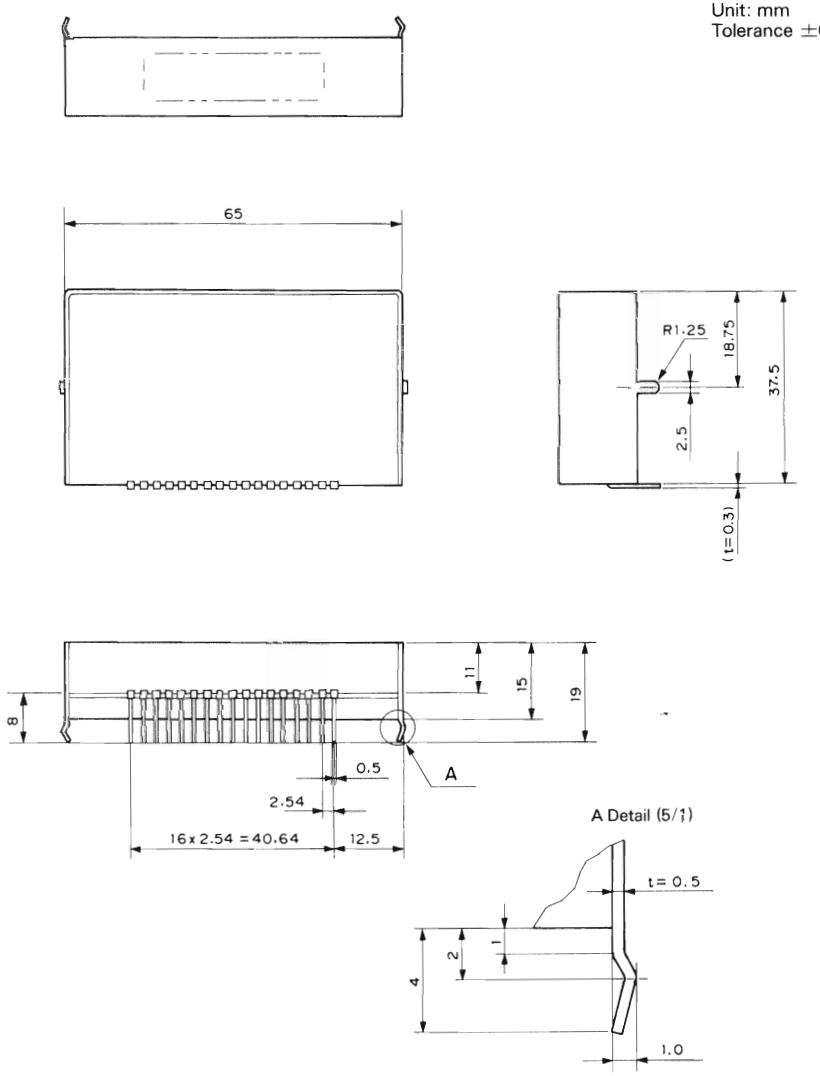
5. Separation adjustment (NR OUT to pin 27)
First, adjustment of the noise reduction circuit should be carried out. Then, adjust the input level of pin 27 so that separation at individual frequencies becomes maximum.

Equivalent Circuit



Package Outline

Unit: mm
Tolerance ±0.3

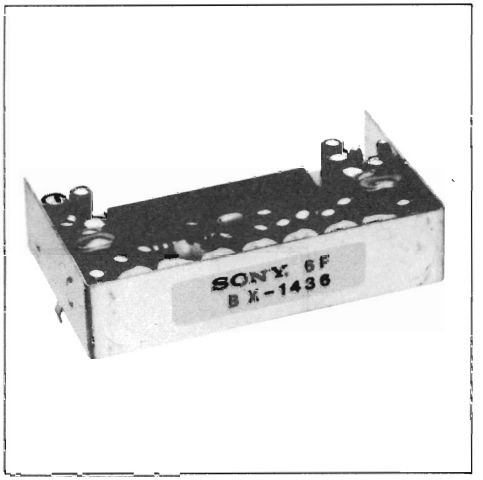


SONY BX-1436

US Multiplex Sound Decoder Module

Description

BX-1436 is a US type multiplex sound decoder module (Hybrid integrated circuit). It is composed of 2 IC's: Multiplex sound decoder IC (CX20112) and dbx noise reduction IC (CXA1011M).



Features

- Stereo demodulation
- SAP (Separate Audio Program) demodulation
- L+R output
- SAP Mute, Mute, Indicating drive
- Forced monaural, SAP squelch

Structure

Hybrid IC

Absolute Maximum Ratings

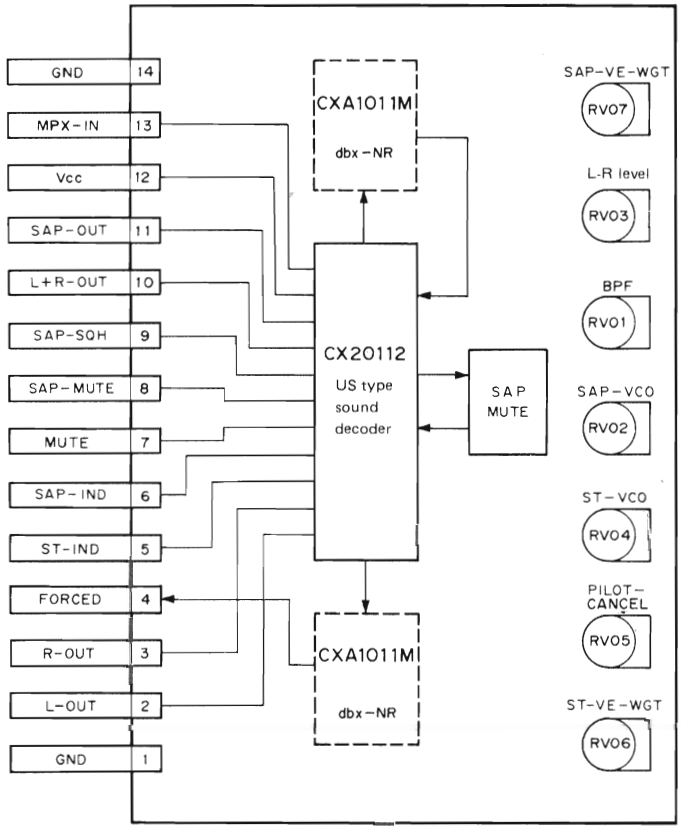
• Supply voltage	Vcc	17	V
• Input voltage of respective control pins		④, ⑦, ⑧, ⑨	Vcc V
• LED drive current	I·LED	40	mA
• Operating temperature	Topr	−10 to +60	°C
• Storage temperature	Tstg	−40 to +80	°C

Recommended Operating Condition

• Supply voltage	Vcc	8.7 to 9.3	V

Note) This module is available only to the licenses of the dbx-TV noise reduction system.

Block Diagram



Electrical Characteristics

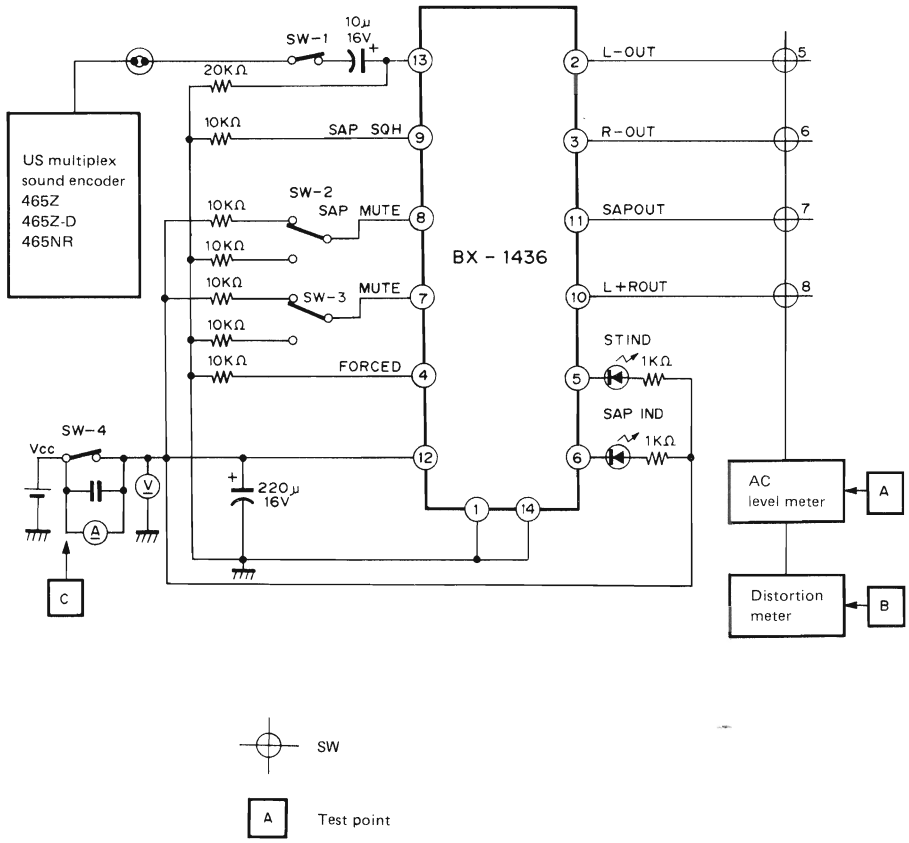
(Ta=25°C Vcc=9.0V±0.1V)

No.	Item	Symbol	SW condition								Test point	Test condition		Min.	Typ.	Max.	Unit
			1	2	3	4	5	6	7	8		Input signal	Test method				
1	Supply current	Icc									C	No signal		–	–	60	mA
2	Stereo output level	VST • L	○			○	○				A	LCH 100% DSB 400Hz *(1)		−5.3	−4.3	−3.3	dBm
3	SAP output level	VSAP	○			○			○		A	SAP 400Hz 100% MOD *(2)		−5.3	−3.8	−2.3	dBm
4	L+R output level	VL+R	○			○				○	A	400Hz 0.7Vp-p		−5.3	−4.3	−3.3	dBm
5	Channel balance	ΔVCB	○			○		○			A	RCH 100% DSB 400Hz	(2)−(5)	−1.0	0	+1.0	dBm
6	S/N SAP	VSAP • N	○			○			○		A	S 400Hz 100% MOD N 0% MOD *(3)	"A" Weight (S)−(N)	54	60	–	dB
7	S/N stereo	VST • N	○			○	○				A	S LCH 100% DSB 400Hz N 0% DSB *(4)	"A" Weight (S)−(N)	54	60	–	dB
8	S/N monaural	VMN • N	○			○	○				A	S 400Hz 0.7Vp-p N, No signal	"A" Weight (S)−(N)	54	60	–	dB
9	SAP distortion level	THD SAP	○			○			○		B	SAP 1kHz 100% MOD			1.0	2.0	%
10	Stereo distortion level	THD ST	○			○	○				B	LCH 100% DSB 1kHz			0.5	1.0	%
11	Monaural distortion level	THD MN	○			○	○				B	1kHz 0.7Vp-p			0.5	1.0	%
12	400Hz separation	SEP A	○			○	○	○			A	(LCH 30% 400Hz)+f_H(0.14Vp-p)	(L)−(R)	30	–	–	dB
13	2kHz separation	SEP B	○			○	○	○			A	(RCH 30% 2kHz)+f_H(0.14Vp-p)	(R)−(L)	25	–	–	dB
14	Stereo mute	VMT • ST	○		○	○	○				A	LCH 100% DSB 400Hz	"A" Weight			−70	dBm
15	SAP mute	VMT • SAP	○	○		○			○		A	SAP 400Hz 100% MOD	"A" Weight			−70	dBm

*(1) LCH 100% DSB 400Hz : 400 Hz DSB($2f_H$ 0.7 Vp-p)+f_H(0.14 Vp-p)+400 Hz(0.35 Vp-p)
*(2) SAP 400 Hz 100% MOD: $5f_H$±10 kHz FM modulation 0.42 Vp-p
*(3) SAP 0% MOD : $5f_H$ 0.42 Vp-p
*(4) LCH 0% MOD : 0% modulation DSB($2f_H$)+f_H(0.14 Vp-p)
* During setting test condition, dbx IC is not active, but it will be active when measurement is done.

SONY®

Test Circuit



Mode Matrix

SAP SQH (squelch) INHIBIT FUNCTION

No.		SAP
⑨	SQH	INDICATOR
L	ON	ON
M	OFF	ON
H	OFF	OFF

FORCED MONAURAL FUNCTION

No.	LINE OUT		STEREO
④	L	R	INDICATOR
L	L	R	ON
M	L+R	L+R	ON
H	L+R	L+R	OFF

Description of Operation (CX20112)

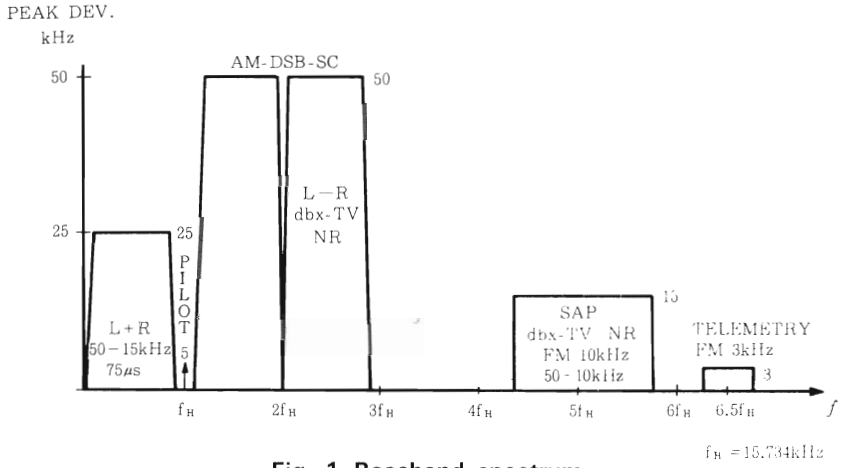


Fig. 1 Baseband spectrum

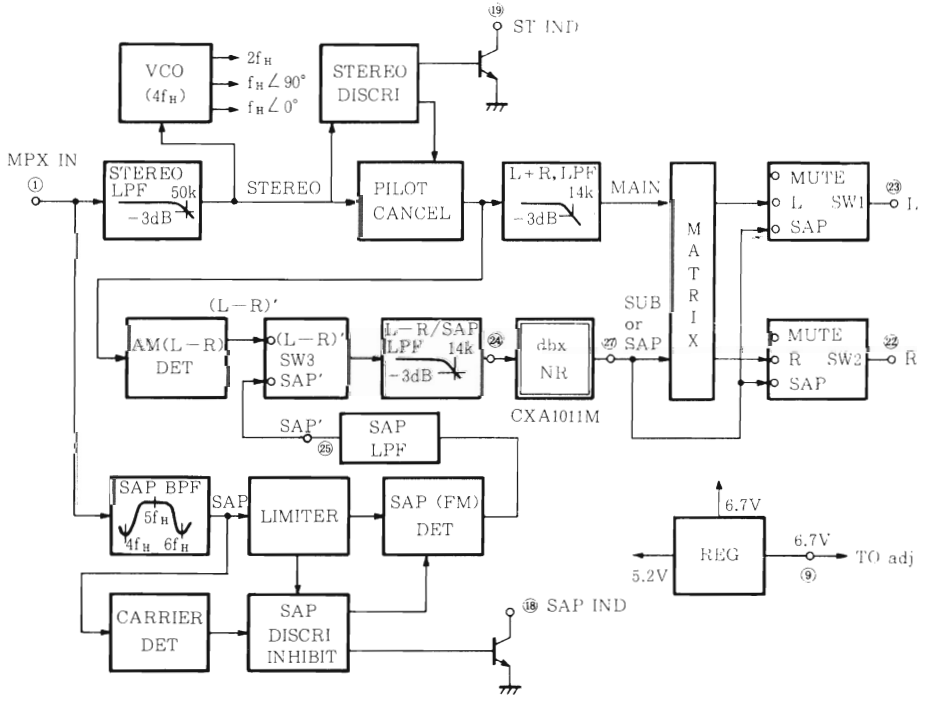


Fig. 2 Block diagram

This IC is US TV sound multiplexing decoder which has the baseband spectrum as shown in Fig. 1. The flows of the signals are roughly separated into 3; namely L:R (MAIN), L-R (SUB) and SAP as shown in Fig. 2.

A. L+R (MAIN)
MPX signal is input from pin①, and SAP and TELEMETRY are eliminated with stereo LPF. Then, pilot cancellation is carried out. Finally, L−R is eliminated with L+R LPF and L+R only is selected to be input to the matrix.

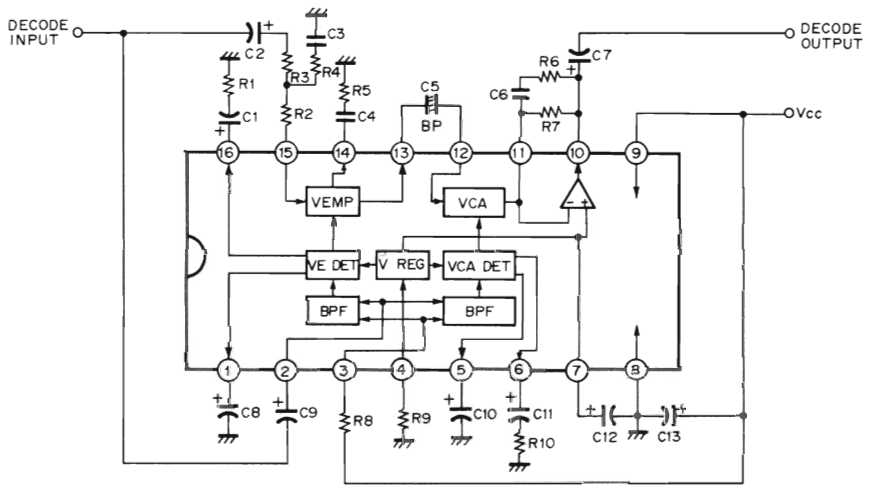
B. L−R (SUB)
Up to the pilot cancellation, similar to L+R. Since L−R is an AM-DSB, amplitude modulation is carried out. At this point, up to 15 kHz there exists L−R on the signal spectrum and also signals remain in the high frequency band. The signal is being encoded with dbx, therefore, it is represented as (L−R)' in Fig. 2. Then, select (L−R)' and SAP', and they are input to SW3 allows to use LPF and dbx noise reduction circuits to be used commonly, and the residual signals in the high frequency band are eliminated with L−R/SAP LPF. As L−R is being applied to dbx NR, connect dbx noise reduction decoder between pins ㉔ and ㉗. After this, it is input to the matrix as L−R (SUB).

C. SAP
SAP is FM signal whose carrier is of $5f_H$, therefore, eliminates only the SAP signal is eliminated by using a BPF of $5f_H$. It is input to SW3 after it is FM detected. The rear stage from SW3 is a combined use with L−R. SAP' in the figure means SAP signal which is being encoded with dbx.

D. In addition to the above, there is mode discriminating circuit. Discrimination of stereo is carried out by detecting the amplitude of the pilot signal. Discrimination of SAP is carried out by detecting the carrier of $5f_H$. VCO generates $4f_H$ with PLL and provides $2f_H$, $f_H 90°$, and and $f_H \angle 0°$ by dividing it with a flip-flop. $2f_H$ is used for AM detection, $f_H \angle 90°$ for PLL, and $f_H \angle 0°$ to extract the pilot signal. The regulator provides voltages of 6.7V and 5.2V and those are supplied to the individual circuits within the IC, 6.7V is also output to pin⑨ which is used as a regulation voltage.
L+R and L−R are separated into L and R with the matrix, and they are input to SW1 and SW2. SW1 and SW2 are used with mode selection pins to allocate the outputs of of pin ㉓ L and pin ㉒ R to either one of L:R, SAP, MUTE, L and R.

Description of Operation (CXA1011M)

(1) dbx-TV decoder characteristics



Basic application circuit

The Basic Application Circuit diagram shows dbx-TV NR decode circuit using CXA1011M. An input signal is fed to the variable de-emphasis circuit through the fixed de-emphasis circuit which is composed of R2 to R4, C2 and C3. The output signal is fed to VCA through C5. The signal current from VCA is converted into output voltage by an operational amplifier. To this are fed the other de-emphasis characteristics composed of R6, R7 and C6 to provide the decode output.
Individual RMS detectors give predetermined weighting characteristics to the input signal through the bandpass filters, to detect signals of RMS value and obtain the control signal.

(2) Block description

(2)-1 Variable de-emphasis circuit
This is an amplifier with high frequency response controlled by the control signal of the RMS detector.
Variable de-emphasis characteristics are determined by the RC series circuit of VE INT pin (Pin 14) and the current of ITIME pin (Pin 4).

(2)-2 VCA circuit
This is a variable gain amplifier controlled by the control signal of the RMS detector for VCA.

(2)-3 RMS detector for the variable de-emphasis circuit

It detects the RMS value of the current flowing in VE WGT pin (Pin 6) to control the variable de-emphasis circuit.

The input current, which makes the variable de-emphasis characteristics flat, is the reference input current of the RMS detector. In this IC it is set at 7.5μ Arms.

The specified attack and recovery time constants are determined by the capacitor of VE TC pin (Pin 1).

(2)-4 RMS detector circuit for VCA

It detects RMS value of the current flowing in the VCA WGT pin (Pin 6) to control VCA gain.

The input current which gives unity current to VCA is the reference input current of the RMS detector. In this IC it is set at 15μ Arms.

The specified attack and Recovery time constants are determined by the capacitor of VCA TC pin (Pin 5).

(2)-5 Bandpass filter for variable de-emphasis

The bandpass filter for variable de-emphasis is formed by an integrated active filter with the characteristics of a 2nd order lowpass filter (fo=20 kHz, Q=0.69), a 2nd order highpass filter (fo=7.66 kHz, Q=0.95) and a 1st order highpass filter (fo=3.92 kHz).

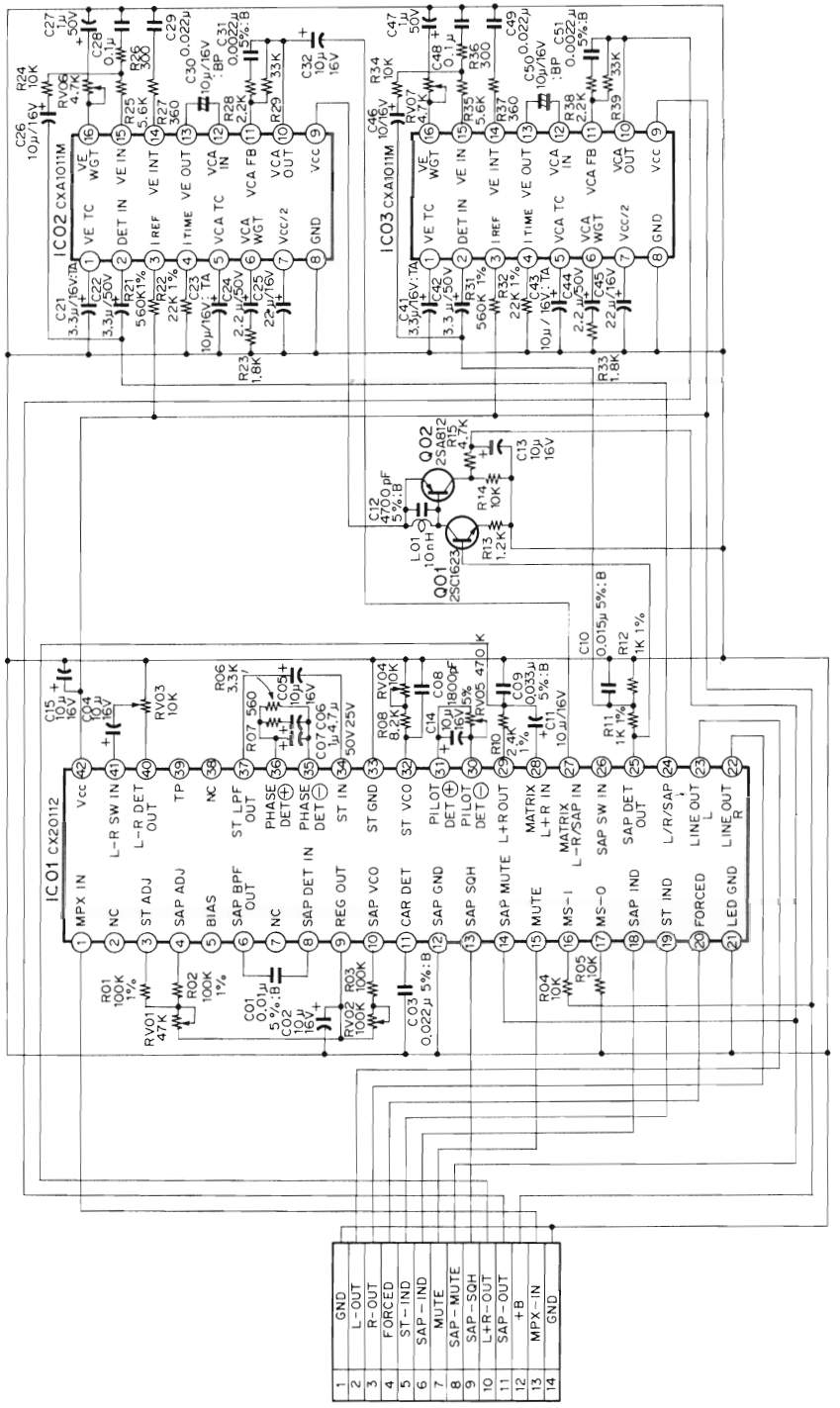
The cut-off frequency of the bandpass filter is determined by the reference current flowing in IREF pin (Pin 3).

(2)-6 VCA band pass filter

It is formed by an integrated active filter circuit possessing the characteristics of a 1st order lowpass filter (fo=2.09 kHz) and the RC time constant circuit connected to VCA WCT pin.

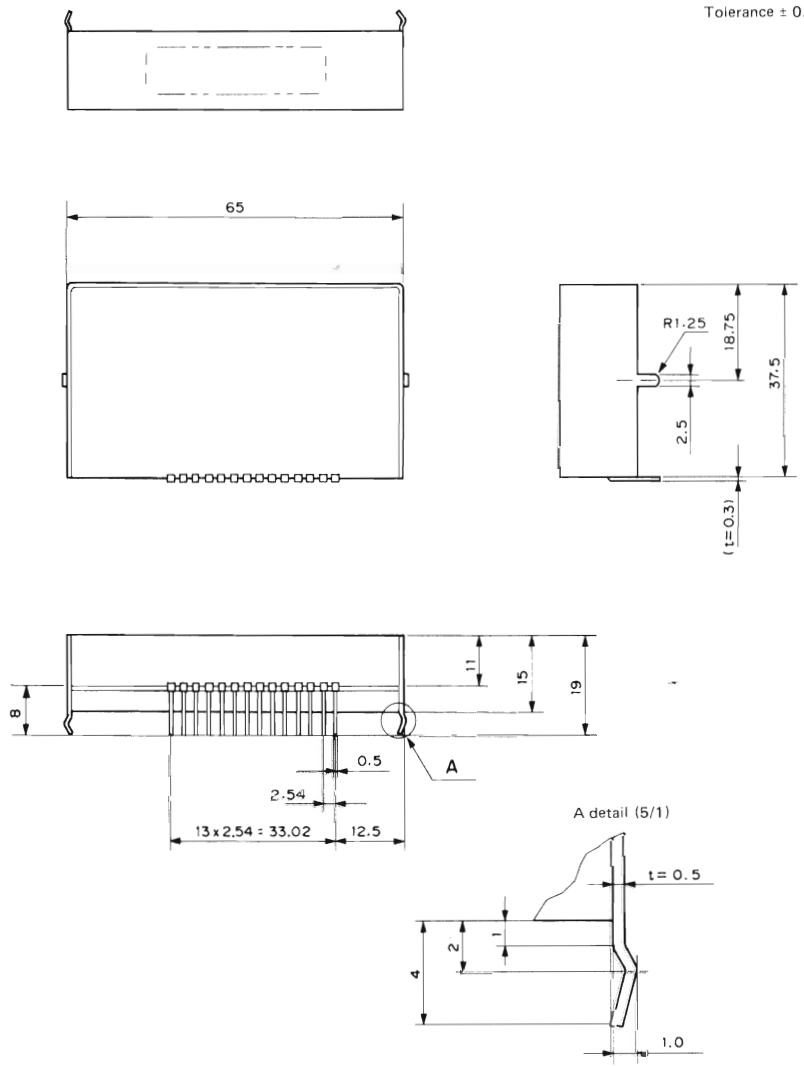
The cut-off frequency of the bandpass filter is determined by the reference current flowing in IREF (the same as for variable de-emphasis bandpass filter) pin (Pin 3).

Equivalent Circuit



Package Outline

Unit: mm
Tolerance ± 0.3



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